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A reconfigurable SAR ADC with pseudo-multiple sampling and calibration for CMOS image sensors

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Abstract: This paper presents a resolution reconfigurable two-step successive approximation register analog-to-digital (A/D) converter (ADC) with the pseudo-multiple sampling (PMS) and gain error calibration method for CMOS image sensors. The proposed ADC can be configured with 10-bit, 11-bit and 12-bit by adjusting the number of 10-bit A/D conversions, thereby satisfying various demands in different situations. The PMS method enables the attainment of high-resolution ADC results by summing the conversion outputs of several low-resolution ADCs, thereby reducing the number of unit capacitors and the area of the capacitor array. A compensation technique is proposed to expand the quantization range and improve the effective resolution of the proposed ADC. A calibration method suitable for bottom-plate sampling is proposed, which reduces the gain error between reference voltages. Simulated in a 55 nm process, the proposed ADC in the 12-bit mode achieves a differential nonlinearity of +0.47/−0.50 least significant bit (LSB) and an integral nonlinearity of +0.75/−0.84 LSB at a sampling frequency of 3.497×10^5 per second with the calibration. The effective number of bits reaches 11.63 bits. The area occupied by a single ADC column is 39.5 μm×119.2 μm and the power consumption is 62.8 μW.

Key words: CMOS image sensor (CIS); reconfigurable analog-to-digital (A/D) converter (ADC); successive approximation register (SAR); error calibration; pseudo-multiple sampling (PMS)

0 Introduction

CMOS image sensors (CISs) exhibit numerous advantages, such as low power consumption, cost-effective production, high integration levels, and low noise. As a result, CISs are widely used in mobile phones, digital cameras, facial recognition, and medical applications. As a critical module within CISs, the column-parallel analog-to-digital (A/D) converter (ADC) is essential in improving the performance of CISs. However, traditional column-parallel ADCs, such as successive approximation register (SAR) ADCs[1-5] and single-slope (SS) ADCs[6-9], are difficult to meet the demands for speed and area efficiency while maintaining high precision. To overcome these limitations, more advanced segmented ADC architectures have been proposed. Two-step (TS) SS ADCs[10-14] feature a compact design and simple structure, but suffer from prolonged conversion times. SAR/SS ADCs[15-17] achieve well-balanced trade-offs among conversion speed, chip area, and accuracy. However, the complex digital logic may introduce additional overhead in terms of power consumption and cost. TS SAR ADCs[18-23] stand out for their fast conversion speed and high resolution, making them especially suitable for high-speed and high-precision CIS applications. However, as the resolution increases, the corresponding area grows exponentially.

Introducing two scaled reference voltages can effectively reduce the area of the capacitor array[20,23]. However, these scaled reference voltages have a strict proportional relationship with the original reference voltages, and the inaccuracy of scaled reference voltages can introduce gain errors in the lower-bit conversions. Therefore, it is necessary to calibrate the scaled reference voltages to minimize gain errors during lower-bit conversion and improve the linearity of the ADC. A pseudo-multiple sampling (PMS) method applied to SAR ADCs achieves high-resolution A/D conversion by repeatedly lifting the input voltage for multiple conversions, summing the digital codes from each conversion, and then enabling a high-resolution ADC with a low-resolution DAC[20]. However, this method significantly extends the time required for a single conversion. Moreover, the PMS method requires raising the input voltage by one least significant bit (LSB)

during each conversion. If the initial input voltage already reaches the upper limit of the quantization range of ADC, subsequent increases will exceed this range, resulting in the loss of code.

As the resolution of ADC increases, the time and power consumption associated with A/D conversion also grows proportionally, making it difficult to meet the demands of practical applications. Reconfigurable ADCs have been proposed[2,7,15,17], with optimized performance by balancing key parameters such as resolution, conversion time, and power consumption. A 10-bit digital-to-analog converter (DAC) is utilized to achieve a resolution of 8-bit to 10-bit[2]. The study employs a switching method to determine whether the high-order capacitors are connected to the DAC array. However, this method requires a 10-bit DAC area for all modes, incurring additional overhead. Adjusting the slope of a ramp signal enables reconfigurable resolution[7,15]. Although the ramp-based method supports high resolution, it increases the A/D conversion time, which is unsuitable for high-speed CIS applications.

This paper presents a resolution-reconfigurable TS SAR ADC. We utilize the PMS method to adjust the number of A/D conversions and achieve the resolutions of 10-bit to 12-bit with only a 5-bit DAC capacitor array, effectively reducing the area of the capacitor array. An error compensation technique is proposed to address the errors in the PMS method, preventing the input voltage from exceeding the quantization range of the ADC. Additionally, a calibration module is introduced to mitigate the gain errors during A/D conversions, thereby improving the linearity of the ADC. Concurrently, the calibration is achieved through a resistor array, which can be performed externally to an ADC array, thereby avoiding any additional area overhead on the ADC array. The remainder of this paper is organized as follows: Section 1 introduces the error compensation and reference voltage calibration methods for PMS methods, Section 2 presents the overall architecture of the SAR ADC and its sub-modules, Section 3 proposes the calibration method for two scaled reference voltages, Section 4 discusses the simulation results, and a conclusion is drawn in Section 5.

1 Proposed TS SAR ADC

1.1 Principle of PMS method

The principle of the PMS method is to achieve a high-resolution ADC by summing the outputs of multiple low-resolution ADCs[24]. In Fig.1, a 4-bit output can be achieved by accumulating four 2-bit outputs. Since the least significant bit (LSB) of an ADC halves with each additional bit, the LSB of a 2-bit ADC is four times larger than that of a 4-bit ADC in the same conditions. Additionally, the input voltage of each 2-bit ADC introduces an offset corresponding to 1 LSB of the 4-bit ADC based on the input voltage of the previous 2-bit ADC. The outputs of four 2-bit ADCs are processed by performing A/D conversions, followed by the summation of the resulting four digital codes. The resulting digital code represents the output of the 4-bit ADC. However, when the digital code value of the 4-bit ADC exceeds 12, the PMS method will surpass the quantization range of the 3-bit and 2-bit ADCs, resulting in an inability to obtain accurate digital code values and consequently leading to errors.

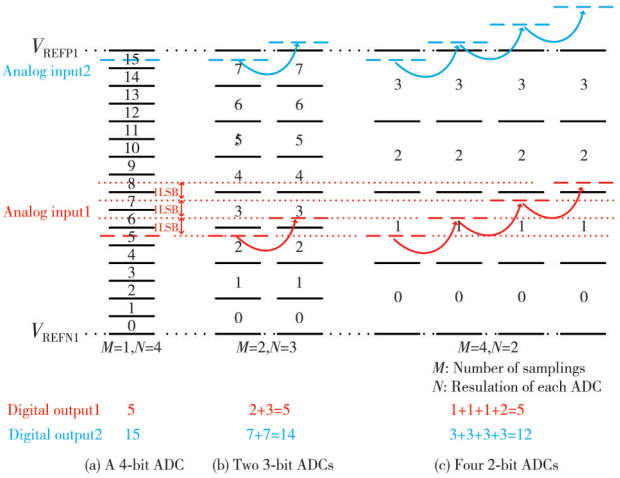


Fig. 1 Principles of PMS method and associated errors

1.2 Proposed compensation technique for errors in PMS method

Errors discussed in Section 1.1 will affect the quantization range of the ADC. Therefore, it is essential to detect and compensate for these errors. This study proposes an error compensation technique for quantization range overflow, as shown in Fig.2.

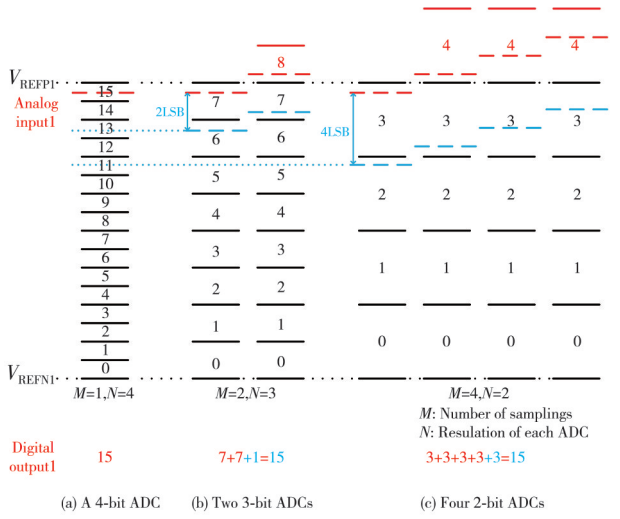


Fig. 2 Principle of compensation technique of PMS method

The input voltage is then offset downward by 1 shift voltage before proceeding with the A/D conversion. If the LSB of the resulting digital code drops from 1 to 0, it indicates no code loss, and the error detection concludes. If the LSB remains 1, the input voltage is further offset downward by additional shift voltage for the next A/D conversion. If the LSB drops from 1 to 0, 1 code value has been lost. Therefore, the accumulated digital code values should be increased by 1 from the original values. If the input voltage must be offset downward by four shift voltages for the LSB to drop from 1 to 0. In that case, the accumulated digital code values will be incremented by 3 from the original values.

1.3 Reconfigurable resolution

The proposed ADC features three modes: 10-bit, 11-bit, and 12-bit. The timing diagram of 10-bit mode is illustrated in Fig. 3(a). For the 11-bit ADC mode, the PMS method performs four 10-bit A/D conversions. The first two conversions generate an 11-bit digital output, while the subsequent two conversions provide error compensation. After the first sampling, the lower plate voltage of the unit capacitor is switched from the high reference input voltage V_{REFP1} to the shifted input voltage V_{SHIFT}. We define the full scale V_{F} as

$$V_{\mathrm{F}} = V_{\mathrm{REFP1}} - V_{\mathrm{REFN1}}, \tag{1}$$

where V_{REFN1} represents the low reference input voltage. The value of V_{SHIFT} is

$$V_{\mathrm{SHIFT}} = V_{\mathrm{REFP1}} + V_{\mathrm{F}}/2^{6}. \tag{2}$$

A 10-bit A/D conversion is conducted using a 10-bit capacitor array, yielding the first 10-bit digital code. The voltages across the capacitor are then reset and resampled. The value of V_{SHIFT} is decreased by $V_{\mathrm{F}}/2^{6}$, while the bottom plate voltage of the unit capacitor remains at V_{REFP1}. A second A/D conversion follows, producing the second 10-bit digital code. Next, an error detection operation is performed by further reducing V_{SHIFT} by $V_{\mathrm{F}}/2^{6}$. The voltage on the bottom plate of the unit capacitor is switched from V_{REFP1} to $V_{\mathrm{REFP1}} - V_{\mathrm{F}}/2^{6}$. According to the procedure outlined in section 1.2, an 11-bit error detection code is obtained. The final 11-bit digital output code is generated by adding the error output code to the sum of the two 10-bit digital codes from the A/D conversions. A simplified timing diagram for the single-line conversion process is shown in Fig. 3(b).

In the 12-bit ADC mode, the PMS operation requires eight 10-bit A/D conversions, where the first four 10-bit A/D conversions generate four 10-bit digital codes, and the last four 10-bit A/D conversions are used for error compensation. The operational procedure is identical to that of the 11-bit mode, except that the voltage decrease of V_{SHIFT} now transitions from $V_{\mathrm{F}}/2^{6}$ to $V_{\mathrm{F}}/2^{7}$. The four 10-bit digital codes are summed, followed by four error detection steps to produce the final 12-bit digital code. A simplified timing diagram for single-row conversion is shown in Fig. 3(c).

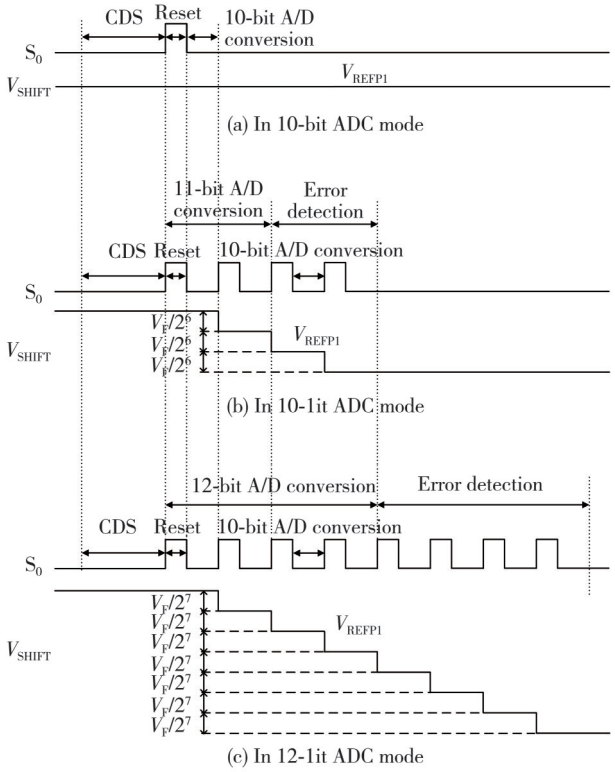


Fig. 3 Timing diagram of three modes of proposed ADC

2 Circuit implementation

2.1 Architecture of proposed SAR ADC

This section presents the design of a reconfigurable TS SAR ADC, which supports 10-bit, 11-bit, and 12-bit three modes using a 10-bit DAC. Fig. 4 illustrates the schematic of the proposed TS SAR ADC, which comprises a non-binary capacitor array, a high-speed comparator, and a SAR logic. There are four reference voltages in the proposed ADC. The two input reference voltages, V_{REFP1} and V_{REFN1}, define the conversion range for the upper 5 bits. The two scaled reference voltages, V_{REFP2} and V_{REFN2}, determine the conversion range for the lower 5 bits. The values of V_{REFP2} and V_{REFN2} are

$$V_{\mathrm{REFP2}} = V_{\mathrm{REFP1}} - V_{\mathrm{F}}/2^{5}, \tag{3}$$

$$V_{\mathrm{REFN2}} = V_{\mathrm{REFN1}} - V_{\mathrm{F}}/2^{5}. \tag{4}$$

In the reset state, switch S_0 is closed, and all the top plates of capacitors are connected to the same potential V_{CM} as the negative terminal of the comparator. All multiplexers select the input voltage V_{CDS} that has passed through the

analog correlated double sampling (CDS) circuit. After the reset state ends, the sampling state starts. S_0 is opened, and the voltages on the bottom plates of all the capacitors are set to V_{REFP1}.

After the sampling phase is completed, the proposed ADC enters the coarse conversion phase. The control switch of the SAR ADC toggles, causing the voltage on the lower plate of capacitor C_6 to switch from V_{REFP1} to V_{REFN1}. If the comparison result of the comparator is 1, the voltage on the bottom plate of C_6 remains at V_{REFN1}, and the highest digital code value, B_9, is 1. If the comparison result of the comparator is 0, the voltage on the bottom plate of C_6 switches from V_{REFN1} back to V_{REFP1}, making the highest digital code value, B_9, equal to 0. This operation is repeated for the remaining capacitors to obtain the highest five digital code values.

Subsequently, the fine transition phase commences. The SAR logic controls the multiplexers to select V_{REFP2} or V_{REFN2} based on the decisions made during the coarse conversion phase. If B_9 is 1 (0), the voltage on the bottom plate of C_6 is V_{REFN1} (V_{REFP1}). The SAR logic controls the multiplexers switches from V_{REFN1} (V_{REFP1}) to V_{REFN2} (V_{REFP2}) for comparison. Based on the comparison result of the comparator, it determines whether to maintain the voltage on the lower plate of capacitor C_6 at V_{REFN2} (V_{REFP2}) or switch it back to V_{REFN1} (V_{REFP1}).

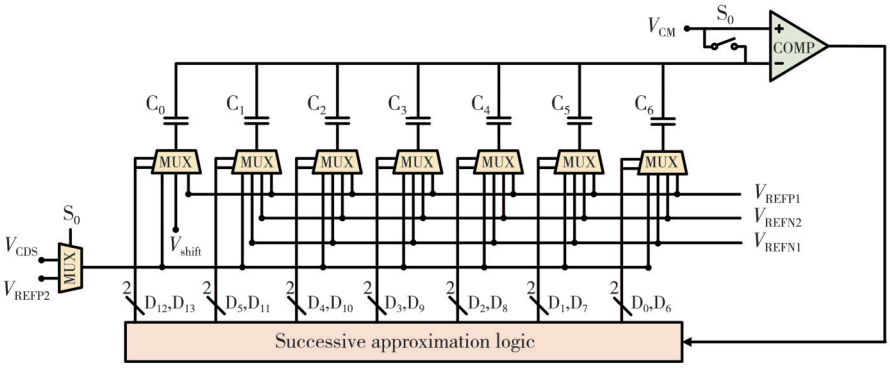


Fig. 4 Block diagram of proposed SAR ADC

2.2 Design of redundant capacitance

A binary redundancy weighting method is employed[1], which requires that any non-binary weighted capacitor be expressed as a combination of two binary-weighted capacitors. Additionally, the weight value of each capacitor must be less than or equal to the sum of the weight values of all lower-order capacitors.

The DAC capacitor array in this study consists of 32 capacitors. The weight of the highest-order capacitor, 2^4, is spited into two capacitors with weights of 2^4—2^1 and 2^1, while the weight of the second-highest-order capacitor, 2^3, is spited into two capacitors with weights of 2^3—2^0 and 2^0, respectively. The weights of 2 and 1 are then combined to form a new weighted capacitor of 2^1+2^0. Thus, the weights of the capacitor array are 14, 7, 4, 3, 2, and 1. The digital output B_{OUT0} is

$$\begin{aligned} B_{OUT0} &= (2^4-2^1)B_5+(2^3-2^0)B_4+ \\ &2^2B_3+(2^1+2^0)B_2+2^1B_1+2^0B_0= \\ &2^4B_5+2^3B_4+2^2B_3+2^1(B_2+B_1-B_5)+ \\ &2^0(B_2+B_0-B_4). \end{aligned} \tag{5}$$

A single-step conversion for a 5-bit ADC requires six cycles, while a two-step conversion for a 10-bit ADC requires twelve cycles. The complete 10-bit digital output B_{OUT1} is

$$\begin{aligned} B_{OUT1} &= 2^9B_{11}+2^8B_{10}+2^7B_9+2^6(B_8+B_7-B_{11})+ \\ &2^5(B_8+B_6-B_{10})+2^4B_5+2^3B_4+2^2B_3+ \\ &2^1(B_2+B_1-B_5)+2^0(B_2+B_0-B_4). \end{aligned} \tag{6}$$

The redundancy method can relax the establishment requirements for the reference buffer and DAC circuits, effectively reducing the power consumption of the reference buffer and increasing the operational speed of the SAR ADC.

2.3 Comparator

A multi-stage comparator cascade with output offset storage technology performs offset storage operations[25], eliminating input voltage offsets. Given that the supply voltage is 2.5 V and the input voltage range is 0.8—1.8 V, all comparators utilize NMOS transistor input structures for better performance. From preAmp1 to preAmp3, the gain of the three amplifiers is set to 20 dB. The dynamic latch comparator operates in two phases: the reset phase and the comparison phase. When CLK is low, the transistor M_9 is turned on, shorting the voltages at both ends to ensure their initial potentials are the same. When CLK goes high, both ends begin to discharge simultaneously. Through a positive feedback loop formed by two inverters, the side with the more significant input voltage discharges faster until it approaches the GND voltage, producing a comparison result.

The offset storage comparator has two operational

phases: the offset storage phase and the amplification phase. During the offset storage phase, the input and output terminals of preAmp1 and preAmp2 are shorted to the common mode voltage V_{CM} via switches, storing the offset voltage on capacitors C_1 to C_4, with the voltage difference between the positive and negative terminals being opposite in polarity to the output offset voltage of the amplifier. The stored offset voltage on the capacitor $V_{OS,OUT}$ is

$$V_{OS,OUT} = -A_v V_{OS,IN}, \tag{7}$$

where A_v represents the gain of the preamplifier and $V_{OS,IN}$ denotes the input offset voltage. After the offset voltage storage, the comparator enters the amplification phase. The switches are opened, disconnecting the input and output terminals of the comparator from V_{CM}, and the input terminal of the first stage amplifier is switched to the input voltage. The voltage difference at the output terminal of the amplifier V_{OUT} is

$$V_{OUT} = A_v(V_{IP} - V_{IN} + V_{OS,IN}) - A_v V_{OS,IN} = A_v(V_{IP} - V_{IN}), \tag{8}$$

where V_{IP} and V_{IN} represent the input voltage of the positive and negative terminals of the comparator, respectively. The offset voltage of the comparator has been eliminated. A simplified schematic of the comparator is shown in Fig.5.

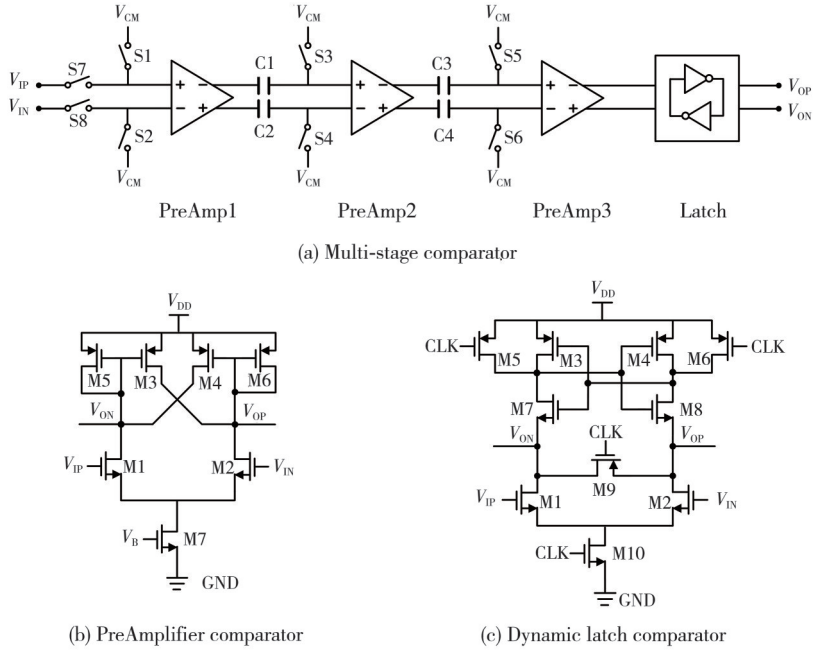


Fig. 5 Schematic diagram of comparator

2.4 Analog CDS circuit

The PMS method can reduce the area of the capacitor array by increasing the number of conversions. Doubling the number of A/D conversion steps allows for saving 1 bit of the most significant capacitor, thereby reducing the capacitor array area by half. The digital CDS method requires performing a complete A/D conversion for both the reset and sampling signals to obtain the output digital code value, and the correct digital code value is determined by subtracting the two output values. Thus, the digital CDS method will increase the number of A/D conversions for the SAR ADC. For instance, employing the PMS method to reduce the capacitor array area by 3/4 necessitates four A/D conversions. If the digital CDS method is applied, eight A/D conversions would be required to obtain the final digital code value, significantly increasing the conversion time for a complete readout cycle. In contrast, the analog CDS method can effectively reduce the number of A/D conversions needed for a readout cycle. The sampling signal undergoes the CDS operation via analog circuitry, followed by four A/D conversions to yield the final digital code value. Compared to the digital CDS method, a complete readout cycle of the analog CDS method can save time equivalent to four A/D conversions, effectively reducing the conversion time for that cycle.

Although the accuracy of the analog CDS method is relatively lower than that of the digital CDS method, the redundant capacitor design can tolerate some errors without sacrificing precision. The schematic diagram of the analog CDS circuit is illustrated in Fig.6. In the reset state, S_1 and S_2 are closed while S_3 is open, storing the offset voltage of the operational amplifier and low-frequency noise on the capacitor C_C. In the sampling state, S_3 closes while S_1 and S_2 open. The input signal is integrated and amplified, with the resulting value stored again on the capacitor C_C.

The offset voltage of the operational amplifier is nearly constant. Given the very short time interval

between the two inputs, noise only varies minimally. Thus, effectively eliminating the fixed offset voltage while mitigating the influence of noise.

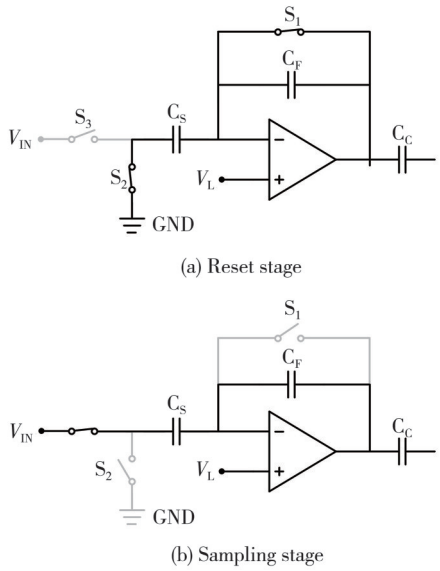


Fig. 6 Analog CDS circuit

3 Calibration

The two scaled reference voltages exhibit a strict proportional relationship with the reference voltages of the two inputs. Consequently, any inaccuracy in the scaled reference voltages will introduce a gain error between the upper 5 bits and the lower 5 bits. Yoshioka previously proposed an in-chip self-calibration method for split capacitor linearity[26], which assesses the equality of the weight of a specific capacitor and the sum of the weights of all lower-order capacitors by comparing digital output codes. Calibration is deemed complete if the output codes from two conversions are equal.

This study proposes a new calibration method suitable for sampling the bottom plate of the capacitor. Initially, the reference voltage V_{REFP2} is calibrated. The lower plates of the upper 5-bit capacitors, C_6-C_2, and the unit capacitor, C_0, are connected to V_{REFP1}. The lower plate of the lowest-bit capacitor, C_1, is connected to V_{REFN1}. The value of the equivalent input voltage V_{IN} is

$$V_{IN} = V_{REFP1} \times 31/32 + V_{REFN1} \times 1/32. \quad (9)$$

If the A/D conversion is performed at this time, the voltage at the positive and negative terminals of the comparator will equalize after the sixth conversion, introducing a new calibration error. A shift voltage V_S is applied to the bottom plate of C_0 after the sampling stage to avoid the calibration error. The input of V_S appropriately lowers the voltage on the top plates of all the capacitors, effectively preventing the comparator's positive and negative terminal voltages from equaling. However, the input of V_S should be less than $V_F/2^6$ to stay within the quantization range of the ADC. Furthermore, V_S should be added to prevent equal voltages at the comparator terminals during the fine conversion phase. Then an A/D conversion proceeds, resulting in the first 10-bit digital code, B_{CAL1}. Following this A/D conversion, a reset sampling operation is performed while the bottom plates of all the capacitors are connected to V_{REFP2}. The value of the equivalent input voltage V_{IN} is

$$V_{IN} = V_{REFP2}. \quad (10)$$

The same shift voltage V_S is applied to the bottom plate of C_0 after the sampling stage, followed by an A/D conversion to obtain the second 10-bit digital code, B_{CAL2}. If the digital codes received from two A/D conversions are identical, the input voltages for the two conversions are equal, it indicates that the completion of the calibration for V_{REFP2}. If the digital codes are different, the value of V_{REFP2} will be adjusted based on the relative magnitude of B_{CAL2} and B_{CAL1}, and the calibration process is repeated until the digital codes of two consecutive A/D conversions are equal.

Next, the reference voltage V_{REFN2} is calibrated. The calibration principle is identical to that of V_{REFP2}. The bottom plates of the highest six capacitors, C_6-C_1, are connected to V_{REFN1}, while the bottom plate of C_0 is connected to V_{REFP1}. The value of the equivalent input voltage V_{IN} is

$$V_{IN} = V_{REFN1} \times 31/32 + V_{REFP1} \times 1/32. \quad (11)$$

A shift voltage V_S is applied to the bottom plate of C_0, ensuring that the input V_S does not cause the positive and negative terminal voltages of the comparator to be equal. A 10-bit A/D conversion is then performed to obtain the first 10-bit digital code value, B_{CAL3}.

After resetting and sampling, the bottom plates of the highest five capacitors, C_6-C_2, are connected to V_{REFN2}, and the bottom plates of C_1 and C_0 are connected to V_{REFP2}. The value of the equivalent input voltage V_{IN} is

$$V_{IN} = V_{REFN2} \times 15/16 + V_{REFP2} \times 1/16. \quad (12)$$

After the sampling, the same shift voltage V_S is applied to the bottom plate of C_0, and an A/D conversion is performed again to obtain the second 10-bit digital code value, B_{CAL4}. The digital code values obtained from the two A/D conversions are then compared. The calibration flow chart of reference voltage is shown in Fig.7.

During the calibration, if the selected scaling reference voltage is lower than the ideal value, the voltage values at each step of the lower 5-bit A/D conversion will be smaller than expected, thereby introducing a gain error. This error

may cause the comparator to fail to reach its threshold voltage, leading to an A/D conversion output of zero. In such cases, since both output codes are identical, the calibration process may erroneously conclude that the calibration is complete.

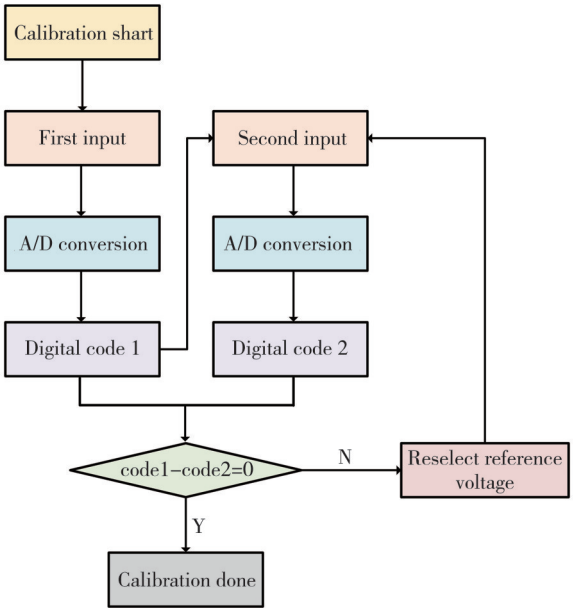
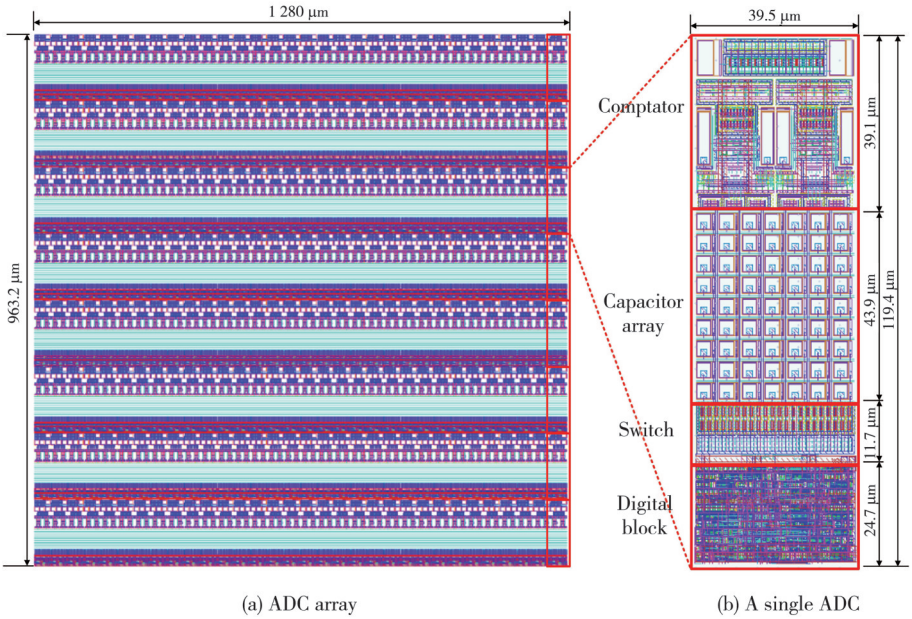


Fig. 7 Flowchart of reference voltage calibration

To avoid this, a slightly larger initial reference voltage should be selected and gradually reduced until the calibration is completed. Since the redundant design can tolerate a certain degree of error, the equality of the digital code values obtained from two calibrations does not indicate that the scaling reference voltage has been accurately calibrated. Therefore, it is essential to adjust the shift voltage and perform multiple calibration steps to enhance the reliability of the calibration process.

4 Simulation

The proposed two-step SAR ADC is designed based on a 55 nm CMOS process, with an analog supply voltage of 2.5 V, a digital supply voltage of 1.2 V, and an input voltage range of 0.8—1.8 V. The simulation was carried out using Cadence tools. First, an ideal sine wave was input. The discrete voltage values were obtained through an A/D conversion. For each cycle, the output voltage was sampled, with the sampling frequency selected according to the corresponding ADC mode. The fast Fourier transform (FFT) spectrum of the output voltage was then analyzed to obtain dynamic parameters such as SNDR and ENOB. Subsequently, an ideal ramp input was applied, and the slope of the ramp was adjusted so that each digital output code of the ADC corresponded to 32 cycles. Similarly, discrete voltage values were obtained and sampled. Static parameters, such as DNL and INL, were calculated based on the differences between the number of output voltage values and the ideal values. The proposed architecture achieves a resolution of 10-bit to 12-bit using only a 5-bit capacitor array, significantly reducing the area occupied by the capacitor array. All capacitors utilize a metal-insulator-metal (MIM) structure with a unit capacitance of 99.19 fF. The area of the column-parallel ADC is 39.5 μm×119.2 μm, with the digital block circuits occupying 20.7% of the total area, the capacitor array and switch array accounting for 46.5%, and the comparator covering the remaining 32.7%. The layout of the ADC is shown in Fig.8.



(a) ADC array (b) A single ADC

Fig. 8 Layout of proposed two-step SAR ADC

A post-simulation analysis was conducted on the circuit before calibration. In the 10-bit/11-bit/12-bit mode, the ADC operates at a sampling frequency of $1.610\times10^6/6.329\times10^5/3.497\times10^5$ per second. A post-simulation analysis of the circuit before calibration was performed. The Fourier transform of the output signal the frequency spectra shown in Fig. 9. The ADC achieves 59.29/63.62/66.82 dB SNDR and 74.09/74.93/85.55 dB SFDR in the 10/11/12-bit modes. Besides, Fig. 10 presents the static performance characteristics of ADC. In three modes, the DNL are +0.83/− 0.50 LSB, +0.88/− 0.59 LSB, and +1.09/− 0.72 LSB, respectively; while the INL are +1.03/− 0.03 LSB, +0.44/− 0.97 LSB, and +1.75/−0.62 LSB, respectively.

After the calibration, the gain error of the reference voltage was improved. The frequency spectra of the output signal after Fourier transform is shown in Fig.11.

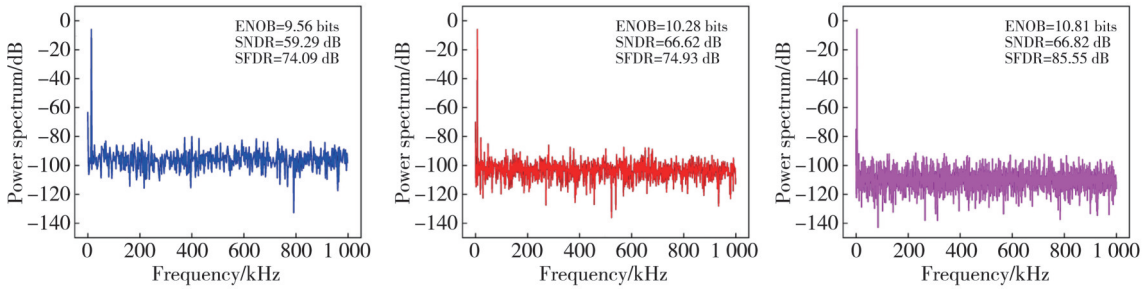


Fig. 9 Output spectra of proposed SAR ADC without calibration

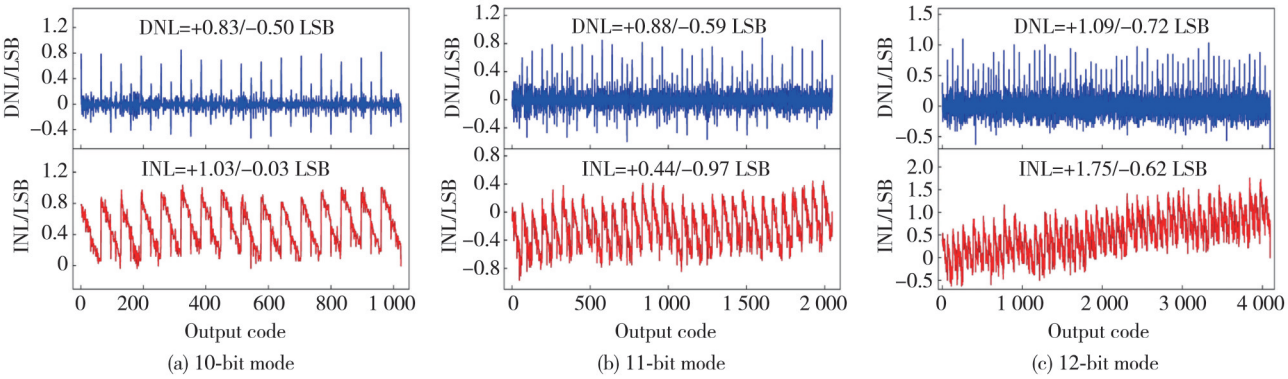


Fig. 10 Static performance of proposed SAR ADC without calibration

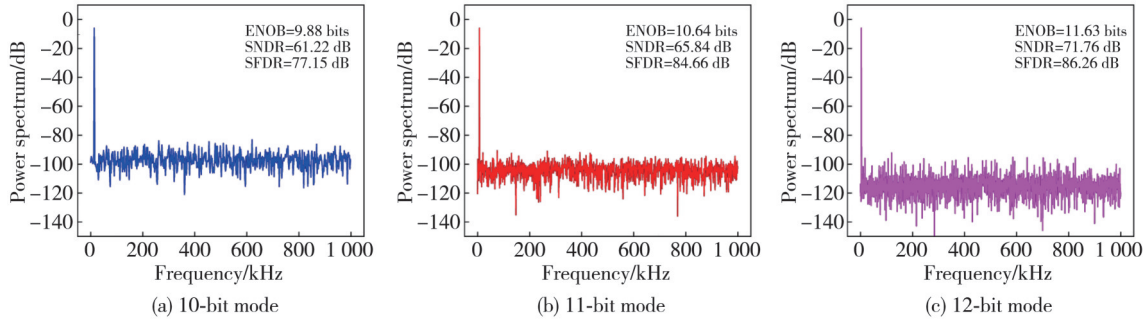


Fig. 11 Output spectra of proposed SAR ADC with calibration

The ADC achieves the 61.22/65.84/71.76 dB SNDR and 77.15/84.66/86.26 dB SFDR in 10/11/12-bit modes. Besides, Fig.12 presents the static performance characteristics of ADC. In three modes, the DNL are +0.22/−0.28 LSB, +0.28/−0.38 LSB, and +0.47/− 0.50 LSB, while the INL are +0.47/− 0.22 LSB, +0.62/− 0.38 LSB, and +0.75/− 0.84 LSB, respectively. The total power consumption of the ADC core in three modes is 59.9/61.2/62.8 μW, respectively.

Table 1 compares the proposed SAR ADC with other column ADCs. Compared to Refs. [12] and [16], the proposed ADC has lower power consumption and superior performance in terms of ENOB and DNL. This work achieves the highest sampling rates in both 10-bit and 11-bit modes, while the sampling rate in the 12-bit mode is slightly lower than that of Ref.[16]. The area of the single-column ADC is only 39.5 μm×119.4 μm, which is significantly smaller than that of other papers in the table,

and the area efficiency is only 1.50 under the premise of 12-bit resolution. The proposed SAR ADC has better area efficiency than the prior SAR ADC designs and realizes a higher resolution with excellent linearity.

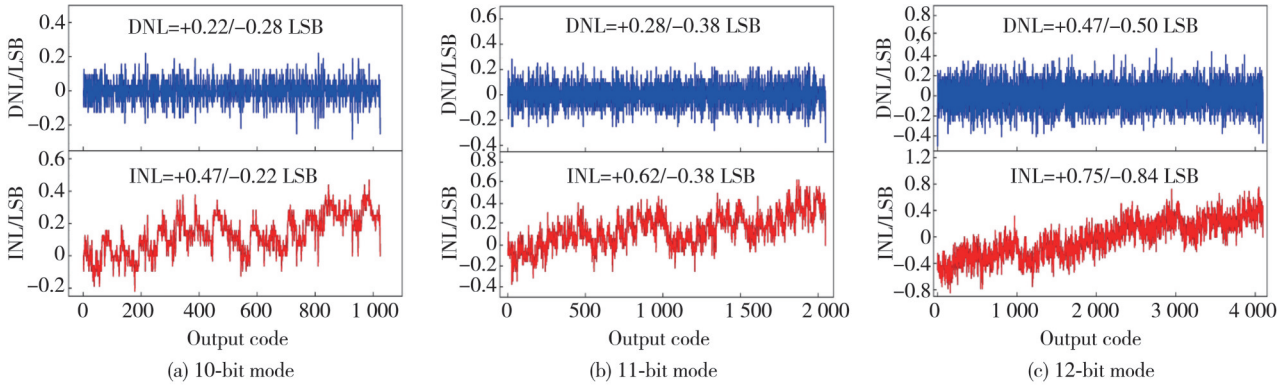


Fig. 12 Static performance of proposed SAR ADC with calibration

Table 1 Summary and comparison of performance

Method	Architecture	Result type	Process/nm	Sampling rate/($\times 10^3$ s^{-1})	DNL /LSB	INL /LSB	Resolution/bits	ENOB/bits	SFDR/dB	Power/μW	Area/μm^2	Area efficiency /(μm^2·code^{-1})
This work	TS SAR	Simulation	55	1612.9	+0.22/−0.28	+0.47/−0.22	10	9.88	77.15	59.9	39.5×119.2	5.43
				632.9	+0.28/−0.38	+0.62/−0.38	11	10.64	84.66	61.2		2.91
				349.7	+0.47/−0.50	+0.75/−0.84	12	11.63	86.26	62.8		1.50
Ref.[2]	SAR	Simulation	180	100	+0.14/−0.12	+0.11/−0.12	8	7.98	67.56	0.81	—	—
				100	+0.09/−0.17	+0.17/−0.15	9	8.95	71.94	0.91		
				100	+0.17/−0.15	+0.25/−0.23	10	9.90	78.41	1.01		
Ref.[6]	SS	Simulation	110	29.9	+0.64/−0.54	+0.04/−6.7	11	—	—	53.7	5×1500	—
Ref.[12]	TS SS	Simulation	130	100	+0.76/−0.80	+10.6/−0.84	12	11.25	78.55	72	7.5×775	2.39
Ref.[16]	SAR/SS	Simulation	180	500	+0.60/−0.50	+0.40/−0.50	12	11.26	81.43	73.15	30×487	5.96
Ref.[19]	TS SAR	Measurement	130	200	+0.87/−0.99	+5.76/−4.37	14	11.65	89.14	57	15×1450	6.77
Ref.[20]	TS SAR	Measurement	130	58.4	+0.99/−0.90	+12.0/−3.9	14	—	—	55.1	11.2×990	—

5 Conclusions

This paper presents a high area-efficiency, resolution-configurable two-step SAR ADC using the PMS method. By adjusting the number of A/D conversions, the proposed ADC can be configured with 10/11/12-bit modes using a 5-bit DAC capacitor array. The resolution can be expanded without increasing the area of the capacitor array and effectively satisfies the shifting requirements of different application scenarios. An error compensation technique is introduced to address the potential reduction in the ADC quantization range caused by the PMS method. Furthermore, a calibration method has been proposed to mitigate the gain error effects by calibrating the scaled reference voltage. The proposed calibration method is suitable for all bottom-plate sampling SAR ADCs. The ADC achieves the 86.26 dB SFDR and 11.63 bits in 12-bit mode. The DNL and INL are +0.47/− 0.50 LSB and +0.75/− 0.84 LSB, respectively. The proposed TS SAR ADC is appropriate for high-speed area-efficient CISs.

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Declaration of conflicting interests

The authors have no conflict of interests related to this publication.

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一种用于CMOS图像传感器的采用伪多重采样和校准的分辨率可重构SAR ADC

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摘　要： 提出了一种用于CMOS图像传感器的采用伪多重采样(Pseudo-multiple sampling, PMS)方法和增益误差校准方法的分辨率可重构逐次逼近模数转换器(Analog-to-digital converter, ADC), 该ADC通过调整A/D转换的次数, 完成了10位、11位、12位三种分辨率的配置, 从而满足用户在不同情况下的需求。PMS方法放宽了对每个ADC的分辨率要求, 从而有效减少了单位电容的数量和电容阵列的面积。同时, 引入了一种补偿方法, 解决了PMS方法易导致ADC量化范围减小的问题。此外, 提出了一种适用于下级板采样的校准方法, 减小了参考电压之间的增益误差, 提高了A/D转换的精度。在55 nm工艺下进行仿真, 结果表明, 所提出的ADC在12位模式下, 采样频率为每秒3.497×10^5, 经过校准后, DNL和INL分别为+0.47/−0.50 LSB和+0.75/−0.84 LSB, 有效位数达到11.63位, 单列ADC所占的面积为39.5 μm×119.2 μm, 功耗为62.8 μW。

关键词： CMOS图像传感器; 可重构模数转换器; 逐次逼近寄存器; 误差校准; 伪多重采样

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