

RESEARCH ARTICLE

Self-aligned TiO_x -based 3D vertical memristor for a high-density synaptic array

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Supporting Information

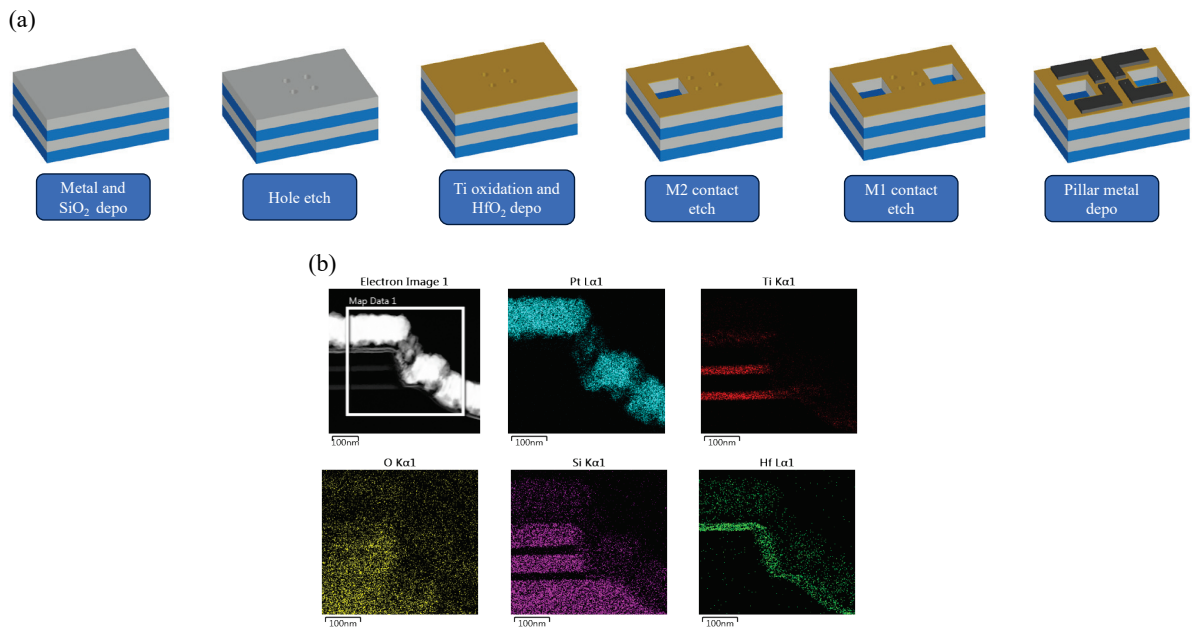


Fig. S1 (a) Fabrication process flow of self-aligned VRRAM. (b) EDS mapping of Pt, Ti, O, Si, and Hf.

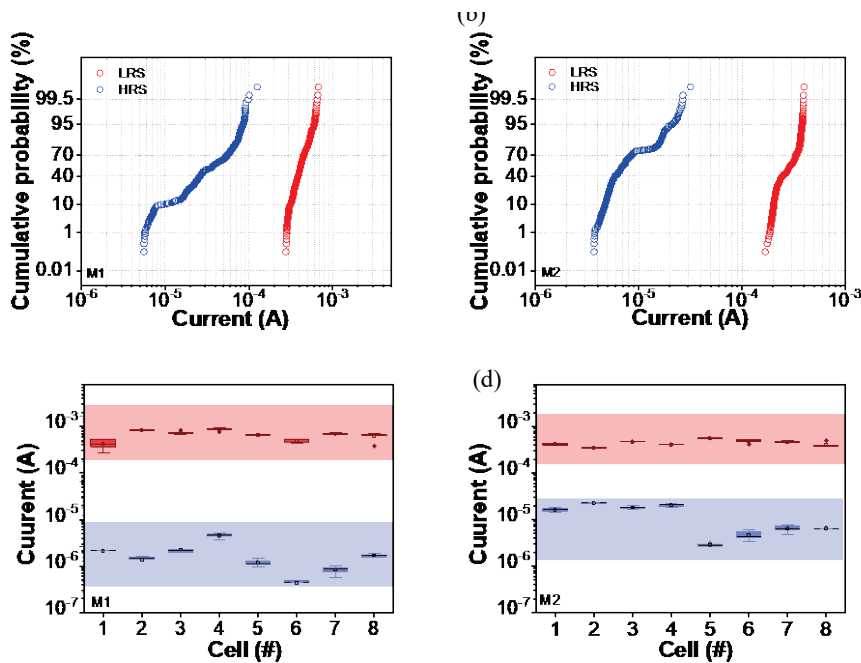


Fig. S2 Cumulative probability function in current levels over 100 cycles (a) on the first floor and (b) on the second floor. Box plot of cell-to-cell variation over 10 cycles (c) on the first floor and (d) on the second floor.

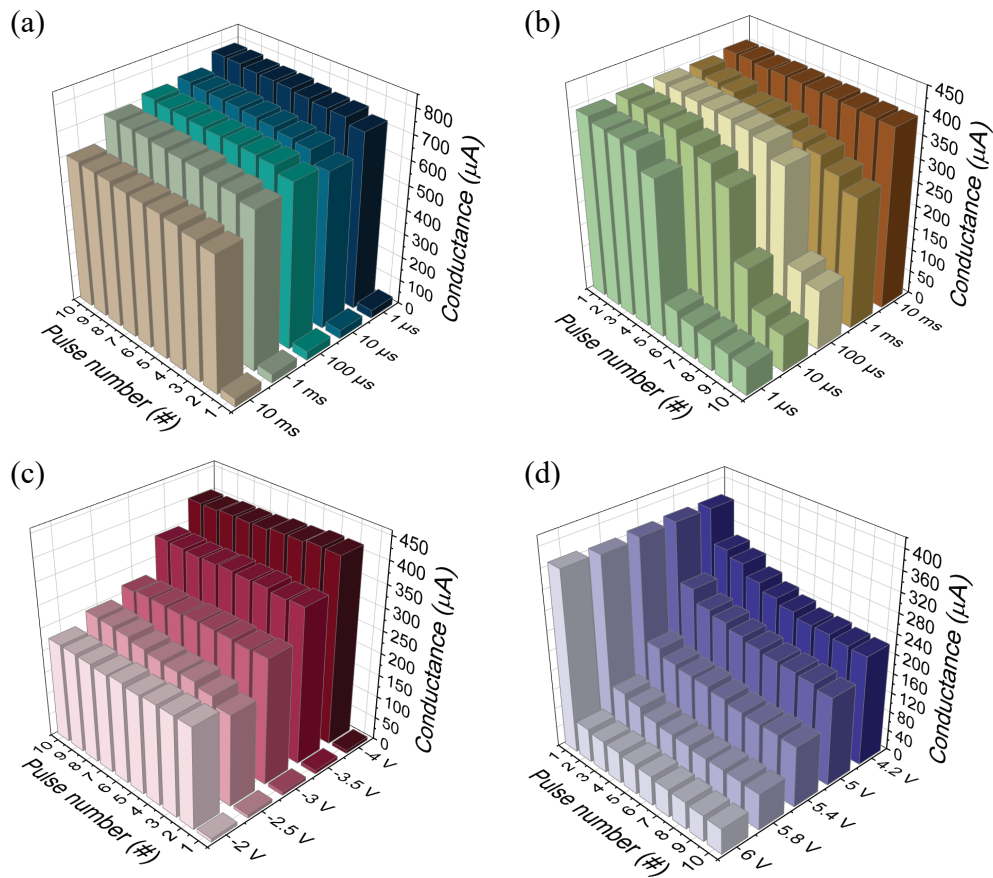


Fig. S3 The conductance response as a function of pulse interval time variation at (a) potentiation and (b) depression. The conductance response as a function of pulse amplitude at (c) potentiation and (d) depression.

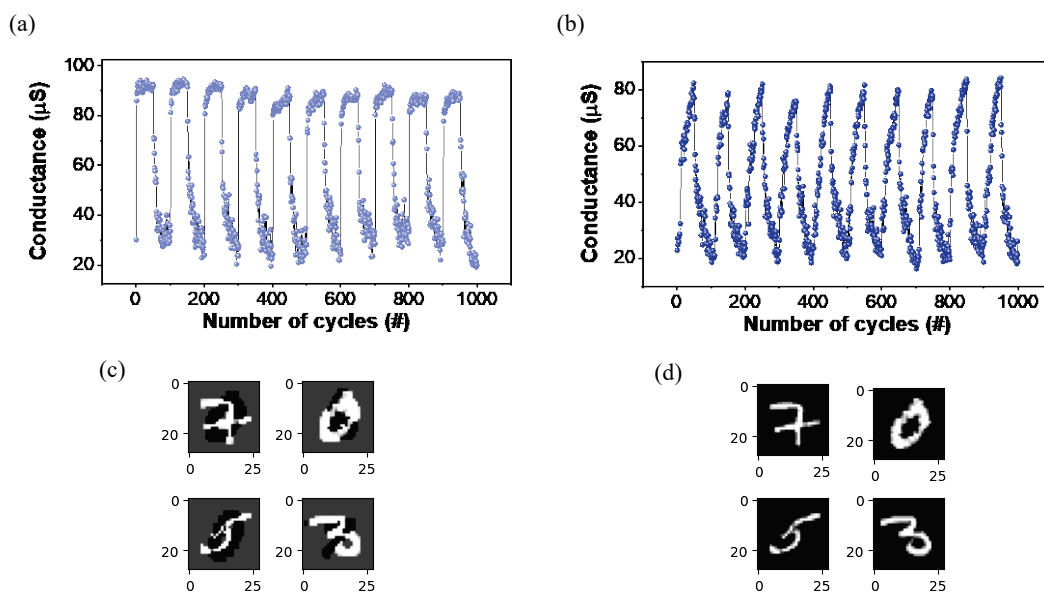


Fig. S4 The result of 10 consecutive potentiation and depression (a) with identical pulse and (b) with incremental pulse modulation. Examples from the MNIST database based on simulations with (c) identical pulse and (d) incremental pulse.