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RESEARCH ARTICLE

# Demonstration and operation of quantum harmonic oscillators in an AlGaAs-GaAs heterostructure

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## Supporting Information

## Methods

### Device fabrication

The devices on $Al_{0.25}Ga_{0.75}As$/GaAs heterostructure wafer were patterned by electron beam lithography in a PMMA/MMA bilayer resist. Thermal evaporation was used after pattern definition to deposit two separate 25 nm thick Al layers. The first Al layer was oxidized in 100 mTorr of oxygen for about 10 minutes to form a thin aluminum oxide layer. Then the second angle evaporation of Al was performed to form the tunnel junctions of the SET by the nanometer scale overlap between the two Al lines. In our devices, the $Al/Al_2O_3/Al$ junction area has a typical size of ~60x60 $nm^2$ achieved by carefully controlling the evaporation angles.

### Device measurements

The electrical measurements were carried out in a $He^3$ refrigerator operating at a base temperature of 300 mK. A home-made 8 channel voltage source provided high-stability voltages to bias the gates during measurements. The currents passing through the SETs were measured by home-made current preamplifiers. All the DC signals were measured using HP3478A multimeters and recorded by LabVIEW programs in the computer.

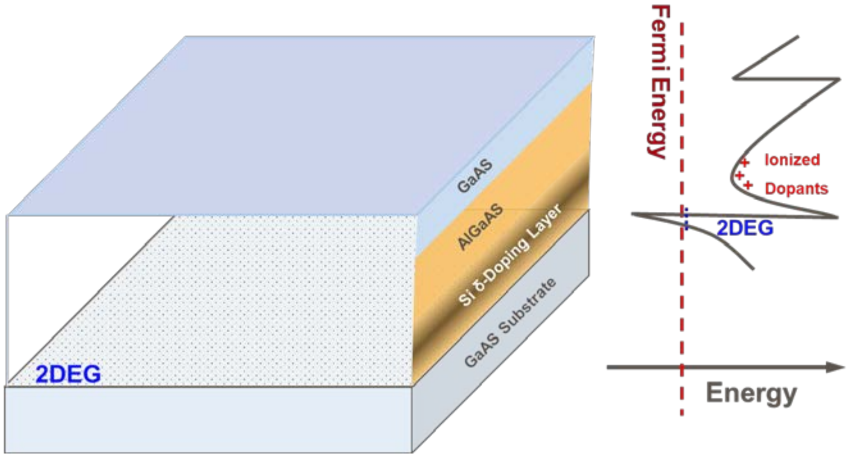

**Fig. S1** Schematic crystal and band structures of an AlGaAs/GaAs 2DEG heterostructure. The AlGaAs/GaAs heterostructure is typically (from bottom to top) composed of an intrinsic GaAs substrate, an AlGaAs barrier layer, a Si δ-doping layer localized in just a few atomic layers which is close to the AlGaAs/GaAs interface, and a thin GaAs cap layer that prevents oxidation of the AlGaAs layer exposed to air/oxygen. A triangular quantum well forms at the AlGaAs/GaAs heterointerface, where 2DEG is populated in the quantum well. The δ-doping Si dopants are used to modulate the carrier density of 2DEG which is confined to quantum well at the AlGaAs/GaAs heterointerface.

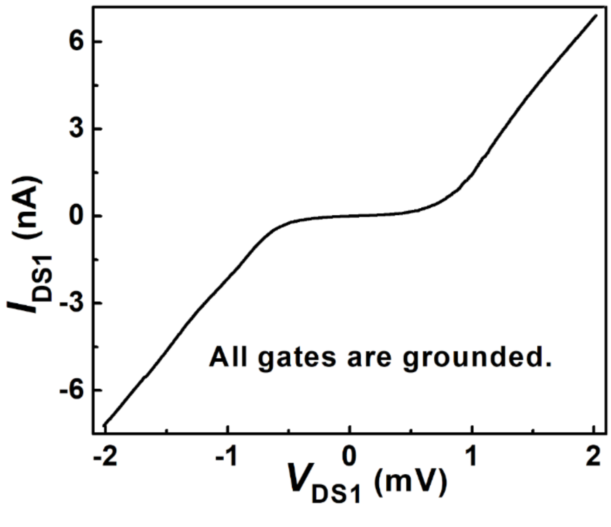

**Fig. S2** *I*-*V* characteristic of the right SET (SET1) as a function of the drain-source bias voltage. The SET demonstrates its Coulomb blockade behavior of a superconducting SET measured at the base temperature of ~300 mK. During this measurement, all the gate electrodes are grounded, so the gate induced charge on SET island is zero. We thus deduce the device parameters from its *I*-*V* characteristic, the total capacitance $C_S \approx 8.9 \times 10^{-16}$ F, the total resistance $R \approx 200.8\ \mathrm{k\Omega}$.