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Quantitative analysis of the transition conditions for the excess noise component of nano-MOSFETs

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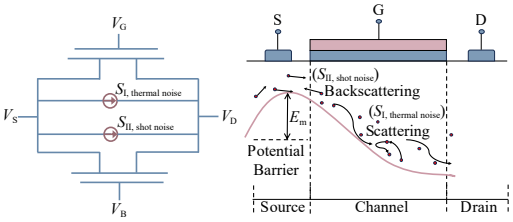
ABSTRACT

In nanoscale metal-oxide-semiconductor field-effect transistors (MOSFETs), excess noise has been experimentally observed as the channel length is scaled down. Theoretical analyses indicate that as the channel length decreases, the dominant component of excess noise gradually changes from modified thermal noise to suppressed shot noise. However, no clear quantitative analysis has been provided regarding the specific conditions for this transition. In this paper, based on a device current model, we analyze the transition conditions under which shot noise replaces thermal noise as the dominant component of excess noise. In the modeling process, we comprehensively consider short-channel effects, including the electric field distribution, mobility reduction caused by electron temperature gradients, and the hot-carrier effect. Meanwhile, we use 3D Monte Carlo simulations to analyze the channel current noise components in MOSFETs with different channel lengths, and we simulate the effects of drain–source voltage, gate voltage, temperature, and substrate doping density on the transition of excess noise components. The simulation results show that the transition trend of excess noise components is consistent with predictions from the physical model: the critical channel length for the transition from thermal noise to shot noise in nanoscale MOSFETs is approximately 20 nm. The model and simulation results presented in this paper agree with reported experimental measurements and provide a theoretical foundation for the quantitative analysis of excess noise components in nanoscale MOSFETs.



Keywords excess noise, thermal noise, shot noise, Monte Carlo simulation, backscattering

1 Introduction

Transistors, as the core components of chips, have smaller gate sizes to achieve higher integration and enhanced performance [1, 2]. With the continuous advancement of semiconductor fabrication processes [3, 4], nano-MOSFETs exhibit excellent low-power characteristics and high unit-gain frequency advantages [5]. However, when the channel length of MOSFET devices is reduced to the nanoscale, the short-channel and parasitic effects of the devices are significantly enhanced, leading to significant excess noise observed in experimental measurements [6]. This not only reduces the efficiency of the devices but also adversely affects their lifetime [7, 8].

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An in-depth understanding of noise characteristics, especially the physical sources of excess noise, is a prerequisite for applying CMOS technology to low-noise RF designs [9]. Regarding the generation mechanism of excess noise, researchers initially attributed it to excess thermal noise and modified the traditional thermal noise model by introducing short channel effects such as hot carrier effect, mobility reduction effect, and channel length modulation effect. However, the modified thermal noise model still cannot reasonably explain the excess noise phenomenon in nanoscale devices when the device channel length is less than 100 nm [10, 11]. Subsequently, experimental measurements have shown that the channel current noise in nanoscale MOSFET devices exhibits shot noise characteristics [7, 12], suggesting that as the channel length of nanoscale MOSFET devices continues to shrink, shot noise will overtake thermal noise as the main component of the excess noise [13]. Therefore, it is necessary to investigate the transition conditions of the excess noise component of nano-MOSFET devices.

Shot noise originates from the randomness of charge carriers crossing potential barriers. In the channel of nano-MOSFETs, the potential barrier is typically located near the source region. Charge carriers from the source randomly cross this barrier and are injected into the channel, which serves as the primary source of shot noise [6]. Meanwhile, whether the carriers injected into the channel can reach the drain region depends on the scattering effects within the channel, whereas the presence of channel resistance leads to the generation of thermal noise [14, 15]. As the channel length decreases, the carrier transport mechanism in nano-MOSFET devices undergoes a significant transformation, gradually shifting from traditional drift-diffusion transport to ballistic or quasi-ballistic transport. This transition in transport mechanism directly affects the components of excess noise in the device [7, 16, 17]. In long-channel devices, the channel resistance is relatively high, and carriers undergo significant scattering during transport. These scattering effects strongly suppress shot noise, making thermal noise the dominant noise source [18]. Therefore, the noise in long-channel devices is typically dominated by thermal noise [19, 20]. However, as the channel length decreases, the influence of the potential barrier on the channel current gradually exceeds that of the channel resistance. The dominant mechanism of the channel current shifts from resistance-limited to barrier-limited, and the effect of the barrier becomes increasingly significant. This transition leads to a gradual shift in the device noise from thermal noise to shot noise [21, 22].

Regarding the transition in the excess noise components of the channel in nano-scale MOSFET devices, existing studies have conducted related physical modeling work. However, these studies are mainly limited to qualitative descriptions and lack quantitative analysis. Moreover, they have not fully considered the various short-channel effects induced by the reduction in device dimensions [23]. Additionally, some studies have predicted the transition conditions of excess noise components in nano-MOSFET devices based on experimental measurements, but they similarly have not established specific quantitative analytical models [6, 24]. The McKelvey flux method can capture the fundamental phenomena of carrier transport in transistors, effectively encompassing the transition from diffusion to ballistic transport [25, 26]. Therefore, in this study, the McKelvey flux method, combined with short-channel effects, is employed to establish a model for the transition of excess noise components in small-sized, nanoscale-channel-length MOSFET devices. The conditions for the transition from thermal noise to shot noise are analyzed in detail. Additionally, a three-dimensional Monte Carlo simulation [27–29] is employed to validate the channel current noise of MOSFET devices with different channel lengths. The power spectral densities of various noise parameters, including channel current noise, total shot noise, and thermal noise, are extracted from the simulation output of current fluctuations. The variations of the excess channel noise components with respect to gate voltage, drain-source voltage, substrate doping density, and temperature are further calculated and analyzed. The trend of excess noise transition in the Monte Carlo simulation results shows good consistency with the theoretical analysis. These findings provide important references for device reliability analysis and characterization.

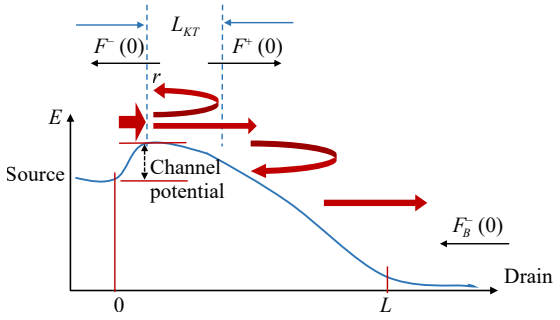

Fig. 1 A simple flux representation of channel carrier transport in nano-scale MOSFETs and a schematic of reverse scattering.

2 Transformation model

The McKelvey flux method [25] decomposes the current into forward and reverse directional fluxes. Figure 1 shows the directional fluxes of the MOSFET. $F^+(0)$ represents the forward flux injected from the source. $F^-(0)$ represents the negative carrier flux under scattering conditions, which consists of two components: the first component is the reverse scattering part of the flux injected from the source into the channel, and the

second component is the negative carrier current flowing from the drain region to the source. The drain-injected flux is represented in Fig. 1 as $F_B^-(0)$.

Based on the directional carrier flux, the drain-source current can be expressed as

$$I_{\mathrm{DS}} = Wq\left[F^+(0) - F^-(0)\right], \tag{1}$$

where W is the device width. The backscattering coefficient r is introduced to describe $F^-(0)$. The backscattering coefficient r is defined as the ratio of the number of carriers scattered back into the injection region to the number of carriers injected [30, 31]. Based on the backscattering coefficient r, $F^-(0)$ can be expressed as

$$F^-(0) = rF^+(0) + (1-r)F_B^-(0), \tag{2}$$

$$F_B^-(0) = F^+(0)\exp\left(-\frac{qV_{\mathrm{DS}}}{kT}\right). \tag{3}$$

The number of carriers at the top of the potential barrier can be expressed as

$$Q(0) = q\frac{F^+(0) + F^-(0)}{v_{\mathrm{inj}}}, \tag{4}$$

where v_{inj} represents the emission velocity at the contact region. By combining Eq. (1) and Eq. (4), we obtain

$$I_{\mathrm{DS}} = WQ(0)\,v_{\mathrm{inj}}\frac{1 - F^-(0)/F^+(0)}{1 + F^-(0)/F^+(0)}. \tag{5}$$

Substituting Eq. (2) and Eq. (3) into Eq. (5), the transport current of the nano-MOSFET under non-degenerate conditions can be obtained,

$$I_{\mathrm{DS}} = WQ(0)\,v_{\mathrm{inj}}\left(\frac{1-r}{1+r}\right)\frac{1 - \exp\left(-\frac{qV_{\mathrm{DS}}}{kT}\right)}{1 + \left(\frac{1-r}{1+r}\right)\exp\left(-\frac{qV_{\mathrm{DS}}}{kT}\right)}. \tag{6}$$

For a well-designed MOSFET, the total carrier concentration at the channel inversion layer potential barrier is approximately determined solely by the gate voltage, i.e., $Q(0) \approx C_{\mathrm{OX}}(V_{\mathrm{GS}} - V_{\mathrm{TH}})$, where C_{OX} represents the MOSFET oxide capacitance, V_{GS} is the gate-source voltage, and V_{TH} is the threshold voltage. When the drain-source voltage $V_{\mathrm{DS}} \gg kT/q$, Eq. (6) can be simplified as

$$I_{\mathrm{DS}} = C_{\mathrm{OX}}Wv_{\mathrm{inj}}\left(\frac{1-r}{1+r}\right)(V_{\mathrm{GS}} - V_{\mathrm{TH}}). \tag{7}$$

The backscattering coefficient r can be analytically calculated using the kT-layer model [26]:

$$r = \frac{L_{KT}}{L_{KT} + \lambda_0}. \tag{8}$$

As shown in Fig. 1, L_{KT} represents the kT-layer length, which represents the distance from the top of the channel barrier to the point where the drain region potential drops by kT/q. Within the kT-layer length, carriers from the source region that cross the channel barrier top may be scattered back to the source region. After carriers have traveled through the kT-layer length, the probability of returning to the source region can be neglected. According to the definition of L_{KT}, $L_{KT} = (kT/q)/\varepsilon(0^+)$, where $\varepsilon(0^+)$ represents the average electric field strength in the kT-layer [32]. λ_0 is the mean free path of carriers in the inversion layer, and $\lambda_0 = 2kT\mu_0/(qv_{\mathrm{inv}})$, where μ_0 is the low-field mobility and v_{inv} is the average random thermal velocity of the carriers in the inversion layer. Substituting Eq. (8) into Eq. (7) gives

$$I_{\mathrm{DS}} = \frac{C_{\mathrm{OX}}W(V_{\mathrm{GS}} - V_{\mathrm{TH}})}{\frac{1}{v_{\mathrm{inj}}} + \frac{1}{\mu_0\varepsilon(0^+)}\frac{v_{\mathrm{inv}}}{v_{\mathrm{inj}}}}. \tag{9}$$

Eq. (9) represents the channel current of the nano-MOSFET as consisting of two components of velocity: one is the carrier emission velocity v_{inj}, representing ballistic transport, and the other is the traditional drift velocity $\mu_0\varepsilon(0^+)v_{\mathrm{inj}}/v_{\mathrm{inv}}$, representing conventional drift-diffusion transport. Therefore, Eq. (9) is applicable to the entire range from drift-diffusion to ballistic transport. By analyzing the two components of velocity, the transition of the channel current noise mechanism in nano-MOSFET devices can be explored.

When the size of the MOSFET device decreases to below 90 nm, short-channel effects significantly impact the device's performance, leading to more noise. Therefore, in this paper, the mobility expression resulting from the mobility degradation effect is introduced,

$$\mu_n = \frac{\mu_{n0}}{\sqrt{1 + \frac{\mu_{n0}qE_y^2}{d}\left[1 - \exp\left(-p \times y\right)\right]}}, \tag{10}$$

where $(d = 10^{-8}W)$ represents the energy relaxation parameter, Eq. (10) can be used to calculate the mobility of each point in the channel. This expression includes the mobility reduction effect influenced by longitudinal electric field, transverse electric field, and electron temperature gradient. Among them [15],

$$\mu_{n0} = \frac{\mu_0}{1 + \theta_1 V_{\mathrm{GT}} + \left[\sqrt{\frac{\theta_2}{L_{\mathrm{eff}}}} - \theta_1(1 - 0.5\alpha)\right]V_{\mathrm{DS}}}, \tag{11}$$

$$p = \frac{2d}{3K\mu_{n0}T_0E_y}, \tag{12}$$

$$V_{\mathrm{GT}} = V_{\mathrm{GS}} - V_{\mathrm{TH}} = V_{\mathrm{GS}} - (V_{\mathrm{TH0}} - \sigma V_{\mathrm{DS}}), \tag{13}$$

where μ_0 is the low-field mobility, θ_1 and θ_2 are fitting

parameters, α is the body factor term, $T_0 = 300$ K, V_{TH0} represents the threshold voltage of the MOSFET device, and σ is the factor for drain-induced barrier lowering (DIBL) effect. E_y is the transverse electric field in the channel,

$$E_y = \frac{1}{\frac{1}{E_C} + \frac{1}{V_{DSAT}} 2L_{elec}\sqrt{1 - \frac{y}{L_{elec}}}}. \tag{14}$$

Here, E_C is the critical electric field, and $E_C = 2v_{sat}/\mu_{n0}$. $v_{sat} = 1.0 \times 10^5$ m·s^{-1}. L_{elec} is the electrical channel length: $L_{elec} = L_{eff} - \Delta L$. The saturation voltage V_{DSAT} of the MOSFET device is given by the following Eq. (15) [16]:

$$V_{DSAT} = \frac{2V_{GT}}{1 + \sqrt{1 + \frac{2V_{GT}}{\alpha L_{eff} E_C}}}, \tag{15}$$

where ΔL is the channel length variation induced by the channel length modulation effect, which can be expressed as

$$\Delta L = l \ln\left(\frac{V_{DS} - V_{DSAT}}{lE_C} + \frac{E_D}{E_C}\right), \tag{16}$$

$$E_D = \sqrt{\left(\frac{V_{DS} - V_{DSAT}}{l}\right)^2 + E_C^2}, \tag{17}$$

$$l = \frac{1}{\lambda}\sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{OX}} t_{OX} X_j}, \tag{18}$$

where ε_{Si} is the dielectric constant of silicon, ε_{OX} is the dielectric constant of the oxide layer, t_{OX} is the gate oxide thickness, X_j is the source/drain junction depth, and $\lambda = 5.23$ is the fitting parameter used to calculate the channel length modulation effect. Subsequently, by substituting the effective mobility expression Eq. (10) into Eq. (9), the current expression incorporating various short-channel effects is obtained,

$$I_{DS} = \frac{C_{OX} W (V_{GS} - V_{TH})}{\frac{1}{v_{inj}} + \frac{1}{\mu_n \varepsilon(0^+)} \frac{v_{inv}}{v_{inj}}}, \tag{19}$$

where v_{inj} is the injection velocity of carriers emitted from the contact region into the channel, which is generally expressed as [26, 32]

$$v_{inj} = v_T^{3D} = v_T \frac{F_1(\eta_F)}{F_{1/2}(\eta_F)}, \tag{20}$$

where $v_T = \sqrt{(2KT)/(\pi m_t)}$ is the random thermal velocity of carriers. F_j denotes the j-th order Fermi–Dirac integral, and $\eta_F = (E_F - E_C)/(KT)$ is the carrier degeneracy factor. Meanwhile, the average random thermal velocity of carriers in the inversion layer is expressed as [33]

$$v_{inv} = v_T^{2D} = \sqrt{\frac{\pi KT}{2m^*}}, \tag{21}$$

where m^* is the effective mass of the electron. From Eq. (19), it can be seen that the channel current in a nanoscale MOSFET consists of two velocity components: one is the carrier injection velocity v_{inj}, representing ballistic transport; the other is the conventional drift velocity $\mu_n \varepsilon(0^+) v_{inj}/v_{inv}$, representing conventional drift-diffusion transport. These two components are in parallel, and the current behavior depends on the smaller of the two. That is, when $v_{inj} < \mu_n \varepsilon(0^+) v_{inj}/v_{inv}$, v_{inj} plays the dominant role in Eq. (19), and the carrier transport mechanism of the device is closer to ballistic transport. Conversely, when $v_{inj} > \mu_n \varepsilon(0^+) v_{inj}/v_{inv}$, the conventional drift-diffusion velocity plays the dominant role, and the carrier transport behaves more like conventional drift-diffusion transport. These two transport mechanisms lead to different types of noise: barrier-limited carrier injection results in shot noise, whereas scattering in drift-diffusion transport induces thermal noise. Therefore, both types of noise coexist in nano-MOSFET devices, and the dominant noise type depends on the carrier transport mechanism in the device.

According to Eq. (19), the condition for the dominant component of excess channel current noise in nanoscale MOSFET devices to transition from thermal noise to shot noise can be expressed as

$$v_{inj} < \mu_n \varepsilon(0^+) \frac{v_{inj}}{v_{inv}}. \tag{22}$$

Substituting Eq. (20) and (21) into Eq. (22) yields

$$1 < \mu_n \varepsilon(0^+) \sqrt{\frac{2m^*}{\pi KT}}. \tag{23}$$

Using the description of the electric field intensity from Ref. [26]:

$$\varepsilon(0^+) = \frac{kT/q}{L_G [kT/(qV_{DS})]^\beta}, \tag{24}$$

where L_G is the channel length, and β is the fitting parameter, $0 < \beta < 1$. Substituting Eq. (24) into Eq. (23) yields

$$L_G < \mu_n \frac{kT/q}{[kT/(qV_{DS})]^\beta} \sqrt{\frac{2m^*}{\pi KT}}. \tag{25}$$

From Eq. (25), it can be clearly observed that the critical channel length for the transition from thermal noise to shot noise is directly proportional to the drain-source voltage and inversely proportional to temperature. To further investigate its transition conditions in relation to the gate voltage and doping concentration, the expression for the average random thermal velocity of inversion layer carriers from Ref. [26] is adopted,

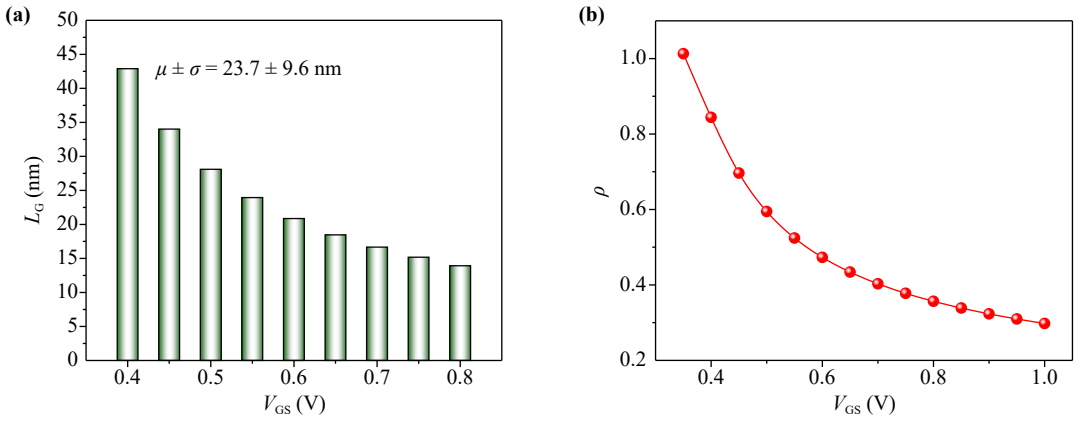

Fig. 2 The relationship between the critical channel length for excess noise component transition and gate voltage in nanoscale MOSFETs. **(a)** Variation of the critical channel length L_G with gate voltage V_{GS}. **(b)** Curve of ρ as a function of V_{GS}.

$$v_{inv} = v_T^{2D} = v_T \frac{F_{1/2}(\eta_F)}{F_0(\eta_F)}. \tag{26}$$

The influence of gate voltage and substrate doping is incorporated in the carrier degeneracy η_F of this expression. Substituting Eq. (26) and the electric field intensity expression (24) into (22) yields

$$L_G < \mu_n \left\{ \rho \frac{kT/q}{v_T [kT/(qV_{DS})]^{\beta}} \right\}, \tag{27}$$

where $\rho = F_0(\eta_F)/F_{1/2}(\eta_F)$.

3 Transition condition analysis

It can be seen from Eqs. (25) and (27) that, under certain bias conditions, a reduction in channel length will cause the inequality condition to hold, thereby satisfying the critical conditions for the transition. The dominant component of MOSFET excess noise will gradually shift from thermal noise to shot noise. The shortening of the channel length reduces the number of inelastic scattering events and weakens space-charge effects [34]. The reduction in inelastic scattering and the weakening of space-charge effects lessen the suppression of shot noise by long-range Coulomb interactions, causing the device transport characteristics to shift from conventional drift-diffusion transport to ballistic transport. As a result, shot noise becomes the dominant component of excess noise, surpassing thermal noise. Additionally, increased mobility also makes the equation valid. Mobility is determined by the scattering mechanism with the highest scattering rate [35]. In phonon scattering, the acoustic phonon scattering probability is greater than the optical phonon scattering probability, while the scattering probability between carriers is much smaller than the two phonon scattering probabilities [36]. With increasing temperature, all three types of scattering increase. At low temperatures, the concentration of thermally excited carriers is low, their mean free path is large, and the scattering probability is small. Therefore, mobility is relatively high. As the temperature increases, the carrier concentration is enhanced, scattering becomes more frequent, and mobility consequently decreases. Therefore, either lowering the operating temperature or using high-mobility materials for the channel will make it easier for the dominant component of excess noise in MOSFET devices to become shot noise.

According to Eq. (27), Fig. 2 illustrates the transition of excess noise components in nanoscale MOSFET devices as a function of gate voltage. Figure 2(a) shows that the critical channel length at which shot noise becomes the dominant component of excess noise in MOSFET devices is around 20 nm. The statistical mean of this dataset is $\mu = 23.7$ nm, with a standard deviation of $\sigma = 9.6$ nm. The relatively large standard deviation clearly reflects the significant influence of gate voltage on the critical channel length. Figure 2(b) shows that ρ exhibits an inverse relationship with the gate voltage V_{GS}, where $\eta_F = (E_F - E_C)/(KT)$ represents the carrier degeneracy, E_F is the Fermi level at the contact, and E_C is the barrier height. The channel barrier height E_C decreases as the gate voltage increases, meaning that η_F is an increasing function of V_{GS}. Consequently, ρ is a decreasing function of the gate voltage V_{GS}. As shown in Fig. 2(a), with the increase in gate voltage, the right-hand side of (27) gradually decreases. This indicates that the critical channel length at which the dominant excess noise component transitions from thermal noise to shot noise decreases as the gate voltage increases. In other words, a higher gate voltage makes it more difficult for shot noise to become the dominant component of excess noise. This phenomenon occurs because, as the gate voltage increases, the enhanced longitudinal electric field leads to more surface scattering for carriers, necessitating a shorter channel length to mitigate the scattering

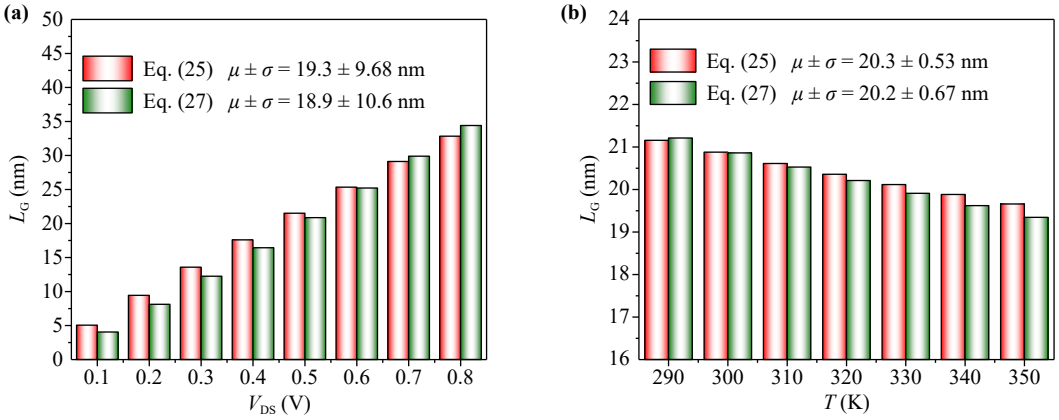

Fig. 3 **(a)** The relationship between the critical channel length L_G for excess noise component transition and the drain-source voltage V_{DS}. **(b)** The relationship between temperature T and the critical channel length L_G for the transition of excess noise components in the channel current of nanoscale MOSFET devices.

effects. Additionally, an increase in gate voltage has two effects: first, it increases the frequency of inelastic scattering, strengthening the Coulomb interaction that suppresses shot noise [37]; second, it enhances carrier degeneracy, reinforcing Pauli exclusion principle suppression, making shot noise less likely to become the dominant component of excess noise [38]. Experimental results confirm that increasing the gate voltage enhances shot noise suppression [12].

Figure 3(a) illustrates the relationship between the excess noise component transition and the drain-source voltage in nanoscale MOSFETs. The red bars represent the results calculated using Eq. (25), with statistical data of $\mu \pm \sigma = 19.3 \pm 9.68$ nm, while the green bars represent the results calculated using Eq. (27), with statistical data of $\mu \pm \sigma = 18.9 \pm 10.6$ nm. Both expressions indicate that, as the drain-source voltage increases, the value on the right-hand side of the transition condition for the excess noise component rises steadily. For devices with different channel lengths, a higher drain-source voltage results in a longer critical channel length where shot noise becomes the dominant excess noise component. For devices in which the channel length is fixed, when the drain-source voltage exceeds a certain critical value, Eqs. (25) and (27) hold true, and shot noise becomes the primary component of excess noise. The experiment in [12] also observed this phenomenon. As the drain-source voltage increases, the kT-layer length shortens [26], leading to a reduction in the backscattering coefficient and a transition toward ballistic transport [21, 22]. At low drain-source voltages, the electric field is weak, and carrier transport is closer to conventional drift-diffusion transport, making the noise resemble equilibrium thermal noise. At high drain-source voltages, the electric field is significantly enhanced, carrier velocity increases rapidly, scattering is reduced, and transport approaches ballistic conduction, with shot noise becoming the dominant component.

Figure 3(b) illustrates the relationship between temperature and the transition of excess noise components in nanoscale MOSFET devices. As shown in the figure, with increasing temperature, the critical channel length at which shot noise becomes the dominant component of excess noise gradually decreases. This indicates that at higher temperatures, shot noise is less likely to be the primary component of excess noise. The red bars represent the results calculated using Eq. (25), with a statistical result of $\mu \pm \sigma = 20.3 \pm 0.53$ nm, and the green bars represent the results calculated using Eq. (27), with $\mu \pm \sigma = 20.2 \pm 0.67$ nm under these conditions. The relatively smaller value of σ indicates that, within the normal range of operating temperature fluctuations, T is a secondary factor affecting L_G. In modern MOS devices, the main scattering mechanisms affecting carriers in the channel are acoustic phonon scattering and optical phonon scattering, both of which decrease in probability as temperature decreases [13]. In the low-temperature region, as the temperature increases, the average velocity of carrier thermal motion increases [36], enabling carriers to skim over the impurity ions faster with smaller deflection angles, making carriers less likely to be scattered. Thus, in the low-temperature region, the suppression of shot noise by the Coulomb effect is weak, and the channel excess noise is primarily governed by shot noise. As the temperature continues to rise, the primary scattering mechanism in the device becomes acoustic wave scattering, which is directly proportional to temperature. The increased frequency of phonon scattering leads to a stronger suppression of shot noise and a decrease in mobility, causing thermal noise to increases with rising temperature. Therefore, at lower temperatures, the transition from thermal noise to shot noise occurs more easily, resulting in a higher proportion of shot noise in the total current noise.

Figure 4 illustrates the transition of excess noise components in nanoscale MOSFETs with substrate

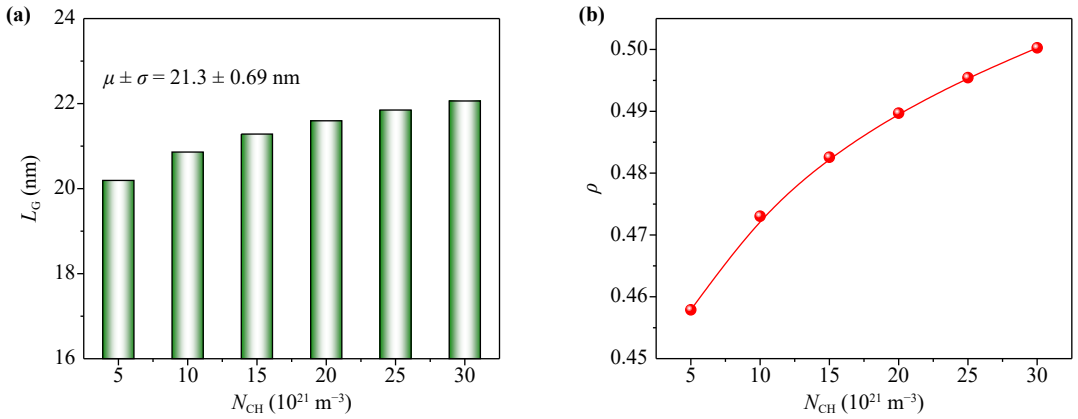

Fig. 4 Relationship between substrate doping density N_{CH} and the critical channel length L_G for the transition of excess noise components in the channel current of nanoscale MOSFET devices: **(a)** Variation of the critical channel length L_G with N_{CH}. **(b)** Curve of ρ as a function of N_{CH}.

doping density. An increase in substrate doping density raises the barrier height E_C, leading to a decrease in η_F. As shown in Fig. 4(b), ρ is positively correlated with the substrate doping density N_{CH}. As N_{CH} increases, the Fermi potential $\psi_{FP} = \frac{kT}{q} \ln \frac{N_A}{n_i}$ gradually increases. N_A indicates the substrates doping concentration, and n_i denotes the concentration of intrinsic carriers. When the surface of the channel region reaches strong inversion, the energy band bending must be equal to or greater than twice the Fermi potential, i.e., $U_S = 2\psi_{FP}$. This means that as the substrate doping density increases, the threshold voltage of the MOSFET also increases. The total carrier charge at the potential barrier peak in the channel inversion layer of the MOSFET is approximately $Q(0) \approx C_{OX}(V_{GS} - V_{TH})$. For a fixed gate voltage, an increase in substrate doping density reduces the number of carriers in the channel inversion layer. As shown in Fig. 4(a), with increasing substrate doping density, the critical channel length at which shot noise becomes the dominant component of excess noise gradually increases, with statistical parameters of $\mu \pm \sigma = 21.3 \pm 0.69$ nm. The reduction in carriers in the channel inversion layer weakens carrier scattering, which in turn reduces shot noise suppression and makes shot noise gradually surpass thermal noise, becoming the primary component of excess noise in the device.

A statistical analysis of Figs. 2 to 4 reveals that, although the trends and magnitudes of the effects of different operating conditions (V_{GS}, V_{DS}, T) and process parameters (N_{CH}) on the critical channel length vary, their statistical mean values all fall within a narrow range of 19.8 nm to 23.7 nm. Furthermore, the fluctuation range of L_G (defined by $\mu \pm \sigma$) under all conditions broadly covers the range of about 15 nm to 33 nm. This analysis indicates that, for the nanoscale-channel-length MOSFETs focused on in this study, the critical scale for the transition of the dominant transport mechanism is not a fixed process node value, but rather a dynamic range modulated by multiple factors. For typical process and operating conditions (V_{DS}/V_{GS} = 0.5–0.7 V, N_{CH} = 5×10^{21}–3×10^{22} m^{-3}, T = 290–350 K), the critical channel length for the transition of the main excess noise component is dynamically distributed in the range of 18 nm to 24 nm. This represents the characteristic length at which this physical transition is most likely to occur under typical design and operating conditions.

4 Monte Carlo simulation

A three-dimensional Monte Carlo simulation flow is established based on the structural characteristics of nanoscale MOSFET devices, and the channel current noise for different channel lengths is extracted. As shown in Fig. 5, as the channel length decreases, the channel current noise of the nanoscale MOSFET device gradually deviates from thermal noise and approaches full shot noise near a channel length of 20 nm. This is

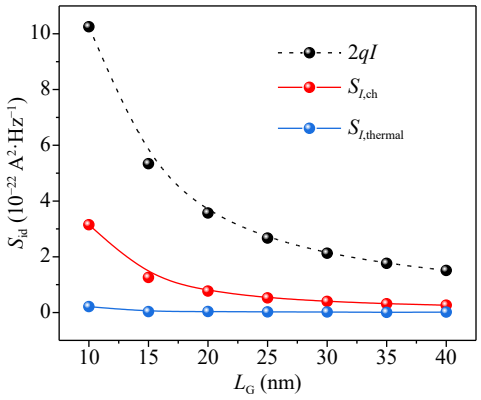

Fig. 5 Relationship diagram of total shot noise ($2qI$), channel current noise ($S_{I,ch}$) and thermal noise ($S_{I,thermal}$) with channel length L_G.

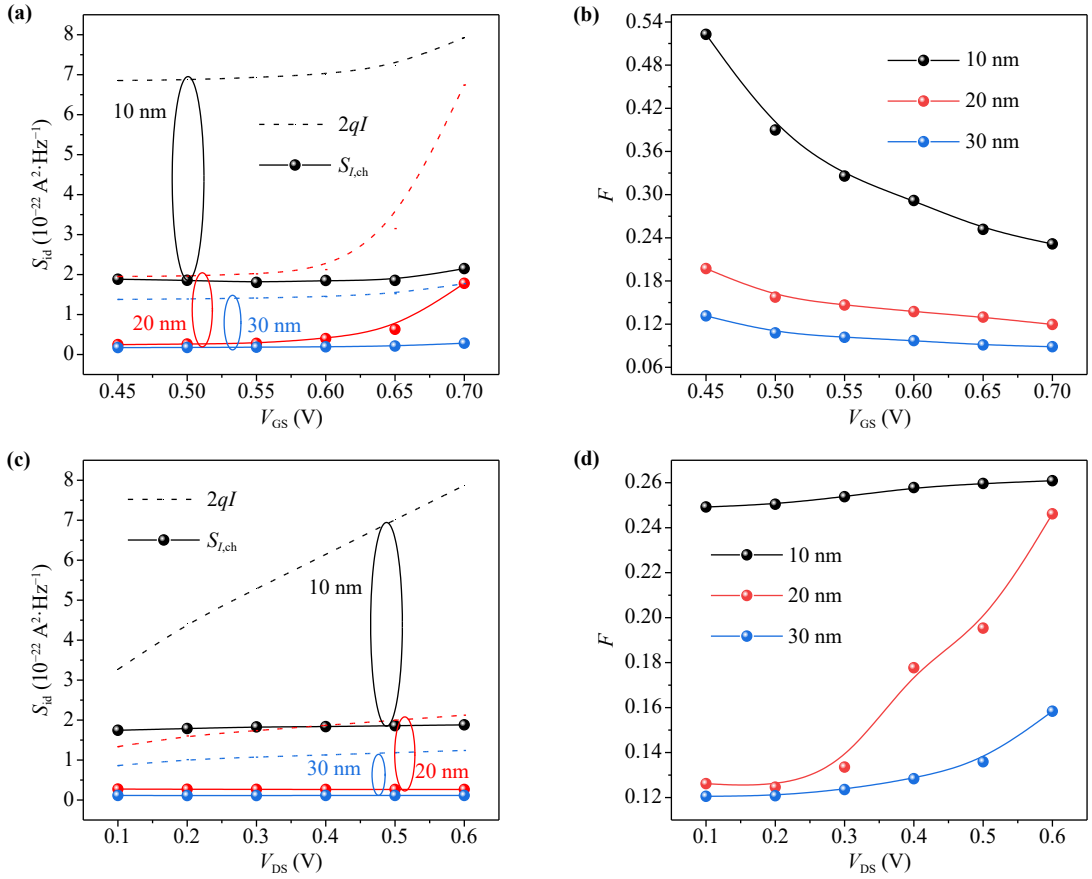

Fig. 6 **(a)** Variation of total shot noise ($2qI$) and channel current noise ($S_{I,\mathrm{ch}}$) with gate voltage. **(b)** Variation of shot noise suppression factor with gate voltage. **(c)** Variation of total shot noise ($2qI$) and channel current noise ($S_{I,\mathrm{ch}}$) with drain-source voltage. **(d)** Variation of shot noise suppression factor with drain-source voltage.

consistent with the physical model and is also in close agreement with the experimental trends reported in Ref. [12] regarding how various types of noise vary with channel length. As the channel length shortens, carrier transport transitions from conventional drift-diffusion transport to ballistic transport. Subsequently, the noise for channel lengths of 10 nm, 20 nm, and 30 nm is analyzed through simulations with different bias parameters. In the simulations, the oxide layer thickness is set to 1 nm, and the channel thickness is set to 3 nm. The source-drain regions are modeled as ideal isotropic n-type silicon, with a doping concentration of 2×10^{20} cm^{-3}. The channel region utilizes low-doped p-type silicon, with the doping concentration treated as a simulation variable. As the simulation region is primarily focused on the channel inversion layer, a dense mesh is applied to the channel region, employing a three-dimensional grid structure of $120 \times 50 \times 1$. Furthermore, to accurately capture the rapid dynamic changes of carriers at the nanoscale, the simulation time step Δt is set to 1 fs. The number of supercarriers selected for the simulation is 10 000. The band structure employed a modified non-parabolic band structure.

Figure 6 illustrates the variation of channel current noise components with bias voltage. Figure 6(a) shows that as the gate voltage increases, the channel current noise gradually rises. This phenomenon occurs because a higher gate voltage drives the channel into a strong inversion state, enhancing the longitudinal electric field and increasing the carrier density. This leads to more scattering and a slight increase in thermal noise. Meanwhile, the channel current noise moves away from the total shot noise level, meaning that shot noise is more suppressed as the gate voltage increases. As a result, at higher gate voltages, shot noise is less likely to be the main part of the excess noise in the channel. Figure 6(b) shows how the shot noise suppression factor changes with gate voltage. As the gate voltage increases, the suppression factor decreases slightly, meaning that a higher gate voltage further suppresses shot noise, reducing its contribution to excess noise.

Figure 6(c) shows how the channel current noise components change with the drain-source voltage. As the drain-source voltage increases, the channel current noise rises slightly, but the change is small. Meanwhile, the total shot noise component increases. Figure 6(d)

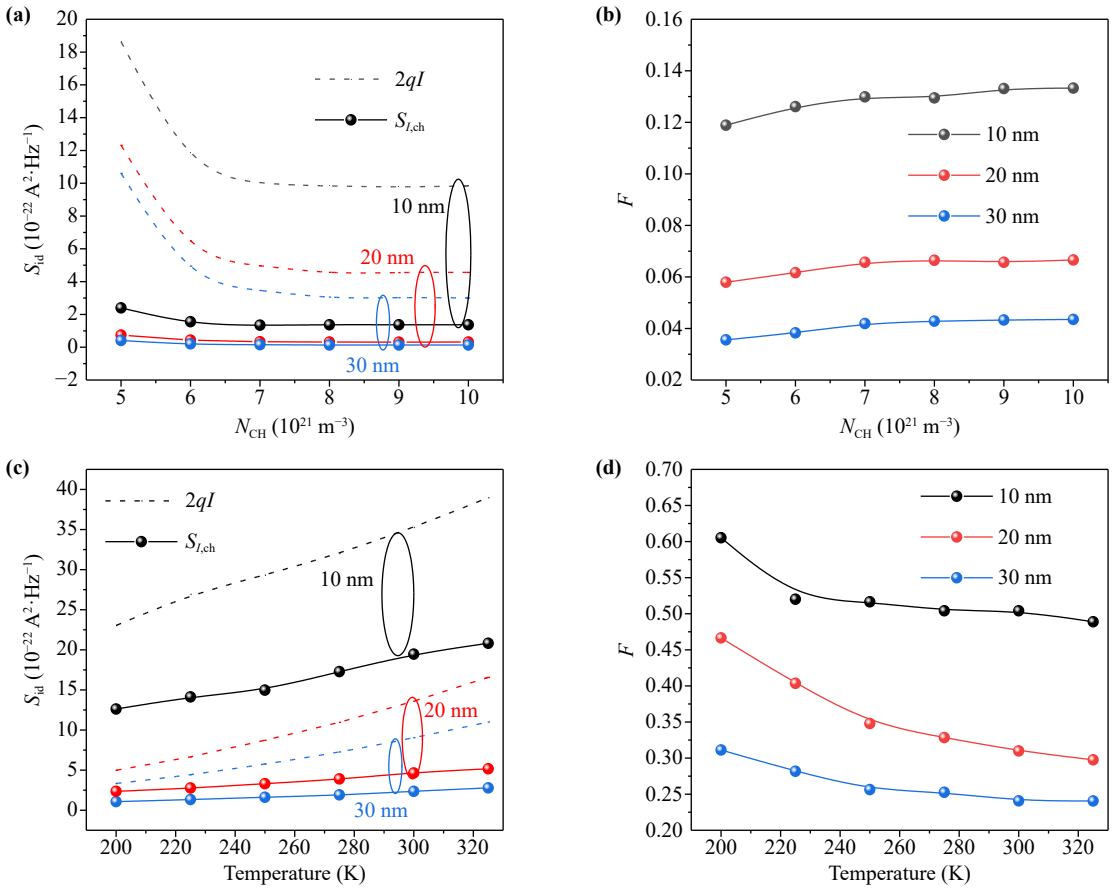

Fig. 7 **(a)** Variation of total shot noise ($2qI$) and channel current noise ($S_{I,\mathrm{ch}}$) with substrate doping density. **(b)** Variation of shot noise suppression factor with substrate doping density. **(c)** Variation of total shot noise ($2qI$) and channel current noise ($S_{I,\mathrm{ch}}$) with temperature. **(d)** Variation of shot noise suppression factor with temperature.

shows that as the drain-source voltage increases, the shot noise suppression factor also increases, meaning that the proportion of shot noise becomes larger. This happens because a higher drain-source voltage increases the carrier velocity, reducing the number of scattering events in the channel. As a result, the thermal noise component decreases, whereas the shot noise component increases to compensate for this reduction. This explains why the overall change in channel current noise in Fig. 6(c) is small. Therefore, as the drain-source voltage increases, the dominant component of excess noise gradually shifts from thermal noise to shot noise.

Furthermore, Figs. 6(a)–(d) collectively indicate that as the channel length decreases, the noise in the device channel region gradually increases, leading to excess noise. Concurrently, the shot noise suppression factor rises, indicating that the degree of shot noise suppression weakens progressively with decreasing channel length. Specifically, when the channel length is reduced from 30 nm to 20 nm, the increase in the shot noise suppression factor is relatively small. However, when the channel length is further decreased from 20 nm to 10 nm, the shot noise suppression factor increases significantly, with a marked rise in the shot noise component. This suggests that as the channel length is reduced to approximately 20 nm, the dominant component of excess noise begins to shift from being primarily thermal noise to being predominantly suppressed shot noise.

Figure 7(a) shows the variation of channel current noise components with substrate doping density. As the substrate doping density increases, the channel current noise gradually decreases and approaches the total shot noise level. This trend indicates that with higher substrate doping density, the dominant component of excess noise in the channel shifts from thermal noise to suppressed shot noise. Figure 7(b) further reveals the relationship between the shot noise suppression factor and substrate doping density. As the substrate doping density increases, the shot noise suppression factor increases slightly, indicating that the proportion of shot noise in the excess noise of the MOSFET gradually rises.

Figure 7(c) illustrates the variation of channel current noise components with temperature. As the temperature increases from 200 K to 320 K, the channel current noise gradually deviates from the total shot noise level. This phenomenon occurs because the rise in temperature

enhances inelastic scattering effects, thereby increasing the suppression of shot noise. As a result, shot noise becomes less likely to dominate the excess noise in the channel at higher temperatures. Figure 7(d) further reveals the relationship between the shot noise suppression factor and temperature. As the temperature increases, the shot noise suppression factor gradually decreases, indicating a declining proportion of shot noise in the excess noise of the channel.

The analysis of Figs. 7(a)–(d) indicates a strong size dependence of the excess noise components in MOSFET channels, with approximately 20 nm serving as the critical channel length for this transition. Specifically, as the channel length decreases, the shot noise suppression factor increases monotonically, leading to a substantial rise in the proportion of suppressed shot noise. As seen in Figs. 7(b) and (d), the degree of shot noise suppression changes little when the channel length is reduced from 30 nm to 20 nm. However, when the channel length is further decreased from 20 nm to 10 nm, the shot noise suppression factor increases significantly, accompanied by a marked increase in the shot noise component. This finding corroborates the theoretical prediction that when the channel length is reduced to around 20 nm, the dominant component of channel excess noise transitions from thermal noise to suppressed shot noise.

5 Conclusion

Based on the McKelvey flux method, a model for the transition of excess noise components in nanoscale-channel-length MOSFETs is established. Combined with 3D Monte Carlo simulations, the evolution of excess noise components with decreasing channel length in small-scale nanoscale MOSFET devices is revealed: the transition of the dominant component from thermal noise to shot noise occurs within a threshold range centered at approximately 20 nm (with a dynamic range of 18–24 nm). When the channel length falls below this range, the carrier transport mechanism shifts from being dominated by drift-diffusion to being dominated by ballistic transport. Ballistic transport leads to the dominance of shot noise. Furthermore, at specific device dimensions, the transition of noise components is also regulated by several key parameters: a decrease in gate voltage, an increase in drain-source voltage, a decrease in temperature, and an increase in substrate doping concentration all lead to an increase in the shot noise component. The transition of excess noise mechanisms is determined by a dynamic phase boundary jointly modulated by electrical and process parameters.

Declarations The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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