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Self-aligned TiO_x-based 3D vertical memristor for a high-density synaptic array

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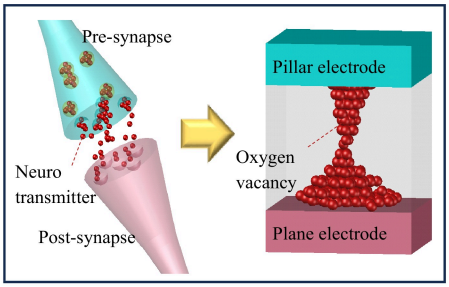
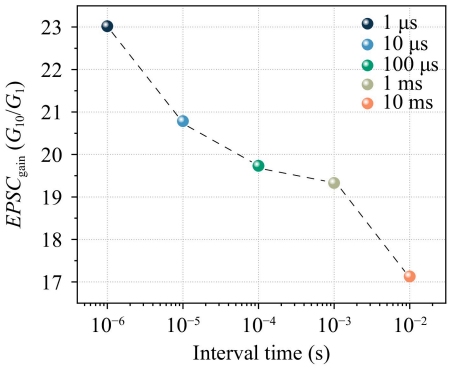
ABSTRACT

The emerging nonvolatile memory, three-dimensional vertical resistive random-access memory (VRRAM), inspired by the vertical NAND structure, has been proposed to replace NAND flash memory which has reached its integration limit. To improve the vertical ionic diffusion occurring in the conventional VRRAM structure, we propose a Pt/HfO_2/TiO_2/Ti self-aligned VRRAM with physically confined switching cells through sidewall thermal oxidation. We achieved stable bipolar switching, endurance (>10^4 cycles), and retention (>10^4 s) responses, and improved the interlayer leakage current issue through a distinctive self-aligned structure. Additionally, we elucidated the switching mechanism by analyzing current levels concerning ambient temperature. To utilize VRRAM for neuromorphic computing, the biological synaptic functions are emulated by applying pulse stimulation to the synaptic cell. The weight modulation of biological synapses is demonstrated based on potentiation, depression, spike-rate-dependent plasticity, and spike-timing-dependent plasticity. Additionally, we improve the pattern recognition rate by creating a linear conductance modulation with an incremental pulse train in pattern recognition simulations. The stable electrical characteristics and implementation of various synaptic functions demonstrate that self-aligned VRRAM is suitable for neuromorphic systems as a high-density synaptic device.

Keywords 3D integration, resistive switching, vertical RRAM, synaptic plasticity, self-aligned insulator





1 Introduction

Following the rapid advancements in artificial intelligence (AI) technologies, represented by chat GPT and autonomous driving, there is an increasing demand for more efficient high-density memory and AI semiconductors. NAND flash memory has been leading the market as a frontrunner in nonvolatile memory owing to its high integration and data-storage capabilities [1–3]. By leveraging the structural advantages of NAND flash memory, vertical NAND (VNAND) has been developed, which stacks in the vertical direction to use space efficiently and store more bits [4–9]. VNAND continues to increase the number of layers to satisfy the increasing memory density requirements. However, NAND flash memory is facing a problem as the required size of the device continues to shrink, and the fabrication process difficulty intensifies during the scaling process [10]. Hence, ongoing research focuses on developing fast and efficient nonvolatile memory (NVM) [11–15]. One of the NVMs, resistive random-access memory (RRAM), is gaining attention owing to its simple sandwich structure and

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metal–insulator–metal, high-switching speed, material diversity, and high-integration characteristics [16–20]. The conductive filament of RRAM is not formed in a specific area within the insulator layer, but rather in a random area, leading to increased instability and cycle-to-cycle or device-to-device variability in the memory device. To address this variability in a stable manner approaches such as stochastic, behavioral, and mesoscopic models, as well as limiting the switching oxide volume to improve reliability, are used [21, 22].

Among various insulating layers, the metal oxide is a major bipolar resistive switching material. HfO_x stands out as a representative material for RRAM owing to its advantages, such as fast switching speed, complementary metal-oxide semiconductor compatibility, and high-dielectric constant (~25) among a diverse range of metal oxides [23–26]. Memristors with HfO_2 mostly conduct stochastic switching through conductive filaments [27]. Therefore, a single HfO_x layer exhibits an abrupt set process and an unstable set voltage. To stabilize such stochastic switching, TiO_x can be inserted into the bilayer structure [28, 29]. Furthermore, TiO_x is a promising candidate as a switching layer owing to its high-dielectric constant (~33), and high-dielectric permittivity [30–32]. TiO_x is commonly deposited using several methods, including physical vapor deposition involving reactive sputtering and chemical vapor deposition, which includes atomic layer deposition (ALD). However, it is also possible to create a TiO_x layer by thermally oxidizing titanium metal at high temperatures with oxygen injection [33, 34]. The oxidation process has the advantage of being cost-effective in mass production as it can treat multiple devices in a single fabrication sequence. In addition, RRAM is being researched as a device capable of implementing neuromorphic computing in computing systems that mimic the operation of the biological brain [20, 35, 36]. An important factor in implementing neuromorphic computing is to create stable interactions between the pre- and post-synaptic neurons by applying external stimuli, ultimately constructing an artificial neural network (ANN) that mimics the neural network in which biological neurons interact to process information. Spike neural network (SNN), which is one type of ANN, mimics the neuron's spike-based information processing method. SNN utilizes discrete signals known as spikes, leading to advantages in power consumption and efficiency. The spikes in SNNs contain temporal information, enabling these neural networks to utilize time-based information [37]. Additionally, another time-dependent data processing method, reservoir computing, can be implemented using two-terminal memory devices with short-term memory characteristics [38]. These neural networks can be implemented through external pulse stimulation composed of various manipulation variables such as stimulus intensity, frequency, and the presence of previous stimuli, applied to memristors, resulting in synaptic weight modulation.

Utilizing the structural features of VNAND to create a high-density VNAND-like, three-dimensional (3D) vertical RRAM (VRRAM) is a practical option for replacing flash memory [39–42]. VRRAM is created by alternately depositing a metallic planar electrode and a passivation layer followed by the creation of a large diameter trench. The switching layer is then uniformly generated on the trench's sidewall using methods such as ALD, sputtering, and metal oxidation. The pillar electrode is then patterned to complete the process. When creating the same number of cells, VRRAM exhibits higher fabrication efficiency and scalability as the lithographic process is simplified compared with a planar structure [43]. The conventional VRRAM experiences interlayer leakage currents owing to the vertical diffusion of electrons caused by a continuous switching layer [44]. These leakage currents impact adjacent cells, thus leading to issues, such as reduced efficiency, increased power consumption, and undesired read errors [45–47]. A self-aligned VRRAM featuring a restricted switching layer formed by oxidizing a plane electrode at high temperatures is proposed that is distinct from the conventional continuous switching layer. Utilizing devices with this structure allows improved device operation characteristics by physically preventing unnecessary ionic diffusion [48, 49]. The TiO_x layer generated through the oxidation process simplifies the fabrication process as it oxidizes the target metal without the need for additional lithographic and deposition processes.

In this study, we demonstrate a promising option for next-generation NVM through a self-aligned VRRAM with a $Pt/HfO_2/TiO_x/Ti$ stack to enhance synaptic performance. The uniformity and electrical stability of fundamental memory characteristics, such as endurance and retention, are verified through cycle-to-cycle and comparisons between layers. In addition, the improved sneak current issue with the TiO_x layer formed through oxidation is also verified through interlayer measurements. The potential application of these synaptic devices for neuromorphic computing systems is demonstrated by emulating various biological features of the human brain, including synaptic weight modulation through pulse train modulation, potentiation, depression, excitatory postsynaptic currents (EPSC), and spike-timing-dependent plasticity (STDP).

2 Experimental section

A $Pt/HfO_2/TiO_x/Ti$ 3D VRRAM device was fabricated using the following process. First, Ti (50 nm) for the plane electrode was deposited using radiofrequency reactive sputtering, and SiO_2 (50 nm) for the passivation layer was created using plasma-enhanced chemical vapor

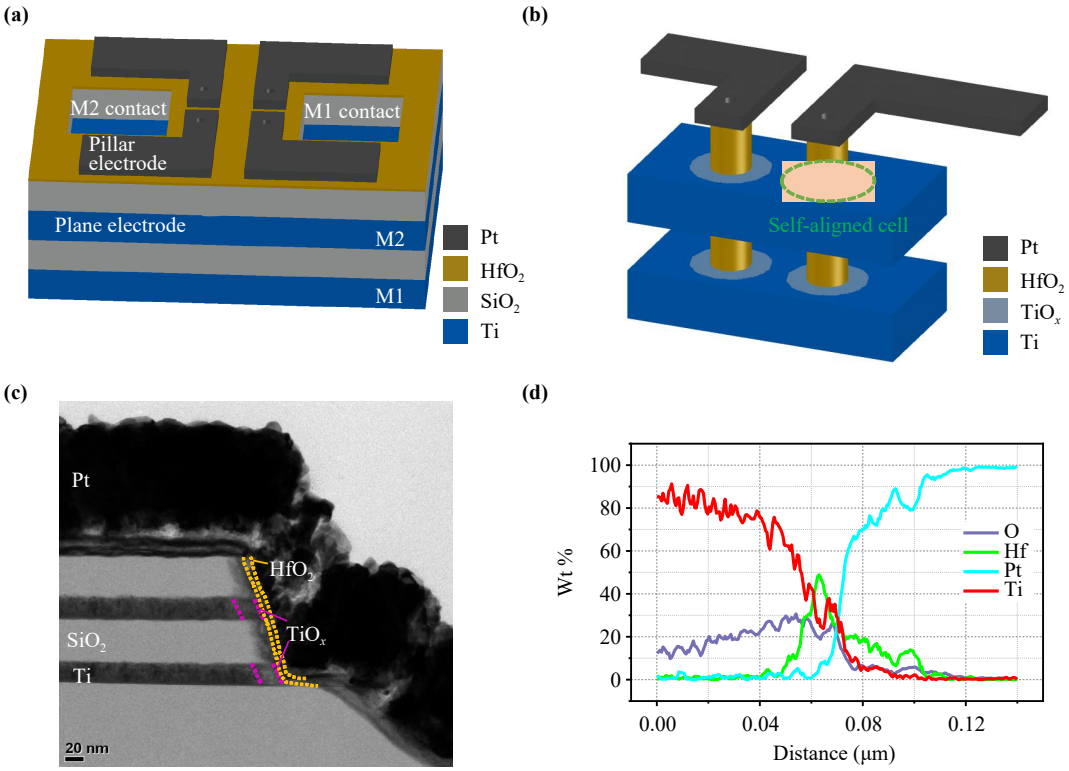

Fig. 1 **(a)** Three-dimensional (3D) schematic of vertical resistive random-access memory (VRRAM). **(b)** Schematic with self-aligned cell configured around a planar Ti electrode. **(c)** Transmission electron microscopy (TEM) image of VRRAM. **(d)** EDS line scan at the second layer.

deposition. To fabricate the 3D stack structure, Ti and SiO_2 were alternately deposited in two cycles. Trench holes were patterned to make vertical RRAM cells, and dry etching was performed using an inductively coupled plasma etcher (Oxford ICP etcher) with CHF_3 gas. To make self-aligned TiO_x by reacting with sidewall Ti inside the hole pattern, annealing was then performed at 400 °C for 10 min at ambient oxygen conditions. Subsequently, HfO_2 (3 nm) was deposited as the switching layer using ALD. The HfO_2 layer used TEMAHf as a precursor and ozone (O_3) as a reactant at 350 °C. Subsequently, to apply bias to the plane electrode, contact pads of each plane electrode layer were patterned and dry etched. Finally, for the adhesion layer, a 10 nm thick layer of Ti and for the pillar electrode and Pt (100 nm) were deposited using an E-beam evaporator followed by a lift-off process. Electrical data using direct current (DC) pulses were measured using a semiconductor parameter analyzer (Keithley 4200-SCS) and an ultrafast 4225-PMU module.

3 Results and discussion

3.1 Structural elements analysis of VRRAM

In Fig. 1(a), we illustrate the overall schematic of each layer element composition in VRRAM. Although not evident in the overall schematic, the self-aligned TiO_x layer formed between the planar electrode Ti and the pillar electrode Pt due to the thermal oxidation of Ti metal (after hole etching during the fabrication process) can be observed in Fig. 1(b). The description of the fabrication process flow is illustrated in Fig. S1(a) of the Electronic Supplementary Materials (ESM). Figure 1(c) presents a transmission electron microscopy (TEM) image of a cylindrical hole pattern. We can confirm the structural characteristics of the planar electrode (20 nm Ti) and passivation layer (a 50 nm SiO_2). Furthermore, a relatively brighter image with the increased intensity at the edges of the Ti hole pattern due to thermal oxidation indicates the formation of the TiO_x layer. Moreover, we observed the uniformly deposited HfO_2 switching layer and the Ti and Pt layers which served as the adhesion layer and the pillar electrode, respectively. In Fig. S1(b) of the ESM, the EDS mapping results of each element are presented. In Fig. 1(d), an EDS line scan conducted on the second floor is presented to verify the presence of the oxidation-formed TiO_x layer. The oxygen ratio just before the Hf peak shows a significantly higher percentage, which is more than twice the oxygen percentage in the Ti layer. This indicates that the TiO_x layer was formed between Ti and HfO_2 during high-temperature oxidation conditions.

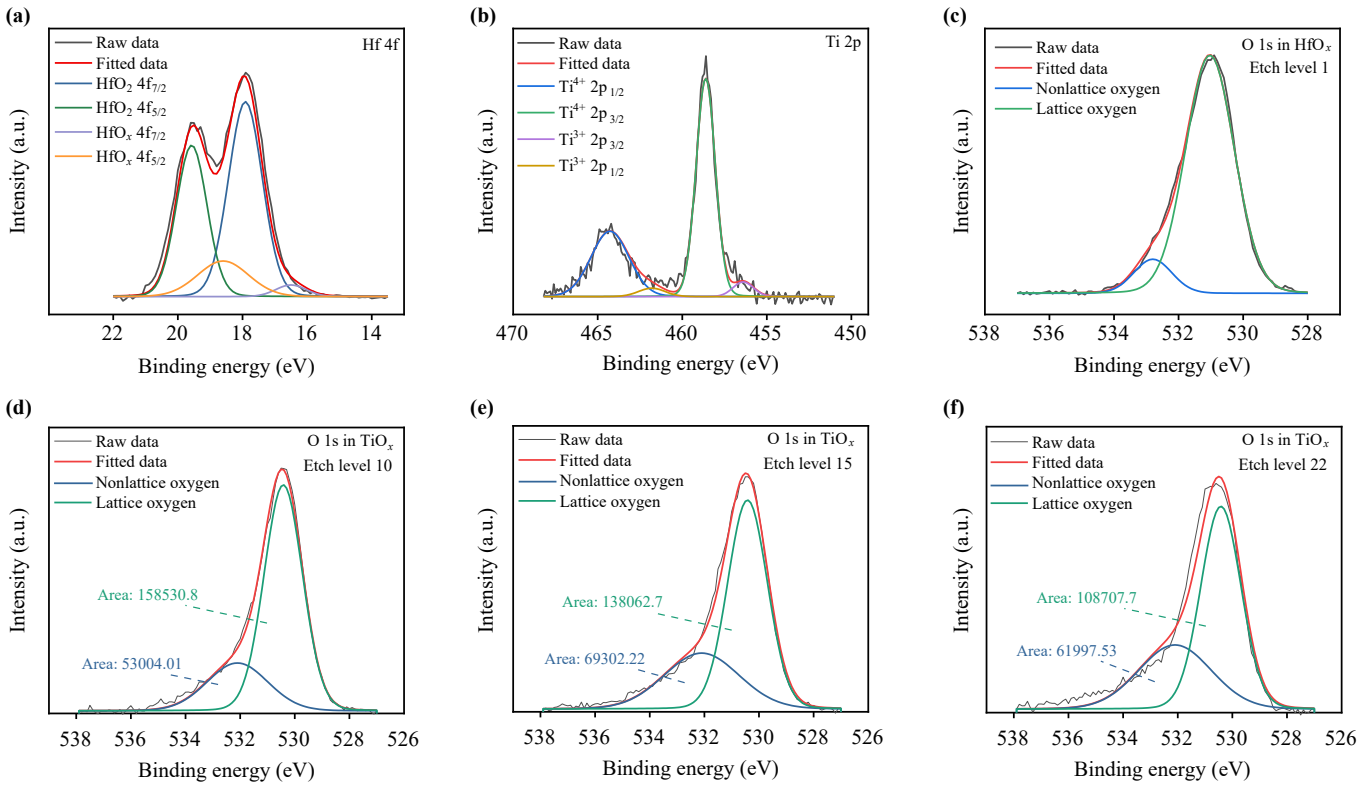

Fig. 2 XPS core level spectra of **(a)** Hf, **(b)** Ti, and **(c)** O 1s in HfO_2 at etch level 1. O 1s in TiO_x at etch levels **(d)** 10, **(e)** 15, and **(f)** 22.

XPS analysis was conducted to investigate the chemical composition and elemental bonding in the switching layer. For XPS analysis, the $HfO_2/TiO_x/Ti$ samples were also prepared using the same process method as that used for VRRAM. Figure 2(a) displays the XPS spectra of Hf 4f. The XPS spectra of Hf are deconvoluted into a doublet peak corresponding to the oxygen vacancy ratio, with a higher intensity representing the Hf 4f 7/2 and Hf 4f 5/2 components and a lower intensity corresponding to Hf 4f 7/2 and Hf 4f 5/2 [50]. Similarly, the XPS spectra of Ti deconvoluted in four peaks, as depicted in Fig. 2(b). Peaks formed at 458.6 eV and 464.28 eV represent the main valence state of TiO_x, specifically indicating Ti^{4+} 4p 3/2 and 1/2, respectively. Peaks at lower intensities (461.8 eV and 456.4 eV), corresponding to Ti contributing to Ti^{3+}, potentially owing to insufficient activation of the oxide, could contribute to subsequent oxygen vacancy formation [51]. Analysis of O 1s in HfO_2 XPS spectra at etch level 1 is presented in Fig. 2(c). A peak indicating the presence of nonlattice oxygen, which contributes to the formation of oxygen vacancies, was observed at 532.8 eV, while a peak representing the bonding between Hf and oxygen, indicating lattice oxygen, was observed at 531.03 eV. At etch level 10, an O 1s peak was observed, representing the O 1s spectra in the TiO_x layer formed by oxidation. Figures 2(d)–(f) illustrate the XPS spectra of O 1s in the TiO_x layer based on the etch level. Peaks corresponding to lattice oxygen and nonlattice oxygen were formed at 530.42 eV and 532.1 eV, respectively. The area of lattice oxygen bonded to the metal showed a decreasing trend as the etch level increased, while nonlattice oxygen, which is involved in the formation of oxygen vacancies, appeared to be more concentrated in the bulk compared with the surface.

3.2 Electrical properties and comparison of operation in self-aligned VRRAM

Figure 3(a) depicts the electroforming process and bipolar resistive switching in the first metal (M1). When applying a dual sweep bias from 0 to −10 V, an electroforming process is observed, transitioning from the initial state to the low-resistance state (LRS), as shown in the inset. To prevent hard breakdown during this process, the compliance current was set to 100 μA. When a negative bias of 0 to –4 V was applied, the device switched abruptly from a high-resistance state (HRS) to LRS. Similarly, applying a positive bias of 0 to 4 V allowed the transition from the LRS to HRS. Note that no additional compliance current was necessary for bipolar switching. The hysteresis loop during resistive switching in self-aligned VRRAM can be interpreted by the migration of oxygen ions within the oxide layer induced by the external electric field applied to each electrode [52, 53]. The electroforming and resistive switching in the second metal

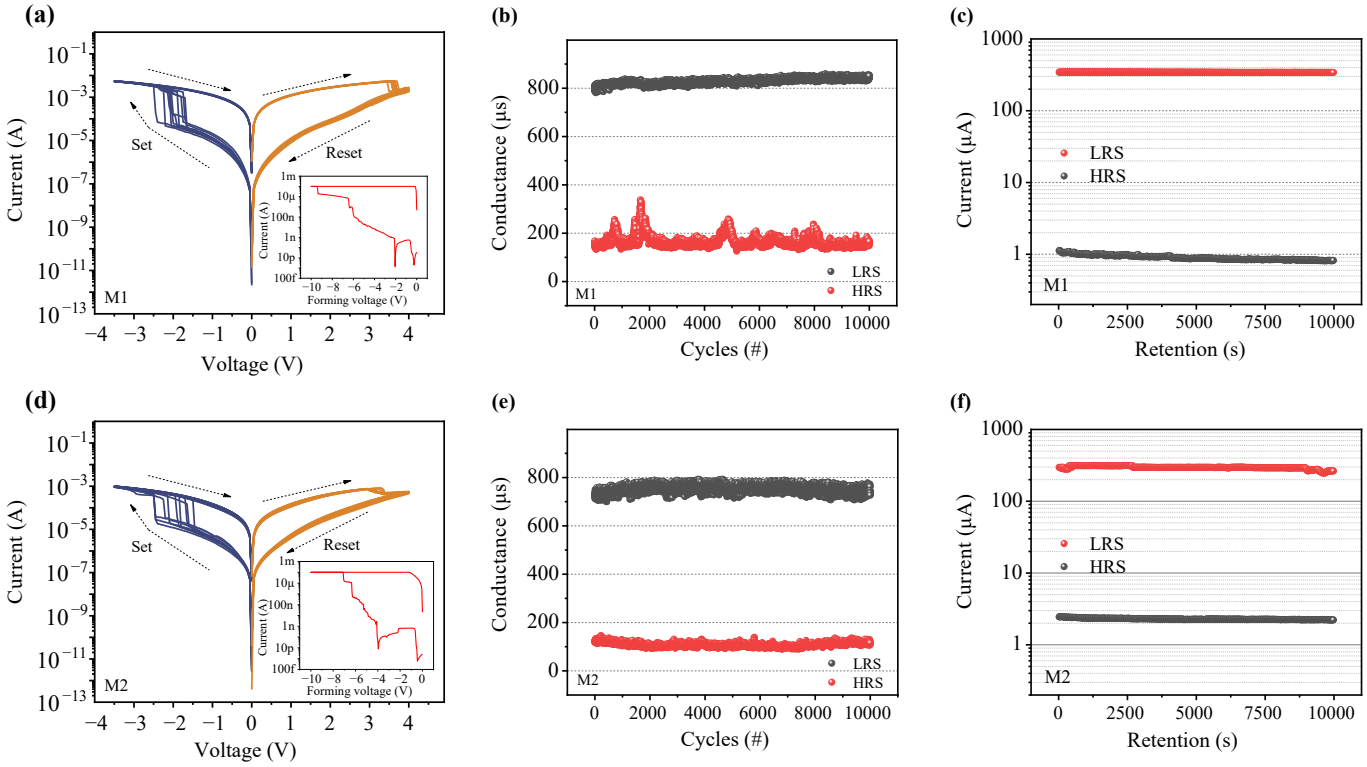

Fig. 3 **(a)** *I–V* characteristic, **(b)** endurance with pulse, and **(c)** retention in the first metal layer. **(d)** *I–V* characteristic, **(e)** endurance, and **(f)** Theme6 contentAck1 retention in the second metal layer.

(M2) were measured in the same way as in M1 and are depicted in Fig. 1(d). Both M1 and M2 switching graphs demonstrate stable operation over 20 cycles. The current distribution (100 cycles) for each metal floor is depicted in Figs. S2(a) and (b) of the ESM. Figures 3(b) and (e) illustrate the pulse endurance of M1 and M2 over 10000 cycles, respectively. Every read during the endurance test was applied at 0.5 V. Throughout all endurance tests, both the LRS and HRS maintained stable conductance levels, with minimal differences between levels in different layers. Figures 3(c) and (f) present the retention results at room temperature. Retention was also read at 0.5 V and demonstrates nonvolatile characteristics by maintaining stable current levels over cycles. Additionally, the stable cell-to-cell distribution of each layer is illustrated in Figs. S2(c) and (d) of the ESM. Based on prior experiments, self-aligned VRRAM exhibits uniform resistive bipolar switching, stable endurance over 10 000 cycles, and nonvolatile characteristics. Additionally, similar operating current levels are observed in each layer during bipolar switching. However, slight differences found in each experiment were attributed to the irregular TiO_x oxide layer resulting from variations in interface area owing to the slope created during the etching process.

To address the sneak current generated by the electron diffusion through the consecutive insulating layers in conventional VRRAM, the sneak current measurements

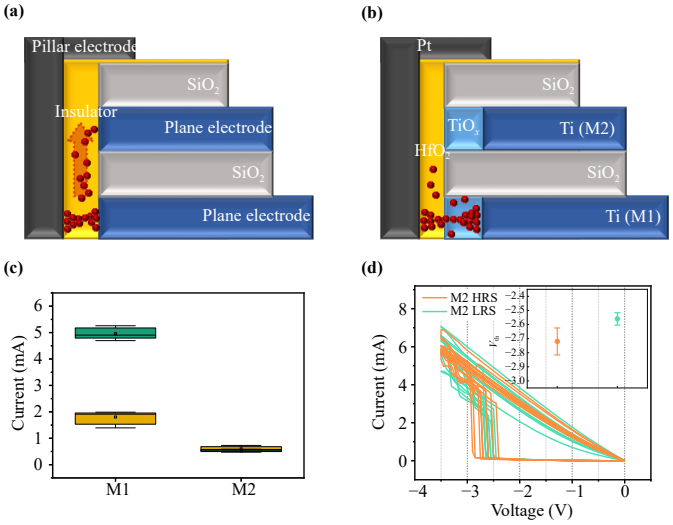

Fig. 4 Schematic of the leakage current in **(a)** conventional VRRAM and **(b)** self-aligned VRRAM. **(c)** Current level switching of M1 while M2 retains the HRS. **(d)** The threshold voltage distribution of M1 depends on the resistance state of M2.

of the self-aligned VRRAM with a physically confined switching layer are presented. Figure 4(a) describes the ion diffusion during resistive switching in traditional VRRAM. Due to the continuous switching layer of the traditional VRRAM, an interlayer leakage current

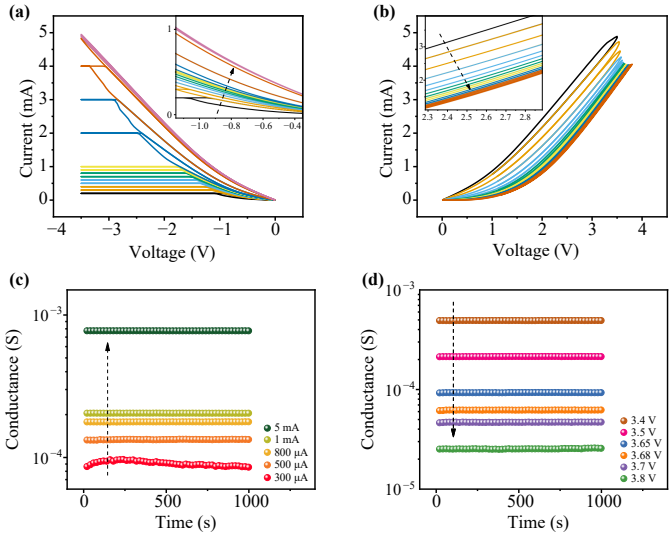

Fig. 5 Multilevel characteristics for **(a)** set and **(b)** reset processes. Multilevel retention in **(c)** LRS and **(d)** HRS.

occurs, which leads to undesired read errors and a decrease in device performance. On the other hand, Fig. 4(b) shows the movement of ions in self-aligned VRRAM. The self-aligned VRRAM can effectively prevent vertical ion diffusion through the physically limited TiO_x switching layer. During the sneak current experiment, M1 was switched between the LRS and HRS by applying set and reset voltages, while M2 remained in the HRS to measure the sneak current leaking during M1 operation. The results of 10 cycles of switching are summarized in a box plot in Fig. 4(c). M1 switches between the high-current level of the LRS (green) and the low-current level of HRS (yellow), while the box plot of M2, which represents the sneak current, shows that it maintains its initial current level of HRS regardless of the switching of M1. Moreover, the experiment investigating the switching of M1 and the threshold voltage ($V_{\rm th}$) according to the resistance state of M2 (inset) is shown in Fig. 4(d). The average $V_{\rm th}$ of M1 when M2 is in LRS is –2.72 V, and the average $V_{\rm th}$ of M1 when M2 is in HRS is −2.56 V, yielding a minor 6% difference. This demonstrates that the sneak current, which was caused by the structural disadvantage of VRRAM was reduced owing to the self-aligned cell of VRRAM fabricated using the thermal oxidation process.

Implementing a multilevel cell (MLC) with various conductance states is essential for multibit storage. MLC provides higher data storage density compared with basic memory cells that only store a single bit, thus enabling low-cost, high-efficiency devices [54, 55]. To implement MLCs, we gradually adjusted the levels of LRS by controlling the CC during the set process. As the applied CC became higher, the formed filament became stronger, thus enabling the implementation of MLC through resistance state modulation. As confirmed in Fig. 5(a), an MLC differentiated into 16 states (from 100 μA to 5 mA) can achieve higher levels of LRS as the CC increases. To adopt an MLC during the reset process, an incrementally increasing reset voltage was applied to the LRS device. Figure 5(b) shows that by applying a reset bias from –3.5 to –3.8 V, an MLC was implemented which differentiated into 16 states, thus indicating that the HRS decreases as a stronger reset bias is applied. Figure 5(c) shows the retention for 10^3 s at a particular resistance state controlled by CC among the multiple levels of the LRS. Figure 5(d) is the retention of HRS according to the modifying reset voltage. We observed a noticeably discrete HRS that was stably maintained during the retention test according to the applied reset voltage. This demonstrates the implementation of MLC by intentionally controlling the resistance state by current limit and bias modulation without distinctive degradation.

The formation and rupture of conductive filaments, induced by the migration of oxygen vacancies owing to an external electric field, constitute the primary switching mechanism in RRAM. Figure 6(a) depicts a schematic of oxygen vacancy migration in the switching layer between the pillar electrode Pt and the planar electrode Ti. According to XPS results, the proportion of nonlattice oxygen contributing to oxygen vacancies is higher in the TiO_x layer compared with that in the HfO_2 layer. Furthermore, ionic mobility in the insulator is faster in the HfO_2 layer than in the TiO_x layer, thus leading to the precedence of conductive filament formation and dissolution in the HfO_2 layer. In Fig. 6(b), the fitting of the I–V curve based on Schottky emission is presented for a comprehensive analysis of the conduction mechanism. Schottky emission is obtained using equation:

$$J = A^{*}T^{2}\exp\left[\frac{-q\left(\phi_B - \sqrt{qE/(4\pi\varepsilon_i)}\right)}{kT}\right], \qquad (1)$$

where T is the absolute temperature, A^{*} is the Richardson constant, ϕ_B is the Schottky barrier height, ε_i is the permittivity of the insulator layer, and k is Boltzmann's constant [56]. The linear relationship between $\ln I$ and sqrt(V) from 0.5 to 1.53 V in the LRS and 0.67 V to 1.96 V in HRS signifies that Schottky emission is the primary switching mechanism of this self-aligned VRRAM. The intercept and slope, parameters derived from the Schottky emission formula, represent the barrier height and Schottky emission distance, respectively [57]. The intercepts in the LRS and HRS, 12.008 and 17.299 respectively, indicate a decrease in the Schottky barrier height upon transitioning from HRS to LRS, thus facilitating electron movement across the reduced barrier. Schottky emission refers to the emission of activated electrons that have obtained sufficient thermal energy to overcome the energy barrier. As indicated by the equation, the current density increases in proportion

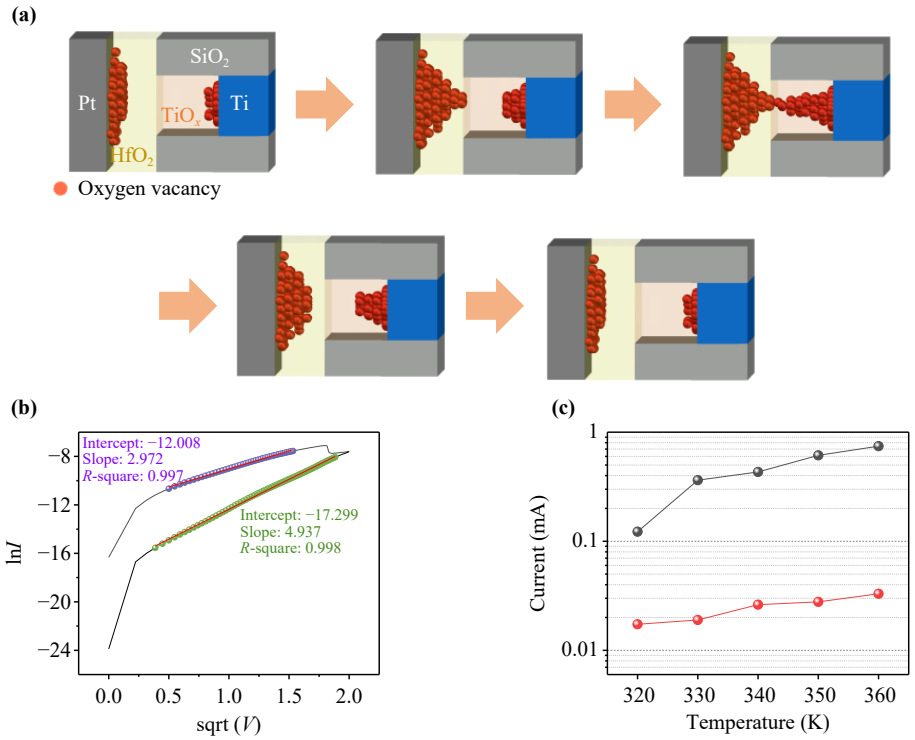

Fig. 6 **(a)** Schematic of the oxygen vacancy migration during the switching process. **(b)** Conduction mechanism fitting based on Schottky emission. **(c)** Variations of current levels in LRS and HRS as a function of the ambient temperature.

to T^2. Figure 6(c) shows the current levels of LRS and HRS measured by increasing the temperature by 10 K from 320 to 360 K. As the temperature increases, it can be observed that the current levels of both the LRS and HRS increase. This indicates that thermally excited electrons are emitted over the barrier in proportion to the temperature.

3.3 Applications for artificial synapse implementation

As illustrated in Fig. 7(a), the biological brain is composed of neurons interconnected via synapses that generate electrical and chemical signals. Synapses engage in the interaction of electrical signals between neurons, facilitating information processing. Pre-synaptic neurons release neurotransmitters in the synaptic cleft that eventually bind to post-synaptic receptors and are uptaken by postsynaptic neurons to achieve information transmission. This model is analogous to two-terminal memristors, modulating resistance states through oxygen vacancies formed between pillar and planar electrodes using external electrical stimulation [Fig. 7(b)]. To implement a neuromorphic computing system using a memristor as an artificial synaptic device that emulates biological synapses, a suitable change in conductance (i.e., synaptic weight) in response to pulse stimuli is essential. We applied various pulse stimulations to our self-aligned VRRAM to adjust synaptic weights utilizing it as a synaptic device.

We initially conducted experiments on EPSC demonstrating the modulation of postsynaptic electrical responses based on the intensity and frequency of external stimulations. EPSC encompasses spike-rate-dependent plasticity (SRDP), where stimuli of varying frequencies are applied while maintaining a constant intensity, and spike-amplitude-dependent plasticity (SADP), which modulates synaptic weight through changes in the amplitude of the stimulus. To implement the SRDP characteristics of neurons based on spike intervals in VRRAM, we applied 10 programming pulses using different interval times (1 μs, 10 μs, 100 μs, 1 ms, and 10 ms). The pulse width was 50 μs, and the amplitude was maintained at −1.8 V, followed by a 0.5 V/20 μs read pulse after each pulse train. To investigate the decrease in the conductance based on interval time, an erasing pulse was applied after a −4 V set pulse with a pulse width of 50 μs, an amplitude of 3.4 V, and an interval time identical to the preceding one. The detailed changes in conductance for each pulse scheme are presented in Figs. S3(a) and (b) of the ESM. We express conductance modulation in the form of an EPSC gain using equation:

$$EPSC_{\text{gain}} = \frac{G_{10}}{G_1}, \tag{2}$$

where G_{10} is the conductance after final pulse stimulation and G_1 is the initial conductance. Figure 7(c) depicts the $EPSC_{\text{gain}}$ with the programming pulse scheme. In this

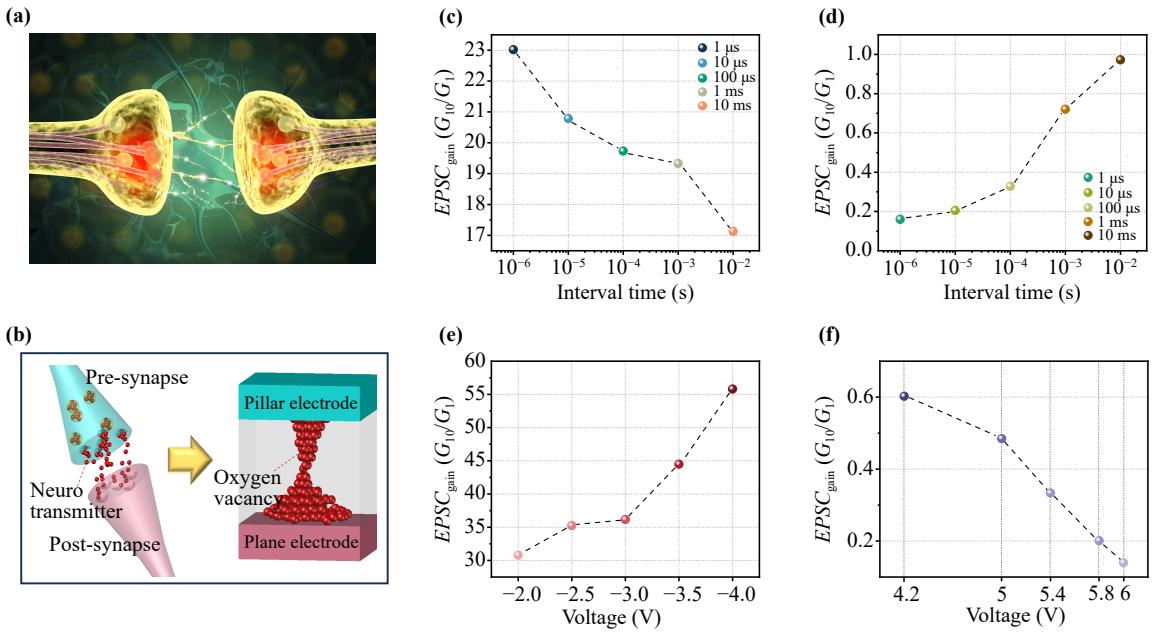

Fig. 7 **(a)** Conceptual illustration of signal transmission in human brain synapses. **(b)** The conceptual structure of biological and artificial synapses. Excitatory postsynaptic current (EPSC) gain modulation relative to interval time at **(c)** potentiation and **(d)** depression. EPSC gain modulation compared with pulse amplitude in **(e)** potentiation and **(f)** depression.

case, as the interpulse interval becomes shorter, the stimuli applied are stronger, thus resulting in the updating of a larger gain. The update rate of gain decreases as the interpulse interval increases. Figure 7(d) illustrates the $EPSC_{gain}$ with erasing pulses. With shorter interpulse intervals, more potent erasing pulses are applied, thus resulting in a significant reduction in final conductance compared with the initial conductance, thus yielding a minimal $EPSC_{gain}$. As the interpulse interval increases, there is a minimal change compared with the initial conductance, thus leading to an $EPSC_{gain}$ close to one.

Furthermore, we explored the characteristics of SADP using the self-aligned VRRAM. To achieve this, we applied 10 programming pulses ranging from –2 to –4 V with a 0.5 V increment and a consistent pulse width of 50 μs. Additionally, a read pulse of 0.5 V/20 μs was applied. We observed a rapid increase in conductance during the pulse train as the amplitude increased. The variation in conductance which resulted from erasing pulses of different amplitudes is shown in Fig. S3(c) of the ESM. The modulation of conductance which is the result of 10 pulses is presented in the supplementary data. Additionally, Fig. 7(e) shows a comparison of the final conductance with the initial conductance indicating that $EPSC_{gain}$ becomes larger at increasing pulse amplitudes. Upon application of the pulse train, we observed an increase in $EPSC_{gain}$ (>81.22%) between the smallest amplitude pulse of –2 V and the strongest pulse of –4 V.

To observe the conductance variation induced by erasing pulses with different amplitudes, we applied 10 identical pulses with the same pulse width (50 μs) and interval time, with amplitudes of 4.2 V, 5 V, 5.4 V, 5.8 V, and 6 V. Subsequently, a read pulse of 0.5 V/20 μs was applied after each pulse to analyze the conductance variation. The plot of the deviation in conductance due to erasing pulses at each amplitude is presented in Fig. S3(d) of the ESM. As the amplitudes of the erasing pulses increased, there was a significant decrease from the initial conductance. Figure 7(f) demonstrates a reduction in $EPSC_{gain}$ as the intensity of the erasing pulse increases. The gain of the strongest erase pulse (6 V) decreased by 76.79% compared with that of the weakest intensity pulse (4.2 V). This indicates that self-aligned VRRAM can effectively mimic synaptic properties that regulate the synaptic weight at the post-synaptic neuron, depending on the intensity of the stimulus transmitted at the pre-synaptic neuron.

The biological synapse exhibits STDP, adjusting the synaptic weight based on the time interval between the pre- and post-synaptic spikes. STDP is considered an essential function as the synaptic device because it follows the Hebbian learning rule, where the connection strength between neurons is regulated by the relative timing of firing between two neurons. When the pre-synaptic spike occurs before the post-synaptic spike, the connection between the two synapses strengthens, thus leading to an increase in synaptic weight. Conversely, if the pre-synaptic spike follows the postsynaptic spike, the synaptic connection weakens, thus causing a decrease in synaptic weight. The waveform depicted in Fig. 8(a) was utilized to implement STDP in the self-aligned VRRAM modifying the stimulation timing between the pre- and post-synaptic neurons. Figure 8(b) illustrates the synaptic weight change as a function of Δt. The solid red line

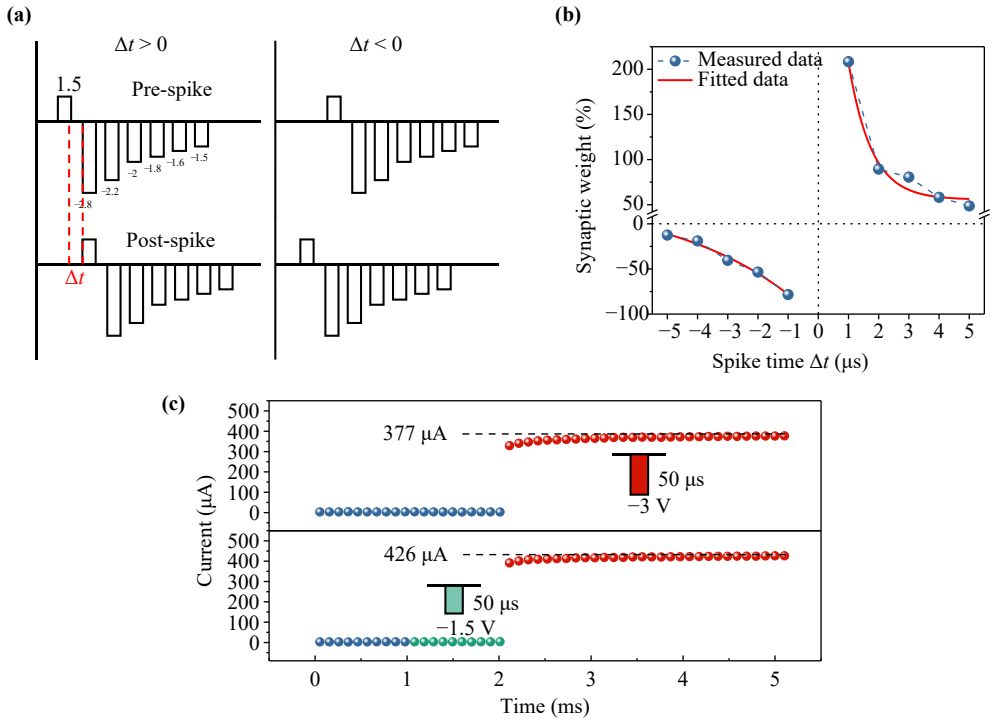

Fig. 8 **(a)** Prespike and postspike pulse schemes for spike-timing-dependent plasticity (STDP) measurements at Δt = 100 μs. **(b)** STDP results. **(c)** Activity-dependent synaptic plasticity (ADSP) behaviors of self-aligned VRRAM.

was fitted using equation:

$$\textit{Synaptic weight change} = \begin{cases} A_+ \exp\left(-\dfrac{\Delta t}{\tau_+}\right), & \text{if } \Delta t > 0 \\ A_- \exp\left(-\dfrac{\Delta t}{\tau_-}\right), & \text{if } \Delta t < 0 \end{cases}, \tag{3}$$

where Δt is the time interval between pre/postsynaptic spikes, $A_\pm$ represents the scaling factor, and $\tau_\pm$ is the time constant of the exponential function [58]. When the prespike precedes the postspike, that is, when Δt is positive, the connection strength of the synaptic pair increases/decreases/changes, thus inducing a potentiating condition. Conversely, with a negative Δt, the connection strength decreases, thus leading to a depressing condition. Moreover, by increasing the interval time between spikes, creating significant differences in synaptic firing timing, we observed a reduction in the change of synaptic weight. This demonstrates the suitability of self-aligned VRRAM as a synaptic device within neuromorphic systems.

As shown, it is possible to regulate the response of the postsynaptic neuron by adjusting the frequency and amplitude of the pulse train. Further, in the biological brain's learning mechanism, minor learning experiences that do not surpass the threshold can act as catalysts for subsequent prominent learning processes. Preceding the main program pulse, experienced stimulations (pulses) can influence the synaptic plasticity of the postsynaptic neuron, known as activity-dependent synaptic plasticity (ADSP) [58, 59]. Figure 8(c) depicts ADSP responses achieved using self-aligned VRRAM. The priming pulse (green), representing prior minor learning experiences, was set at a low amplitude (–1.5 V), insufficient to switch the device to an on state. Conversely, the programming pulse (red) representing the actual learning process was set at a higher voltage (–3 V). Following each pulse, a read pulse (blue) of 0.5 V/50 μs was applied. The upper panel demonstrates the modulation by applying only 20 read pulses without a priming pulse, thus confirming the initial state. Subsequently, the programming pulse was applied for learning, thus resulting in a current of 377 μA. Following the application of 10 read pulses, a priming pulse was applied to assess the impact of experienced stimulation on activating the device. While the priming pulse did not immediately affect the current level, it yielded a higher current level (426 μA) when the programming pulse was applied. This demonstrates that the priming pulse is not an adequately strong stimulus to cause total ionic migration in the memristor, but it can induce partial ionic migration, thus resulting in higher current levels in cases in which the applied (main) pulse has a higher voltage amplitude. Thus, the postsynaptic current regulated by the priming pulse demonstrates the implementation of one of the biological brain's learning mechanisms, namely ADSP, in VRRAM.

To replicate an artificial synapse mimicking the

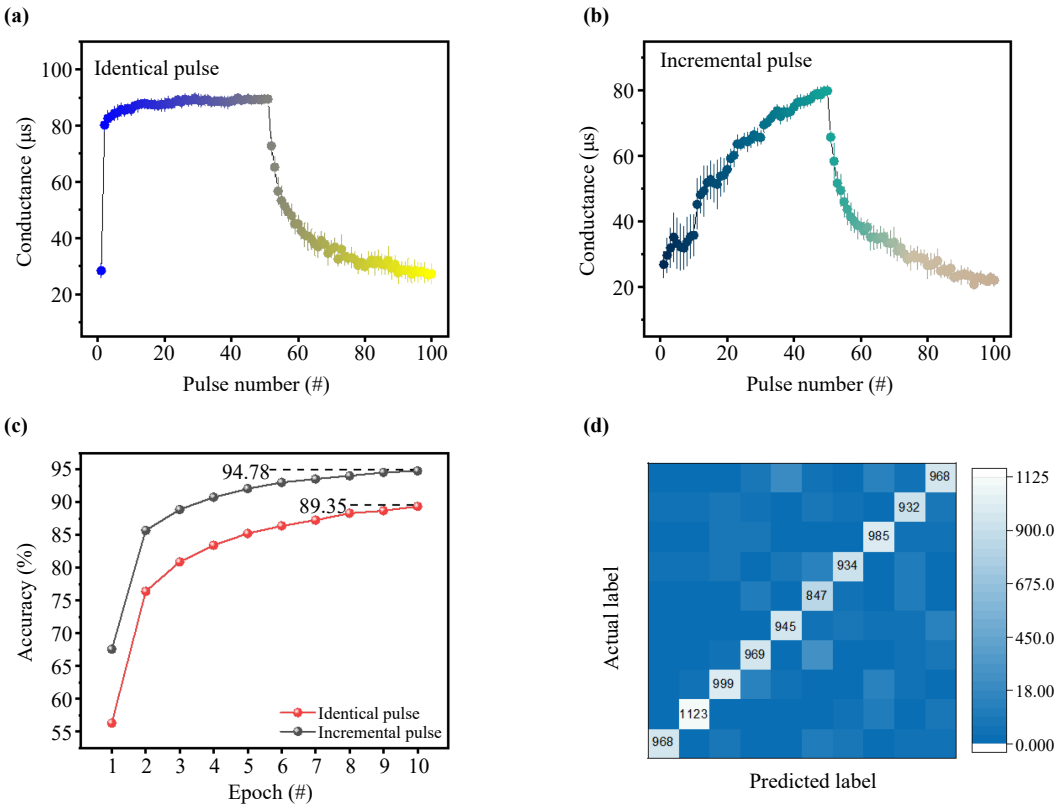

Fig. 9 Potentiation and depression under **(a)** identical pulse and **(b)** incremental pulse scheme conditions for linear conductance modulation. **(c)** Training results of pattern recognition with incremental pulse modulation. **(d)** Pattern recognition test after training.

biological synapse, various pulse analyses were conducted. Among them, long-term potentiation (LTP) and long-term depression (LTD) are essential synaptic functions [60, 61]. The interaction between the pre- and postsynaptic neurons through pulse stimulation results in either potentiation or depression. Two methods were employed to achieve effective implementation of both LTP and LTD. The first involved the representation of LTP and LTD using 50 consecutive identical programming pulses. Figure 9(a) illustrates a graph plotting the average, maximum, and minimum values of 10 cycles of 50 potentiation and depression pulses. The complete data for the 10 cycles are available in Fig. S4(a) of the ESM. For potentiation, pulses of –1.5 V/50 μs were used, while for depression, 1.45 V/50 μs pulses were utilized, and a read pulse of 0.5 V/50 μs was employed. However, binary modulation of potentiation and depression using identical programming pulses does not satisfy the characteristics of analog synaptic plasticity. Using the second method (the incremental pulse scheme), more linear LTP and LTD responses are obtained, as shown in Fig. 9(b). For potentiation programming, we applied 10 programming pulses with amplitudes of –0.7 V, –0.9 V, –1 V, –1.2 V, and –1.4 V with the same duration of 50 μs, thus resulting in a gradual change in conductance. During the depression, a sequence of 20 reset pulses were applied for 50 μs at 1.15 V and 10 pulses at 1.3 V, 1.35 V, and 1.4 V. This process demonstrated a linear reduction in conductance during the depression pulse sequence. The complete data for 10 cycles is presented in Fig. S4(b) of the ESM.

To evaluate of performance of the synaptic device for the neuromorphic system, pattern recognition simulations were conducted. In simulations, deep neural networks, a type of ANN, were used and employed the Modified National Institute of Standards and Technology (MNIST) database. The set of 60 000 MNIST training images, structured with 600 columns and 100 rows, constitutes input data processed through a nonlinear transformation across three hidden layers to yield an output across 10 nodes (representing labels from zero to nine). Figure 9(c) demonstrates the pattern recognition accuracy over 10 epochs using the conductance changes of LTP and LTD, utilizing both identical and incremental pulse schemes. The examples from the MNIST database for each pulse scheme are shown in Figs. S4(c) and (d) of the ESM. While the use of identical pulses showcased a final accuracy of 89.35%, the analysis employing the incremental pulse scheme revealed an improved accuracy of 94.78%. This demonstrates the potential of self-aligned VRRAM for enhanced utilization as a synaptic memristor based on linear conductance modulation. Utilizing the algorithm

trained from the previous training iteration, a simulation was performed using incremental programming pulse scheme data to determine the accuracy of labels for 10 000 test images from the MNIST database. The heat map of actual labels against predicted labels is shown in Fig. 9(d). Leveraging the algorithm trained with the previous set of 60 000 images, this simulation exhibited an improved recognition rate of 96.659%.

4 Conclusions

In this study, we fabricated a 3D VRRAM of Pt/HfO_2/TiO_x/Ti stack for application in neuromorphic computing. Structural imaging and elemental bonding states of each layer of the self-aligned VRRAM, including the TiO_x layer through sidewall titanium thermal oxidation after hole-type trench etching, were confirmed using TEM and XPS. We confirmed the layer-wise bipolar switching stability, uniform cell-to-cell deviation, reliable endurance, and retention. Additionally, we addressed the interlayer interference through the electron diffusion-restricted cell. We successfully implemented biological synaptic functions, such as potentiation, depression, STDP, and ADSP using TiO_x-based VRRAM as an artificial synaptic device. Finally, the self-aligned 3D VRRAM with the oxidized TiO_x layer has the potential to be utilized in neuromorphic computing as a promising artificial synapse.

Declarations The authors declare that they have no competing interests and there are no conflicts.

Author contributions Subaek Lee: Device fabrication; Measurement; Formal analysis; Investigation – performed the experiments; Resources; Writing – original draft. Juri Kim: Device Fabrication; Data curation. Sungjun Kim: Conceptualization; Writing – review & editing; Resources; Project administration; Funding acquisition.

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