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Sub-5 nm bilayer GaSe MOSFETs towards ultrahigh on-state current

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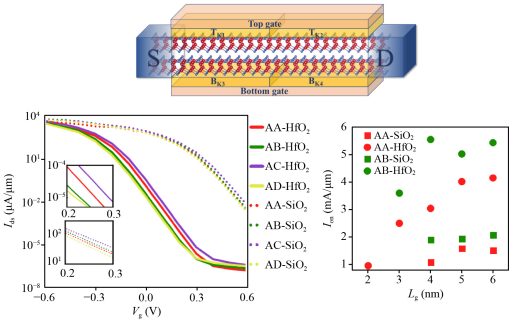
ABSTRACT

Dielectric engineering plays a crucial role in the process of device miniaturization. Herein we investigate the electrical properties of bilayer GaSe metal-oxide-semiconductor field-effect transistors (MOSFETs), considering hetero-gate-dielectric construction, dielectric materials and GaSe stacking pattern. The results show that device performance strongly depends on the dielectric constants and locations of insulators. When high-k dielectric is placed close to the drain, it behaves with a larger on-state current (I_{on}) of 5052 μA/μm when the channel is 5 nm. Additionally, when the channel is 5 nm and insulator is HfO_2, the largest I_{on} is 5134 μA/μm for devices with AC stacking GaSe channel. In particular, when the gate length is 2 nm, it still meets the HP requirements of ITRS 2028 for the device with AA stacking when high-k dielectric is used. Hence, the work provides guidance to regulate the performance of the two-dimensional nanodevices by dielectric engineering.



Keywords GaSe stacking pattern, metal-oxide-semiconductor field-effect transistors (MOSFETs), ultrahigh on-state current, dielectric engineering

1 Introduction

Two-dimensional (2D) semiconductors-based devices are promising for electronic and optoelectronic fields, such as photodetectors [1–3], solar cells [4–6], memristive [7–9], and neuromorphic devices [10–13]. Moreover, the performances of 2D devices are greatly affected by dielectric engineering [14, 15]. For Na_3Sb field-effect transistors (FETs), the HfO_2 dielectric is used to suppress the leakage current and decrease the off-state voltage [16]. Robert *et al.* [17] exploited TiO_2 to reduce the impact of source-to-drain tunneling currents in black phosphorous metal-oxide-semiconductor FETs (MOSFETs), making subthreshold swing (SS) approach 60.2 mV/dec. Moreover, Choi *et al.* [18] designed hetero-gate-dielectric tunnel FETs to improve on-state current (I_{on}) (~30%) and suppress ambipolar behavior. The hetero-gate-dielectric structure also enhances the I_{on} of the gate-all-around tunnel FETs [19]. Therefore, dielectric engineering can enhance the gate control ability to improve the I_{on} and reduce leakage current in FETs.

Gallium selenide (GaSe) [20, 21] is a stable p-type semiconductor with exceptional properties such as high carrier mobility and tunable energy bandgap [22]. Previously, GaSe showed field effect mobility of about 0.6 $cm^2 \cdot V^{-1} \cdot s^{-1}$, with the good on/off current ratios in the range of 10^4– 10^5 [23]. Furthermore, GaSe showed high 2D Young's modulus of about 819 ± 127 $N \cdot m^{-1}$ [24]. Based on such excellent characteristics, GaSe is a good candidate for nanoelectronic devices. Recent advances in

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GaSe open up new opportunities towards novel nanoelectronics devices. Chen *et al.* [25] believed that the "Mexican hat" shape valence band is suitable for FETs. The GaSe/graphene heterostructure interface possesses a controllable Schottky barrier, which is desirable in electronic devices [26]. In recent years, large area ultrathin layers of GaSe crystals were successfully synthesized on SiO_2/Si substrates by using micromechanical cleavage technique [27, 28]. The GaSe stacking patterns result in different energy bandgap and effective mass [29], which affects the transport performance. However, there is limited research on the role of the dielectric in GaSe FETs.

In this work, we choose GaSe as an example to illustrate the impact of dielectric engineering. We first study the relationship between the dielectric positions and transfer characteristics. In addition, we investigate the effect of four GaSe bilayer stacking patterns as channel on the transport properties in different dielectric environments. The outstanding results provide reasonable proposals for regulating 2D nanodevices by dielectric engineering.

2 Computational details

For 2D bilayer GaSe, the geometrical optimization and electronic properties are computed with the Vienna *ab initio* simulation package (VASP) code [30–33]. Exchange correlation energies are described by the generalized gradient approximation (GGA) using the Perdew–Burke–Ernzerh (PBE) function [34]. The force tolerance on each atom is less than 10^{-2} eV/Å, and the converged energy is less than 10^{-5} eV. A 500 eV plane wave cutoff energy and a 13 × 13 × 1 Monkhorst–Pack *k*-point grid are chosen for geometrical optimization. The vacuum region of 20 Å is added to avoid interaction with the adjacent periodic structure.

The device performance is simulated in Atomistix Toolkit (ATK) [35–37] package. Ballistic transport properties are calculated by coupling the density-functional theory (DFT) and the nonequilibrium Green function (NEGF) methods. The exchange-correlation function uses the GGA in the form of PBE, and an additional Grimme DFT-D3 function [38–42] is used to correct the weak van der Waals interactions. The norm-conserving pseudopotential and the basis set are PseudoDojo and Medium, respectively. The electrostatic potential is treated by solving the Poisson equation self-consistently via a real space solver with the "multi-grid" type. We set the cutoff to 110 Hartree, the *k*-point grid to 1 × 15 × 250 and the temperature to 300 K. Finally, the periodic, Neumann and Dirichlet boundary conditions are used along the transverse, perpendicular and transport direction of the GaSe plane [43, 44]. The self-consistent calculation is performed until the energy and force converge to 10^{-5} eV and 0.01 eV/Å, respectively. We use the Landauer–Büttiker formula [45–48] to calculate the drain current at a certain bias and gate voltage:

$$I\left(V_{\mathrm{ds}}, V_g\right) = \frac{2e}{h}\int \left\{T\left(E, V_{\mathrm{ds}}, V_{\mathrm{g}}\right) \cdot \left[f_{\mathrm{S}}\left(E-\mu_{\mathrm{S}}\right) - f_{\mathrm{S}}\left(E-\mu_{\mathrm{D}}\right)\right]\right\} \mathrm{d}E,$$

where $T\left(E, V_{\mathrm{ds}}, V_{\mathrm{g}}\right)$ is the transmission coefficient at the given V_{ds} and V_{g}. The $f_{\mathrm{S/D}}$ and $\mu_{\mathrm{S/D}}$ are the Fermi–Dirac distribution functions and the Fermi level of the source or drain electrode.

3 Results and discussion

3.1 Transmission direction and doping concentration test

Before investigating the effect of the dielectric engineering on the device performance, we first explore the role of concentration and transmission direction on device performance. Figure 1(a) presents the double gate (DG) device schematic of MOSFETs based on bilayer GaSe, in which gate dielectric architecture is broken into four portions to control the dielectric layer. The length and thickness of the dielectric are 2.5 and 0.5 nm, respectively. Also, the *p*-doped bilayer GaSe is used as the source (S) and drain (D), the channel is an intrinsic bilayer GaSe and band structure is illustrated in Fig. 1(b). It possesses an indirect gap of about 1.50 eV, as well as the conduction band minimum (CBM) and valence band maximum (VBM) are located at the Γ point and between the Γ and M points, respectively, which is consistent with the report [49]. The valence band has a "Mexican hat" edge shape, which facilitates the generation of high density of states (DOS). The band structure of GaSe exhibits the typical "Mexican hat" shape at the top of the valence band, resulting in a high density of states (DOS) [50, 51]. The "Mexican hat" shape of the valence band edge leads to sharp peaks in the density of states [21]. In Fig. 1(c), we show the transfer characteristic curves (I_{ds}–V_{g}) of DG MOSFETs at different doping concentrations along armchair (Arm) and zigzag (Zig) directions, where the gate insulators are SiO_2, bias voltage is 0.64 V and the gate length (L_{g}) is 5 nm. The leakage current in the off-state region obviously decreases from 10^{-2} to 10^{-4} μA/μm with the decline of doping concentration. Especially, the I_{ds}–V_{g} of both directions are similar.

From the I_{ds}–V_{g}, we can obtain the key figures of merit, shown in Figs. 1(d)–(f). The I_{on} is obtained from the transfer characteristic curves at on-state gate voltage $V_{\mathrm{on}} = V_{\mathrm{off}} - V_{\mathrm{ds}}$, where the V_{ds} is the bias voltage. According to the high-performance (HP) standard of the International Technology Roadmap for Semiconductors (ITRS) 2028 Version [52], the V_{off} is defined by the off-state current (I_{off}) at 0.1 μA/μm. When the doping

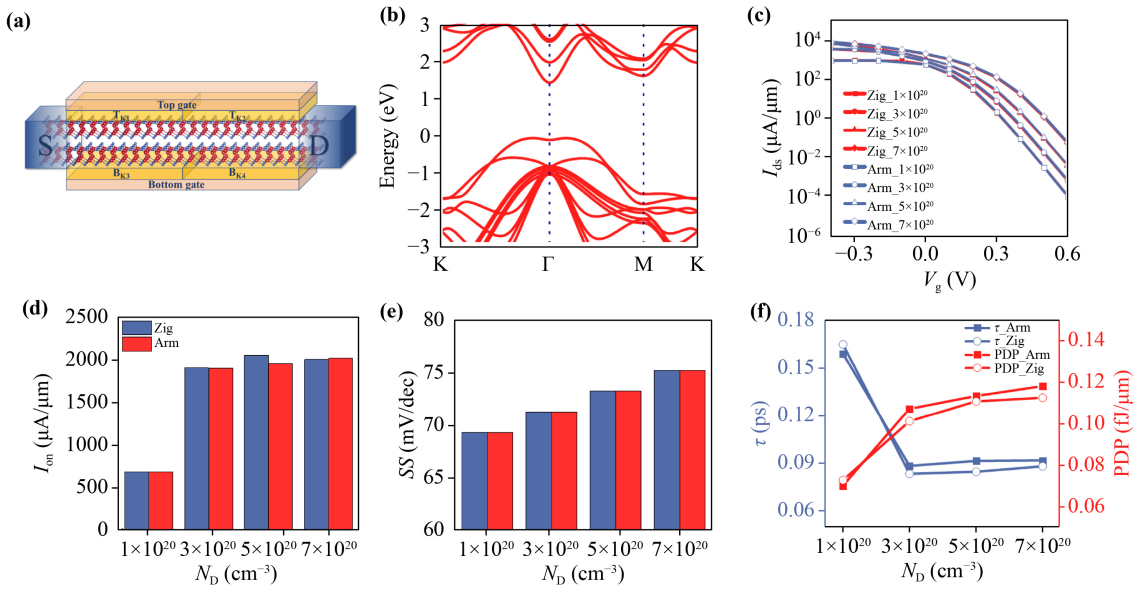

Fig. 1 **(a)** Structure diagram of the double gate MOSFETs. **(b)** Band structure of bilayer GaSe. **(c)** Transfer characteristic curves. **(d–f)** I_{on}, SS, τ and PDP of the devices with dielectric constants of 3.9 under V_{ds} = 0.64 V. The Arm, Zig, and N_D denote armchair direction, zigzag direction, and doping concentration, respectively.

concentration changes from 1 × 10^{20} to 3 × 10^{20} cm^{-3}, the I_{on} increases rapidly. However, when the concentration is greater than 3 × 10^{20} cm^{-3}, the I_{on} fluctuates around 2000 μA/μm. To describe the gate control ability of devices, *SS* is defined as the required gate voltage to change the current by one decade and can be expressed by $SS = \partial V_g/\partial \lg I_{ds}$. With doping concentration increasing, *SS* changes from 69 to 75 mV/dec and the gate control capability deteriorates. Moreover, intrinsic delay (τ) and power dissipation product (PDP) are much lower than 0.423 ps and 0.24 fJ/μm, which are the HP standards of ITRS. Thus, in terms of two-direction comprehensive performance, we finally choose the armchair direction as the transport direction and 5 × 10^{20} cm^{-3} as the doping concentration of the source and the drain to further study the role of high-*k* dielectric engineering.

3.2 The effect of high-*k* dielectric position

In order to assess the effect of high-*k* dielectric position on the device performance, we construct hetero-gate-dielectric structures in Fig. 1(a), and can be divided into two structures. For the type-A structure in Fig. S1, different dielectric materials are used for the top and bottom insulators, respectively. For type-B structure in Fig. S1, transverse dielectric is divided equally into two parts, and dielectric material are not the same. In order to concisely state the characteristics of the two structures, the dielectric positions are coded in the order of $T_{K1,\ K2}B_{K3,\ K4}$, where Ki (i = 1, 2, 3, 4) represents the dielectric position. The high-*k* dielectrics of Al_2O_3, and HfO_2 are chosen for the simulation, in addition, the air dielectric is considered for comparison. When the dielectric material is air, Al_2O_3, and HfO_2, K(i) = 0, 1, and 2, respectively. The gate length is set to 5 nm, and the doping concentration is 5 × 10^{20} cm^{-3}.

To compare the transport performance of devices, we plot the I_{ds}–V_g of type-A structures in Fig. 2(a). The device with higher dielectric constant has a lower leakage current and higher I_{on}. In addition, Figs. 2(b) and (c) display the I_{on} and on/off-state current ratio (I_{on}/I_{off}). The I_{off} is defined by V_{off}, which is obtained by scanning from 0.1 to 0.6 V with a step size of 0.1 V. The I_{on} of the MOSFETs with the $T_{11}B_{22}$ and $T_{22}B_{11}$ structures reach 4580 and 4614 μA/μm, respectively, far exceeding the ITRS standard. However, the value is lower than HfO_2 (5084 μA/μm) and higher than Al_2O_3 (3936 μA/μm) as the dielectric, which are improved comparing with the situation of SiO_2 in Fig. 1. The I_{on}/I_{off} of these four devices is close to 10^8 together with I_{on} close to 10^3 μA/μm, and has similar change as I_{on}. The same transmission performance of $T_{22}B_{11}$ and $T_{11}B_{22}$ structures implies that device performance is independent of the position of the top and bottom dielectric. Hence the device can achieve excellent performance and reduce the difficulty of experimental production when employing high-*k* material at the bottom insulator.

Figure 2(d) presents the transfer characteristic curves of type-B structure. For the asymmetric structure, the device is able to obtain a lower leakage current when the insulator with a larger dielectric constant is used on the drain side. We extract the I_{on} and I_{on}/I_{off} shown in Figs. 2(e) and (f). The I_{on} of the device with $T_{12}B_{12}$ structure is approximately 5052 μA/μm, while that with

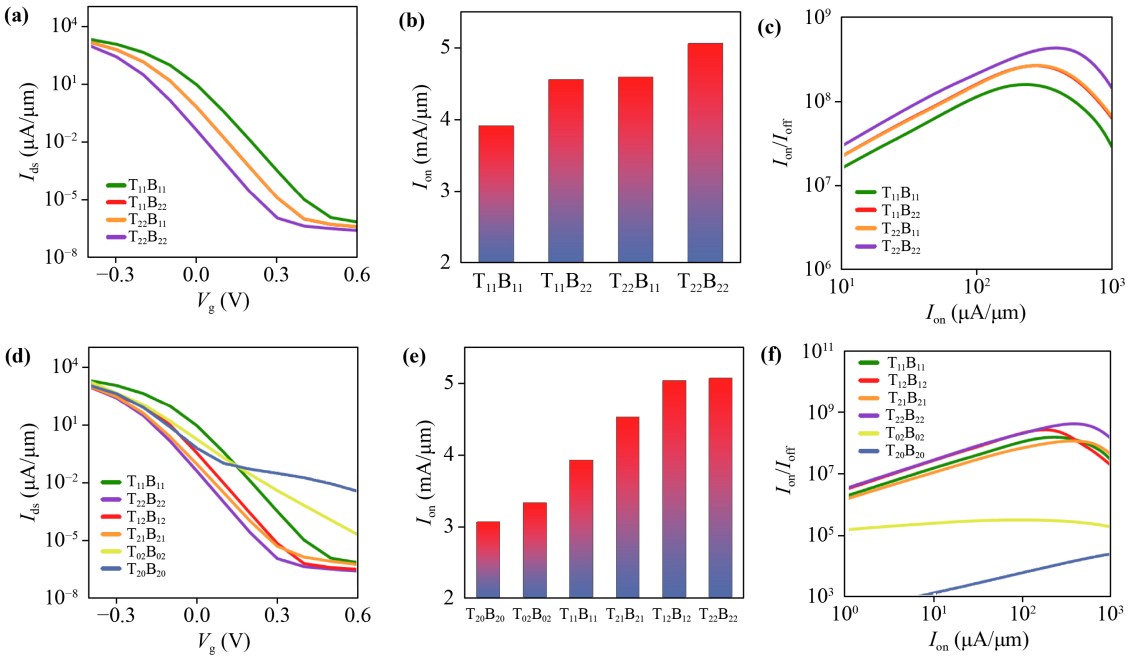

Fig. 2 The **(a–c)** I_{ds}– V_g, I_{on}, and I_{on}/I_{off} of the MOSFETs with L_g = 5 nm for type-A structure, the **(d–f)** for type-B structure.

$T_{21}B_{21}$ construction only reaches 4538 μA/μm. The I_{on}/I_{off} of MOSFETs with $T_{12}B_{12}$ structure behaves excellently compared to that of $T_{21}B_{21}$ construction. Similar phenomena can also be found in $T_{02}B_{02}$ and $T_{20}B_{20}$ devices. This shows that the device has better performance when the high-k gate dielectric is located close to the drain side, and this architecture is more suitable for making high-performance electronic devices.

To clearly illustrate the mechanism between gate dielectric position and device performance, the projected local density of states (PLDOS) and spectral current are plotted in Figs. 3(a, b) and (d, e). The effective barrier height (Φ_h) represents the energy barrier between the maximum value of the channel VBM and the source Fermi energy level. Additionally, spectral current consists of tunneling current (I_{tunnel}) and thermionic current (I_{therm}), which is separated by the Φ_h. As can be seen from Fig. 3(a), the Φ_h of the device with $T_{22}B_{22}$ structure is 0.19 eV in the off-state, and I_{tunnel} is hardly generated. Figure 3(b) presents that the barrier heights of the Al_2O_3 (Φ_{hs}) and HfO_2 (Φ_{hd}) part are 0.13 and 0.23 eV, respectively. In the on-state, the VBM shifts upward and enters the bias window for both structures, resulting in the disappearance of the barrier. Thus, the I_{therm} completely dominates the total spectral current, which is comparable for both structures. Different dielectrics are used on the left and right sides for the device with $T_{12}B_{12}$ constructions, the VBM moves up different distances in different regions. Therefore, the I_{on} of the MOSFETs with $T_{22}B_{22}$ and $T_{12}B_{12}$ structures are almost equal, indicating that high-k materials can be saved while maintaining performance.

We plot the valence band profiles of the device in Figs. 3(c) and (f) to explain the better performance of the high-k materials close to the drain than the source. When the gate voltage is −0.2 V, both structures in Fig. 3(c) have similar barrier heights, but the width of the $T_{12}B_{12}$ structure is significantly smaller, which makes the current larger. In Fig. 3(f), the barrier of the MOSFETs with $T_{02}B_{02}$ structure disappears, but that with the $T_{20}B_{20}$ construction still exists. Therefore, when the high-k material is close to the drain side, the gate has stronger electrostatic control of the channel and better performance. Additionally, when the gate voltage is applied to 0.4 V (off-state), there is almost no difference in barrier height, but an obvious distinction in barrier width. In Fig. 3(f), the device with $T_{20}B_{20}$ structure only has a barrier close to the source, while the MOSFETs with $T_{02}B_{02}$ construction has a barrier close to both the drain and source, thus it can better suppress carrier tunneling and achieve a lower drain current.

3.3 The high-k dielectric on devices with different stacking pattern channel

The dielectric location can have a large impact on the device performance, but the effect of the high-k dielectric on devices with different stacking pattern channel needs further investigation. The $T_{22}B_{22}$ structure is chosen and SiO_2 insulator is used to compare with case of high-k dielectric. Figure 4(a) displays the I_{ds}–V_g of the MOSFETs based on the bilayer GaSe with AA, AB, AC,

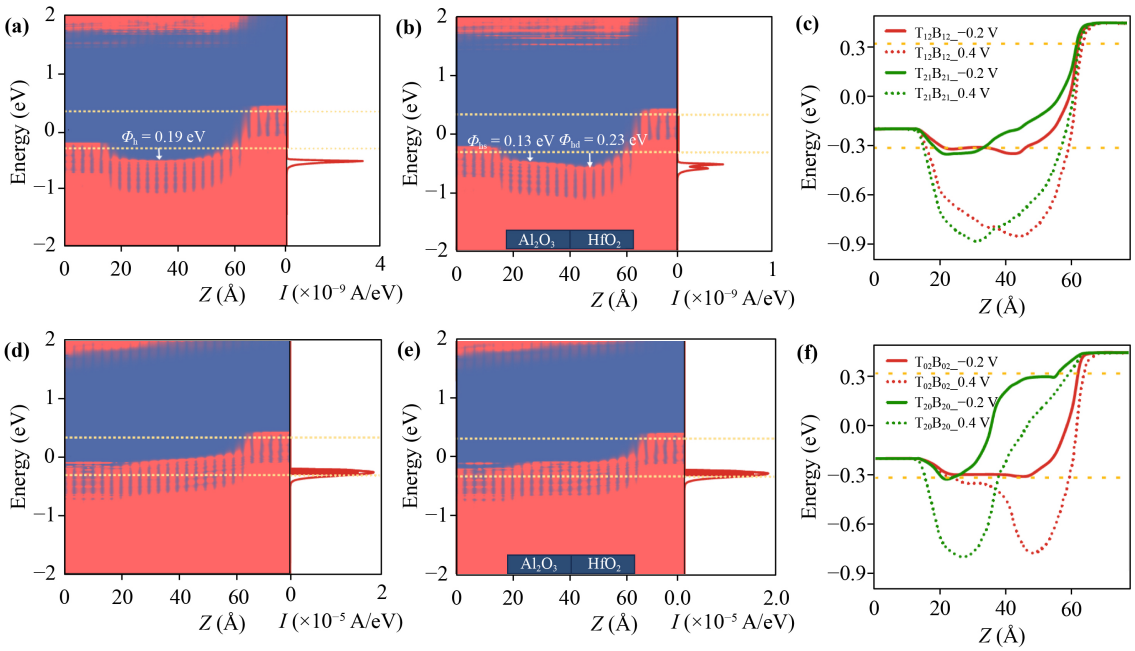

Fig. 3 The PLDOS and spectral current of the $T_{22}B_{22}$ and $T_{12}B_{12}$ devices at **(a, b)** off-state and **(d, e)** on-state under V_{ds} = 0.64 V. The light red area indicates the spectral current in the bias window, and the yellow dashed area indicates the bias window. The **(c)** and **(f)** valence band profiles of devices at different gate voltages when V_{ds} = 0.64 V.

and AD stacking patterns. The stacking orientations and corresponding band structures are presented in Figs. S2 and S3. Table S1 lists the detailed structural parameters. The insets of Fig. 4(a) show the enlarged curves for all stackings between V_g = 0.2 V and V_g = 0.3 V. When HfO_2 dielectric is used, the difference in the transport performance of the devices with four structures is more obvious, especially in the off-state region. When using SiO_2 as dielectric, the stacking orders have little effect on device performance, and the largest difference of the I_{on} between devices with AA and AB stacking is only 349 μA/μm. Thus, the stacking patterns have a great impact on device performance when using HfO_2 as dielectric, the difference of the I_{on} between MOSFETs with AA and AC stacking is the largest (1111 μA/μm), which is larger than the SiC [53]. Furthermore, this result can be found from the V_{off} of the devices with four stacking patterns, as shown in Fig. 4(c). When SiO_2 is used, the V_{off} fluctuates slightly around 0.49 V, while it fluctuates obviously around 0 V for HfO_2 dielectric. These results show that when high-k dielectric is used to improve device performance, the choice of channel stacking pattern should be paid attention to.

To gain insight into the above observations, in Figs. 4(b) and (d), the transmission spectra of devices with different insulators and four stacking patterns are depicted at the gate voltage of 0.2 and –0.2 V. Regardless of the gate voltage of 0.2 or –0.2 V, the difference between the VBM of MOSFETs with four stacking is smaller for SiO_2 than that of HfO_2 dielectric. And with the gate voltage changing from positive to negative, the difference between the VBM of devices with four stacking at high-k will become small. In addition, when V_g changes from 0.2 to –0.2 V, the VBM of high-k shifts about 0.3 eV to the right, while it changes about 0.2 eV for SiO_2. It indicates that when high-k insulator is used, device has better gate control capability. When V_g = –0.2 V, the VBM of the device with AA stacking pattern and SiO_2 dielectric appears to be farther away from the Fermi level. The I_{on} (1605 μA/μm) of MOSFETs with AB stacking is lower than the other three structures (1954, 1879, 1691 μA/μm correspond to AB, AC, AD stackings), while all the devices meet the HP standard of IRTS, but are below the case of high-k. Thus, it is necessary to choose the appropriate stacking order when high-k dielectric is used for MOSFETs to improve performance.

3.4 Scaling of the gate length

Device performance with AA and AB stacking patterns is chosen for different gate length to investigate the role of dielectrics in size scaling. Figures 5(a)–(c) and S4 display the transfer characteristic curves of the device. When the L_g is reduced from 6 to 4 nm, the minimum leakage currents of the devices with AA and AB stacking increase by approximately 3 orders of magnitude for the HfO_2 dielectric, which is 2 orders of magnitude larger than the case for the SiO_2 dielectric. Thus, the lower leakage current can be obtained in the off-state region by using high-k dielectric. Additionally, when L_g is reduced to 2 nm, the device performance degenerates

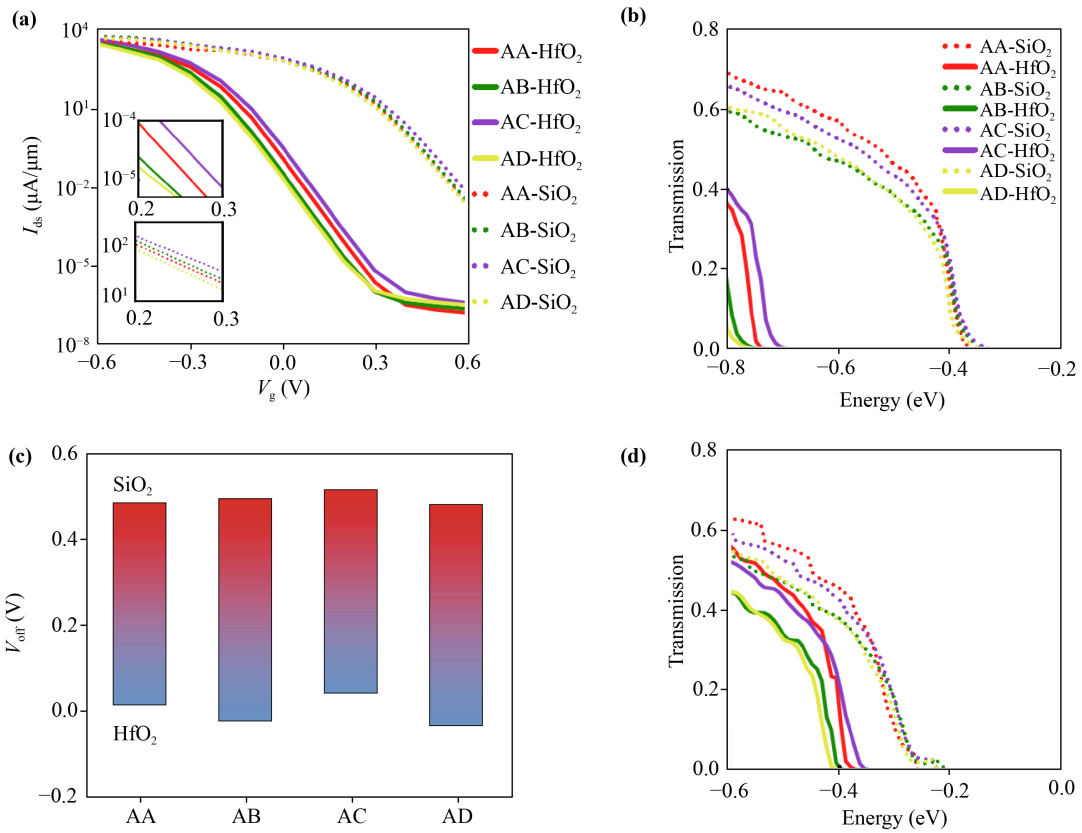

Fig. 4 **(a)** The I_{ds}–V_g of MOSFETs with different stackings under L_g = 5 nm. The inserts are for the enlarged curves between V_g = 0.2 V and 0.3 V. The transmission spectra of bilayer GaSe under V_{ds} = 0.64 V with **(b)** V_g = 0.2 V and **(d)** V_g = –0.2 V. **(c)** The V_{off} of the devices with SiO_2 and HfO_2 insulators under different stacking patterns.

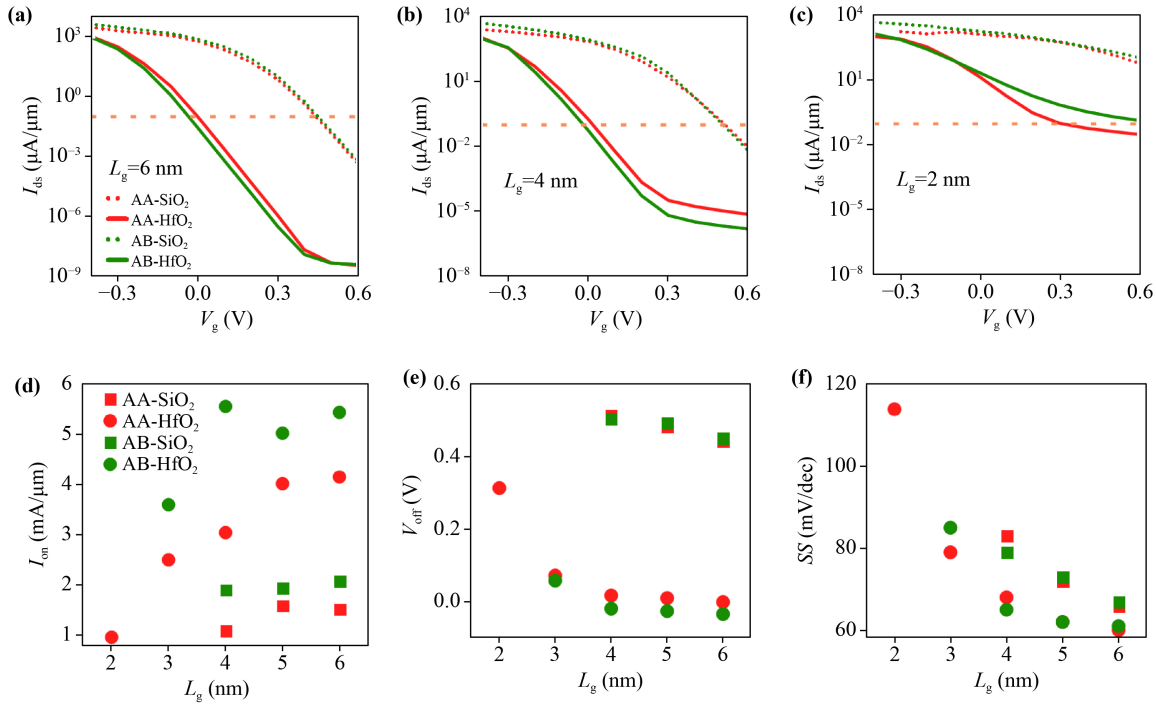

Fig. 5 The I_{ds}–V_g of devices with SiO_2 and HfO_2 dielectric for AA and AB stackings at **(a)** L_g = 6 nm, **(b)** 4 nm and **(c)** 2 nm. **(d–f)** The I_{on}, V_{off} and SS of the devices for different L_g.

drastically and is difficult to reach the off-state.

Figures 5(d) and (e) present the I_{on} and V_{off} in different dielectric environments. When L_g is 6 nm, the I_{on} of device with high-k insulator reaches 270% (260%) of that with SiO_2 dielectric for AA (AB) stacking pattern, and the other L_g devices behave similar phenomenon. Moreover, Fig. 5(d) also shows that whatever the size is, stacking pattern has more obvious effects on the I_{on} when high-k dielectric is used. At 4 nm, the I_{on} difference for the MOSFETs with the HfO_2 dielectric is about 2509 μA/μm, while it is only 813 μA/μm for SiO_2. A similar phenomenon also is found in off-state in Fig. 5(e). At the same time, the switching characteristics of the device are also discussed. Figure 5(f) also shows the SS of devices with AA and AB stacking at different L_g. When HfO_2 is used as an insulator and L_g is 4 nm, the SS is close to the limit of 60 mV/dec at room temperature, which shows better gate control ability compared to that of SiO_2. When the L_g is less than 3 nm, the short channel effect is more severe and the SS increases sharply, approaching 114 mV/dec for AA stacking. The difference of SS and I_{on} between MOSFETs with AA and AB stackings for $L_g = 6$ nm (4 nm) is 1 (4) mV/dec and 550 (813) μA/μm, respectively. The results show that high-k dielectric is more favorable for size reduction and excellent performance.

In consideration of the HP standard of ITRS, the L_g of the device with AA stacking can be reduced to 2 nm and I_{on} is close to 978 μA/μm when high-k dielectric is used. While the L_g of the device with AB stacking is reduced to 3 nm, the I_{on} is up to 3604 μA/μm. Additionally, for AA or AB stacking devices with SiO_2 dielectric, the L_g is only reduced to 4 nm considering the ITRS 2028 standard. The AA stacking is superior in the preparation of ultra-short channel MOSFETs in a high-k dielectric environment.

4 Conclusions

In summary, we have explored the theoretical quantum transport properties of bilayer GaSe MOSFETs, considering the impact of the gate dielectric location on device performance. The device behaves best performance when the high-k dielectric is placed close to the drain. This is mainly attributed to better control over the channel when the position of high-k material is near the drain. Moreover, stacking and dielectric environments have a great influence on device performance. The largest I_{on} difference is about 1111 μA/μm under high-k dielectric. The device holds the I_{on} about 978 μA/μm when L_g = 2 nm for AA stacking. This work indicates that the dielectric environment is closely related to device performance and provides an effective direction for dielectric engineering applications.

Declarations The authors declare that they have no competing interests and there are no conflicts.

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