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HfAlO-based ferroelectric memristors for artificial synaptic plasticity

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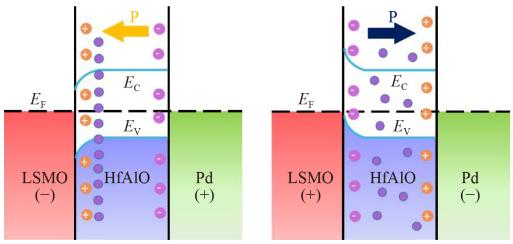
ABSTRACT

Memristors have received much attention for their ability to achieve multi-level storage and synaptic learning. However, the main factor that hinders the application of memristors to simulate neural synapses is the instability of the formation and breakage of conductive filaments inside traditional memristors, which makes it difficult to simulate the function of biological synapses in practice. However, the resistance change of ferroelectric memristors relies on the polarization inversion of the ferroelectric thin film, thus avoiding the above problem. In this study, a Pd/HfAlO/LSMO/STO/Si ferroelectric memristor is proposed, which can achieve resistive switching properties through the combined action of ferroelectricity and oxygen vacancies. The *I*–*V* curves show that the device has good stability and uniformity. In addition, the effect of pulse sequence modulation on the conductance was investigated, and the biological synaptic function and learning behavior were simulated successfully. The results of the above studies provide a basis for the development of ferroelectric memristors with neurosynaptic-like behaviors.



Keywords memristor, ferroelectric domain polarization, resistance regulation, artificial synapse

1 Introduction

With the rapid expansion of data and information, modern computers based on von Neumann architecture are facing severe challenges [1]. The storage and flexible processing of intelligent computers are the direction of future computer development. Due to the "storage wall bottleneck" in the "von Neumann architecture", existing computing platforms cannot efficiently implement related algorithms, and power consumption becomes a limiting factor [2]. In contrast, the human brain can

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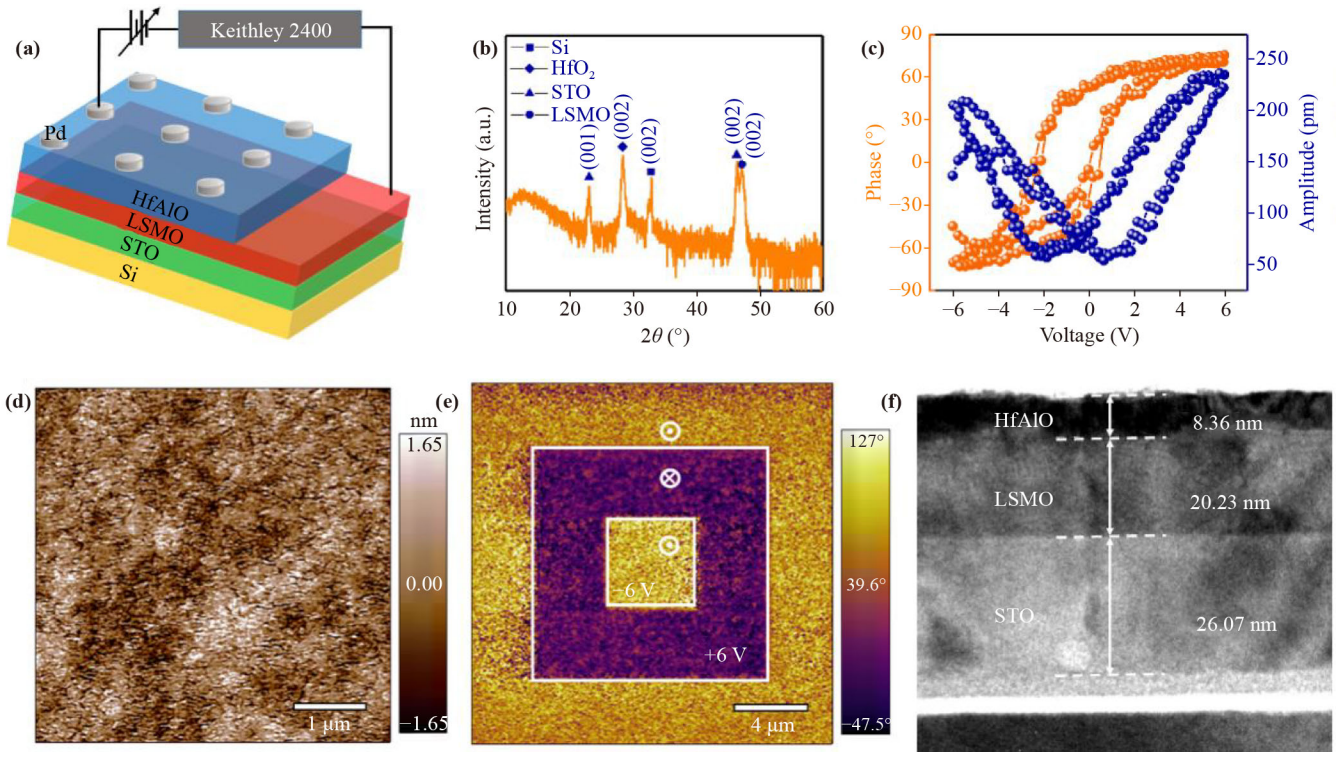

Fig. 1 **(a)** The Pd/HfAlO/LSMO/STO/Si device structure diagram. **(b)** XRD diffraction patterns of HfAlO (6.5% Al). **(c)** PFM hysteresis loop. **(d)** Morphology scans of HfAlO films grown on p-Si substrates in the 20 μm × 20 μm region. **(e)** PFM phase images. **(f)** TEM images.

complete various learning tasks quickly with low power consumption. There are about 100 billion neurons in the human brain, and each neuron is connected by thousands of synapses to form a complex neural network [3]. The synapses of the human brain can perform memory and calculation at the same time, which is obviously different from the "von Neumann architecture". The memristor can realize storage and calculation at the same time which is considered to be the most potential electronic synaptic device [4]. By applying voltage at both ends of the device, the resistance state can be flexibly changed, so as to realize the plasticity of the synapse. In addition, the memristor also has the advantages of small size, low operating power consumption, large-scale integration, and so on [5–7]. Therefore, the brain-like computing hardware system based on memristor has become an international research hotspot. However, the formation and breakage of conductive filaments inside conventional memristors is unstable. Therefore, it is difficult to truly mimic the function of biological synapses [8]. This problem has become a major obstacle to the application of memristors to simulate neurosynapses.

Ferroelectric memristors overcome the drawbacks of conventional memristors because their resistance changes depending on the polarization flip of the ferroelectric film. So far, many ferroelectric memristors with metal oxide materials have been reported, and it has been found that resistive random access memories with moderate doping of metals such as Y, Gd, and Zr with HfO_2 have more significant ferroelectric properties [9–15]. Among them, HfAlO ferroelectric films have excellent ferroelectricity and are compatible with CMOS processes, offering great potential for ferroelectric memories [16–20].

In this work, we fabricated a 6.5% Al-doped HfAlO ferroelectric memristor on p-type Si substrate. We investigated its I–V switching characteristics and the effect of pulses with different parameters on the conductance of the device. The high-to-low (R_{OFF}/R_{ON}) resistance ratio of the device is about 10, which can well mimic synaptic learning behavior. This research lays the foundation for the development of ferroelectric memristors with neurosynaptic-like behaviors.

2 Experiment

The schematic diagram of the device Pd/HfAlO/LSMO/STO/Si structure is shown in Fig. 1(a). First, pulsed laser deposition (PLD) was used to grow $SrTiO_3$ (STO) on the p-Si substrate as a buffer layer. Next, a $La_{0.67}Sr_{0.33}MnO_3$ (LSMO) layer was deposited on the STO layer as the bottom electrode. Subsequently, the HfAlO ferroelectric functional layer film was grown at 700 °C with 6.5% Al doping. Finally, a Pd layer with a thickness of 10 nm and a diameter of 90 μm was

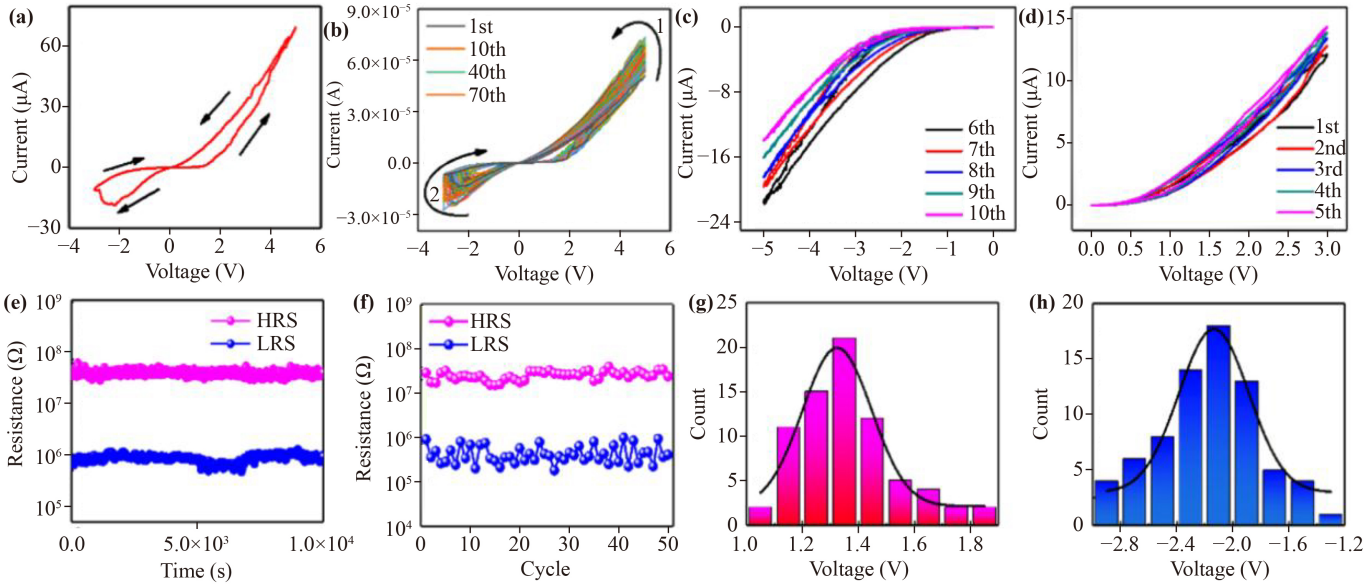

Fig. 2 **(a)** Current-voltage sweep. **(b)** Voltammetry curves of 100 scan cycles. **(c, d)** Five consecutive sweeps of negative voltage of 0 V → –5 V → 0 V and positive voltage of 0 V → 3 V → 0 V in DC mode. **(e)** HRS and LRS plots versus time. **(f)** HRS and LRS hold for 50 turns. **(g, h)** Switching voltages of the devices.

deposited as the top electrode on the surface of the device by magnetron sputtering. LSMO has several excellent properties that motivated us to use it as a bottom electrode. The LSMO bottom electrode has higher self-resistance compared with the traditional metal bottom electrode, which can be used as a series resistor to provide a compliance current, thus simplifying the device structure [21]. Meanwhile, the reset process can be performed at a low current, thereby reducing the power consumption of the device. More importantly, high quality LSMO epitaxial growth can be achieved by growing an STO buffer layer on Si [22], which provides an epitaxial template for the HfAlO functional layer to ensure its good ferroelectric properties [23]. Figure 1(b) shows the XRD diffraction pattern of the device. It can be seen from the figure that the film has an obvious diffraction peak at 28.25°, which is consistent with the results reported in the literature [24]. This peak matches the o(002) structure of the orthorhombic Pmnb [25]. Figure 1(c) is the PFM hysteresis loop, which shows the ferroelectric properties of the HfAlO film. It can be clearly observed from the figure that the coercive voltage of the sample is about –2 V and 0.6 V. The morphology and ferroelectric properties of HfAlO samples grown at 700 °C were characterized by atomic force microscopy (AFM). The morphological scan of the sample in the area of 10 μm × 10 μm is shown in Fig. 1(d). It can be observed that the entire surface of the film is relatively flat. The PFM phase image is shown in Fig. 1(e). When a bias voltage of +6 V is applied to the device, the HfAlO film is polarized downward. When a –6 V bias is applied, the HfAlO film is polarized upward. The phase contrast of 174.5° shows that the polarization of the two regions is antiparallel through the reversal of the ferroelectric domain under the electric field. The PFM amplitude mapping and P–V loop of the device are shown in Fig. S2 of the Electronic Supplementary Materials (ESM). Figure 1(f) shows the transmission electron microscope (TEM) image of the device. The thicknesses of each layer of HfAlO/LSMO/STO are about 8.36 nm, 20.23 nm, and 26.07 nm, respectively.

3 Results and discussion

In order to investigate the resistance switching effect of the memristor, the I–V curves of the memristor were tested. The current–voltage (I–V) characteristics of the Pd/HfAlO/LSMO/STO/Si memristor were obtained by applying a direct current (DC) voltage to the Pd top electrode while grounding the LSMO bottom electrode, as shown in Fig. 1(a). When the programming voltage sweep was set as 0 V → 3 V → 0 V → –5 V → 0 V, the resistance values were reversibly changed from high-resistance state (HRS) to low-resistance state (LRS) through RESET and SET processes. The I–V curve can repeat 70 cycles of sweeping, showing that the device has good repeatability and uniformity. More importantly, the HRS of the device is an order of magnitude larger than the LRS, showing excellent resistance-change characteristics. To further demonstrate the progressive tuning of the conductance in the DC mode, the device is subjected to five consecutive DC voltage sweeps. The current of the device gradually decreases with the scan period during five consecutive negative voltage sweeps from 0 to –5 V, as shown in Fig. 2(c). The current of the

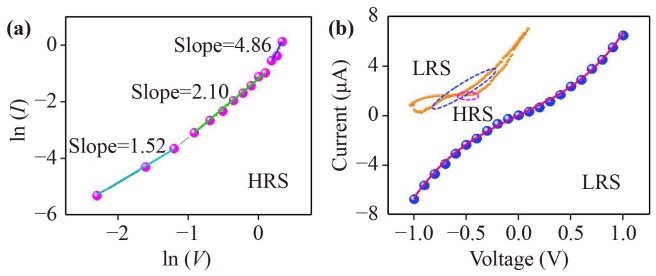

Fig. 3 **(a)** According to the HRS partial I–V curve fitting results, the conduction mechanism corresponds to the SCLC model. **(b)** The LRS partial I–V curve can be fitted to the $I = A\sinh(BV)$ function, where the fitting constants are $A = 2.32$ and $B = 1.79$, respectively. The inset is a typical I–V curve of a Pd/HfAlO/LSMO/STO/Si device.

device gradually increases with the scan period during five consecutive positive voltage sweeps from 0 to 3 V, as shown in Fig. 2(d). The retention properties of HRS and LRS are shown in Fig. 2(e). It can be found that the retention time can last 10^4 s without degradation at the bias voltage, indicating that the device has good retention properties. The HRS and LRS of the 50 cycle tests fluctuated in small ranges, as described in Fig. 2(f). It can be seen that the HRS/LRS ratio is always larger than 10, showing good resistance-to-variation characteristics. The high-resistance and low-resistance states of the device also provide strong support for simulating the process of stimulation and inhibition of synaptic information transfer. In addition, the 70-cycle I–V curves of the memristor was analyzed by statistical and Gaussian fitting, as shown in Figs. 2(g) and (h). It can be seen that the device turns on in the voltage range of 1.0–1.9 V (concentrated at 1.3 V) and turns off in the voltage range of –3 – –1.2 V (concentrated at –2.1 V).

In the study, the I–V properties were fitted to understand the conduction mechanism and further explain its physical mechanism. Ferroelectricity and semiconducting properties induce ferroelectric resistive switching (FE-RS) effects, which can be explained by some models [26]. To better understand the resistive switching behavior of the device, the $\ln I$–$\ln V$ linear fitting curve is shown in Fig. 3(a). In the low voltage region, a small amount of electrons are injected into the trap, and the current and voltage satisfy the relationship of ohmic conduction ($I \sim V$). As the voltage increases, the slope of the HRS changes from 1.52 to 2.10, which can be explained by the increasing number of injected electrons filling the trap, at which point the relationship between current and voltage satisfies Child's law ($I \sim V^2$) [27, 28]. Then, the slope becomes 4.86, indicating a dramatic increase of electrons injected in the high voltage region where the current increases exponentially. Therefore, the SCLC model may be applicable to our observations, which is consistent with the conclusions of related reports [29–32]. As shown in Fig. 3(b), the I–V curve of the LRS part can be fitted as a function formula:

$$I = A\sinh(BV).$$

The fitting constants $A = 2.32$ and $B = 1.79$ are obtained in this paper. This functional relationship is consistent with the characteristics of the electron tunneling model [33]. Through further analysis, the width and height of the barrier can be found to be 0.76 nm and 0.29 eV, respectively.

Figures 4(a)–(c) show the variations of the memristor's current after stimulation with different numbers of pulses as well as different pulse amplitudes. In this case, both the pulse width and pulse interval are 500 ns. From the figures, it can be found that the pulse conduction of the device increases with increasing pulse amplitude for the same number of pulses. This is similar to the positive correlation between the speed of information transmission and the intensity of synaptic excitation. In addition, the pulse conduction gradually reaches a saturation value after several consecutive pulse stimulations. From a neuroscientific point of view, the characteristics of the device are consistent with synaptic phenomena, where synaptic learning is most pronounced in the early learning stage (that is, a small number of pulses are applied to the amnestic device) and the synaptic weight gradually saturates in the late learning stage (that is, a sufficient number of pulses are applied to the memristors). In the voltage scanning mode, the device conductance changes gradually rather than abruptly. In order to further verify the continuous tunability of the conductance of the memristor in the alternating current (AC) pulse mode, the controllability of the conductance tuning was investigated. First, the influence of the excitation pulse amplitude on the conductance of the device was investigated. As shown in Fig. 4(d), the pulse amplitude is increased from 3 V to 6 V. It can be found that the conductance of the memristor increases as the pulse amplitude increases when the pulse width and pulse interval are 500 ns and the pulse number is 40 cycles. This is similar to the positive correlation between the speed of information transmission and the intensity of synaptic excitation. Next, Fig. 4(e) illustrates the effect of different pulse intervals on the conductance. The amplitude of the programmed pulse is 6 V and the width is 500 ns. It is observed that the trend of the conductance changing with the pulse interval is opposite to the trend of the pulse amplitude. Finally, the effect of pulse width on conduction variation was investigated. Figure 4(f) shows the effect of pulse width on conduction at 6 V pulse amplitude and 500 ns pulse interval. The results show that the conductivity increases with increasing pulse width. This indicates that the duty cycle directly affects the conductance change of the memristor, as the continuous enhancement of the signal increases the synaptic weights. More importantly, the device conductance changes more rapidly with increasing

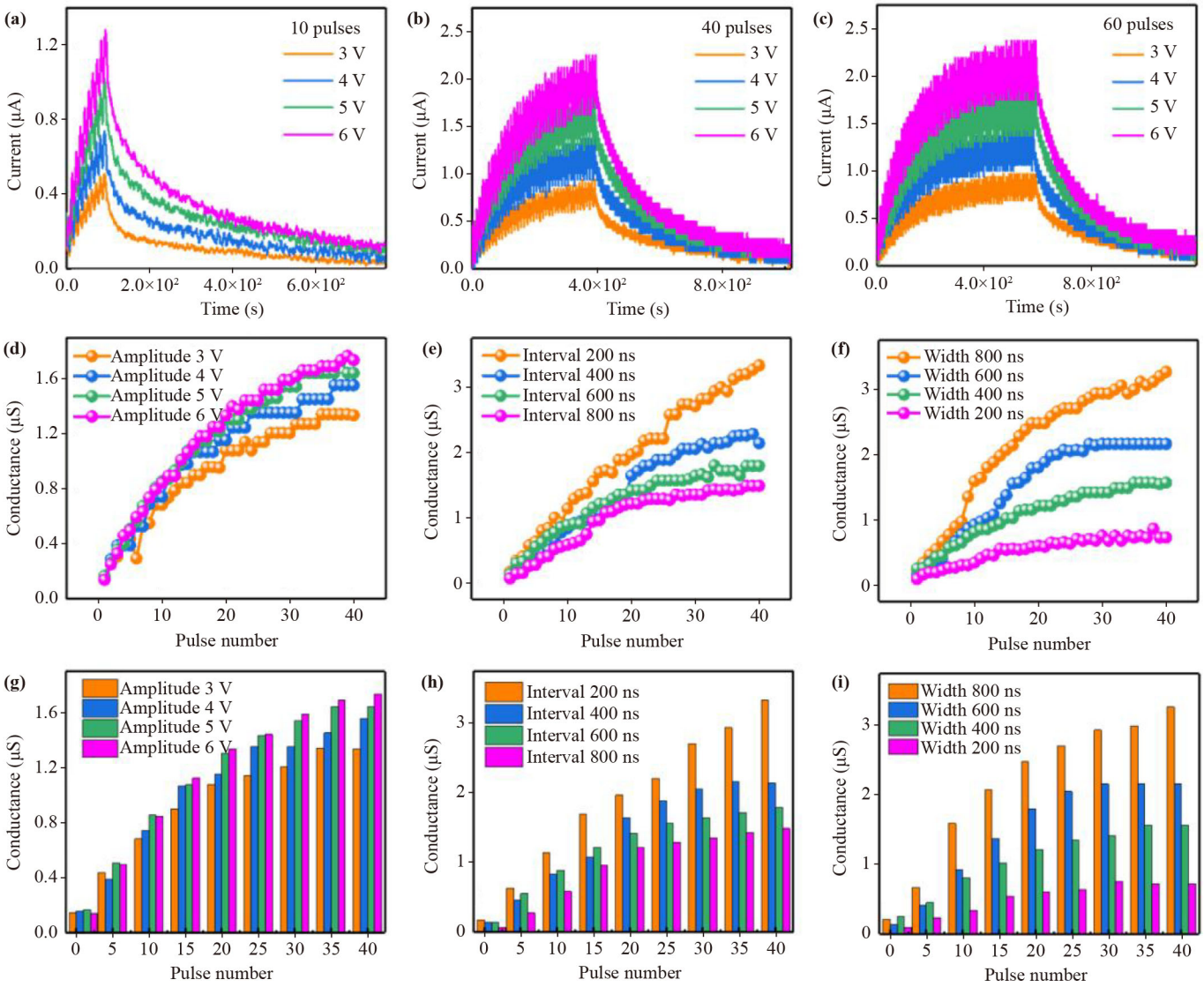

Fig. 4 Pulse tests of HfAlO ferroelectric memristor. **(a–c)** The current response of the memristor at different pulse numbers and different voltage amplitudes. **(d–f)** Measured device conductance with different pulse amplitudes, pulse intervals, and pulse widths. **(g–i)** Measured device conductance for 30 pulse cycles with (g) different pulse amplitudes, (h) different pulse intervals, and (i) different pulse widths, respectively.

pulse width. In short, the intensity, direction and duty cycle of the pulse stimulus all affect the device conductance, similar to the role of synapses in neural information transmission. In Figs. 4(g)–(i), it can be observed that the conductance increase rate strongly depends on the stimulation, and the conductance rises after each pulse. As shown in Fig. 4(g), at a fixed width and interval (both 500 ns), a higher amplitude will lead the conductance to rise faster. However, when the pulse interval is increased, the situation is just the opposite, as shown in Fig. 4(h). When the pulse width (500 ns) and pulse amplitude (6 V) are fixed, the wider the pulse interval, the slower the conductance change. In addition, Fig. 4(i) shows the effect of the pulse width on the rate of increase in conductance. It is found that the larger pulse width, the faster the change in conductance. Overall, the conductance of the device can be fine-tuned by the number, amplitude, interval and width of the pulses, which facilitates the simulation of biological synaptic function [34, 35].

The synaptic structure of a neuron is shown in Fig. 5. Hebbian theory describes the basic principle of synaptic plasticity, whereby sustained and repeated stimulation of a presynaptic neuron to a postsynaptic neuron can lead to an increase in synaptic transmission efficacy. In this work, spike-timing-dependent plasticity (STDP) and paired-pulse facilitation (PPF) learning rules of the device were investigated. According to the STDP learning rule, the presynaptic membrane is stimulated earlier than the postsynaptic membrane ($\Delta t > 0$), indicating

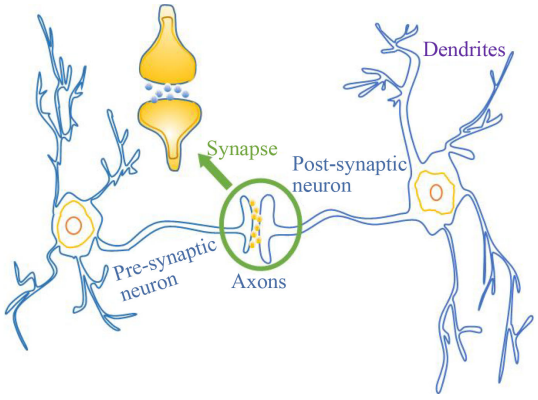

Fig. 5 Schematic representation of the synaptic structure of a neuron, including pre-synaptic, post-synaptic, cell and nucleus, axon and dendrite.

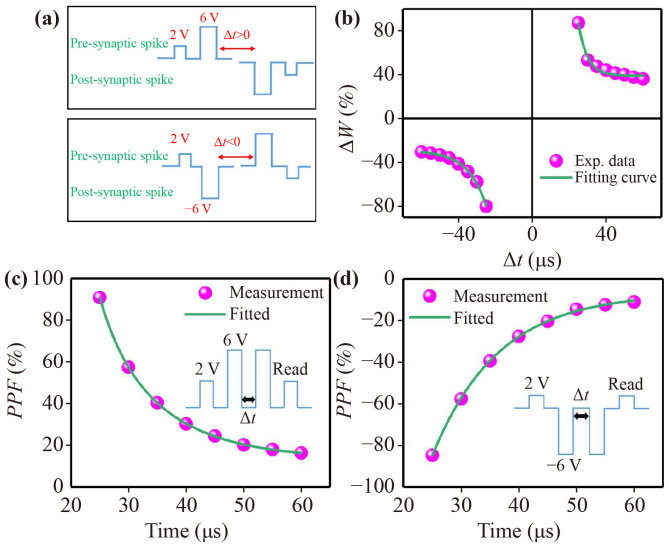

Fig. 6 **(a)** Waveforms of pre- and post-spikes for STDP measurements. **(b)** STDP characteristics of ferroelectric amnestic blockers. **(c, d)** *PPF* characteristic curves.

that the biological synaptic connection between the two neurons is enhanced, resulting in long-term plasticity (LTP). If the presynaptic membrane is stimulated later than the postsynaptic membrane ($\Delta t < 0$), the biological synaptic connection between the two neurons is weakened, resulting in long-term depression (LTD). The biological neuron consists of presynaptic and postsynaptic neurons, similar to the sandwich structure of the upper electrode-HfAlO layer-lower electrode of the memristor, as shown in the enlarged portion of Fig. 5. The resistance (or conductivity) of the device is equal to the weight of the synapse. An increase or decrease in conductivity corresponds to synaptic enhancement or suppression, respectively. The polarization of the HfAlO ferroelectric film will cause the resistance of the memristor to change, so the memristor can simulate the change of the weight of biological synapses.

Pre-synaptic and post-synaptic spikes were applied to the bottom and top electrodes of the device, respectively, a pair of ±6 V pulse waveforms were used to simulate presynaptic stimulation, and conductance values were read at 2 V, as shown in Fig. 6(a). Synaptic weights were adjusted by changing the pulse interval between pre- and post-synaptic peaks, as shown in Fig. 6(b). The change in synaptic weight (ΔW) is considered to represent a change in relative conductivity, which is defined as $\Delta W = (G_{\text{post}} - G_{\text{pre}})/G_{\text{pre}} \times 100\%$, where G_{post} and G_{pre} are the conductance before and after the pre- and post-spiking pairs, respectively. And the time difference between the postsynaptic pulse and presynaptic pulse (Δt) is expressed as $\Delta t = t_{\text{pre}} - t_{\text{post}}$. The change in synaptic weights will be more significant when $|\Delta t|$ approaches zero. The results indicate that as the stimulus interval decreases, the synaptic weight increases and the memory effect becomes more obvious. Synaptic weight increased ($\Delta W > 0$) when the neural stimulation signal from the presynaptic neuron was promoting the neural stimulation signal from the postsynaptic neuron ($\Delta t > 0$). As $|\Delta t|$ decreases, synaptic weight increases and the presynaptic neurostimulator signal plays a greater role. When the neurostimulator signal from the presynaptic neuron plays a role in suppressing the generation of neurostimulator signal from the postsynaptic neuron ($\Delta t < 0$), the synaptic weight decreases ($\Delta W < 0$). The change in synaptic strength for STDP modification is given by the mathematical equation:

$$\Delta W = \begin{cases} A_+ \times \exp(-t/\tau_+) + \Delta W_0, & \Delta t > 0 \\ A_- \times \exp(-t/\tau_-) + \Delta W_1, & \Delta t < 0 \end{cases},$$

where ΔW is the relative change in synaptic weights, A_+ and A_- are scaling factors, τ_+ and τ_- are time constants, and ΔW_0 and ΔW_1 are constants representing the uncorrelated components of synaptic change. The STDP can be successfully fitted using the above exponential function by varying the pulse interval (i.e., varying t). The fitting results are $A_\pm$ = 1.27/–6.49, $\tau_\pm$ = 6.49/–15.86.

Another important synaptic learning rule is the *PPF*. The intensity of the output pulse signal increases as the interval between paired input pulse excitations decreases. As shown in Figs. 6(c) and (d), the equation for calculating the *PPF* is

$$PPF = \frac{G_2 - G_1}{G_1} \times 100\% = C_1 \exp\left(-\frac{t}{\tau_1}\right) + C_2 \exp\left(-t/\tau_2\right),$$

where G_1 and G_2 represent the conductance of pre-pulse and post-pulse respectively, which are used to simulate the relaxation time of synaptic message transmission. τ_1 and τ_2 are two fitting constants corresponding to the fast and slow decay terms of *PPF*, respectively. For positive voltage pulses, the values of τ_1 and τ_2 are 3.47 ns and 11.31 ns, respectively. And for negative voltage pulses,

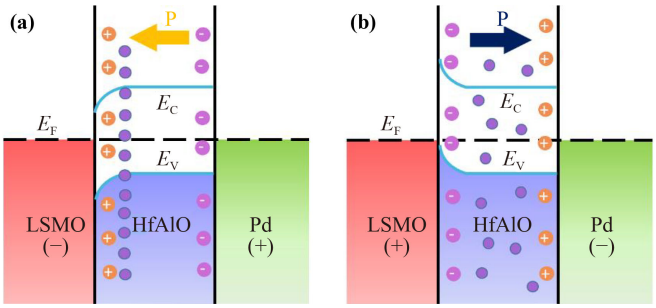

Fig. 7 **(a, b)** Schematic diagrams of the device resistance switching process under positive and negative applied voltages. The blue dots represent oxygen vacancies. E_F, E_V, and E_C represent the Fermi level, valence band, and conduction band of HfAlO, respectively.

the values of τ_1 and τ_2 are 11.41 ns and 11.52 ns, respectively. Similar to biological synapses, the *PPF* phenomenon can be successfully simulated by reducing the pulse-to-pulse interval to enhance the memory effect of continuous pulses.

The top metal electrode forms an ohmic contact with HfAlO, and the interface is in a low-resistance state, which is conducive to electron transport and does not participate in the resistance switching of the device. The interface formed by the HfAlO and LSMO bottom electrodes is affected by polarization and oxygen vacancies. The barrier layer belongs to the switching interface and affects the switching of the device resistance value. Therefore, the main consideration is the effect of the bottom electrode rather than the top electrode [36, 37]. The schematic diagram of the device resistance conversion process under positive and negative applied voltages is shown in Figs. 7(a) and (b). When a positive voltage is applied across the top Pd electrode, the depletion width and barrier height at the bottom HfAlO/LSMO interface are reduced due to the downward polarization, thus placing the device in the LRS state. Conversely, a negative voltage applied to the top electrode will generate upward polarization, increasing the barrier height and depletion width at the bottom interface, thus the device is in the HRS state. At the same time, when a forward voltage is applied, the positively charged oxygen vacancies migrate from the HfAlO film to the HfAlO/LSMO interface. The accumulation of oxygen vacancies at the interface also reduces the barrier height, and electrons can easily pass through the interface barrier and the device switches to the LRS state. When a reverse voltage is applied, this process is reversed, and the oxygen vacancies are pulled away from the HfAlO/LSMO interface back to the interior of the HfAlO film, increasing the interface barrier [38], and the device switches to the HRS state. It is worth noting that when the HfAlO thin film device is in the LRS state, the potential barrier on the HfAlO/LSMO interface is relatively low so that electrons can be easily injected into the HfAlO/LSMO interface [39], which is similar to the electron tunneling in Fig. 3(b). In addition, it has been reported that the polarization-induced the accumulation of oxygen vacancies can also reduce the barrier height [40], which further confirms the plausibility of the model proposed in this paper: that ferroelectricity and oxygen vacancies may co-regulate the interface barrier, thereby causing the resistance switching of the memristor.

4 Conclusion

In summary, we demonstrate the grown memristor on Si substrates with HfAlO ferroelectric layers. The ferroelectric memristor of this structure has stable I–V switching characteristics and excellent synaptic-like behavior. Pulses with different parameters affect the modulation of conduction current and conductance of the device. And the resistance switching behavior of the device can be used to simulate biological synaptic learning, forgetting processes, and short-term memory, long-term memory, and short-to-long conversion, such as STDP and *PPF*. Through further analysis, it is found that ferroelectricity and oxygen vacancies may co-regulate the interface barrier, thereby causing the resistance switching of the memristor. In short, the results demonstrate that HfAlO-based ferroelectric memristors has great potential in the application of new types of memory and brain-like chips in the future.

Declarations The authors declare that they have no competing interests and there are no conflict of interest.

Data availability The data that support the findings of this study are available from the corresponding author upon reasonable request.

Electronic Supplementary Material The online version contains supplementary material available at https://doi.org/10.1007/s11467-023-1310-6 and https://journal.hep.com.cn/fop/EN/10.1007/s11467-023-1310-6. See the Electronic Supplementary Material for the change of device relaxation time with the number of pulses. The relaxation time increases as the number of stimulation pulses increases. The fabricated memristor is confirmed to have the feasibility of transitioning from STP (short-term plasticity, STP) to LTP. Supplementary material also demonstrates the PFM amplitude mapping and P–V loop of HfAlO, and the effect of negative voltage pulses on conductance of the device. In addition, the LRS mechanism of the Pd/HfAlO/LSMO/STO/Si structure memristor is further studied in the supplementary material.

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