FRONTIERS OF PHYSICS

TOPICAL REVIEW
Volume 18 / Issue 6 / 63601 / 2023

Synthetic two-dimensional electronics for transistor scaling

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Received March 22, 2023; accepted May 4, 2023

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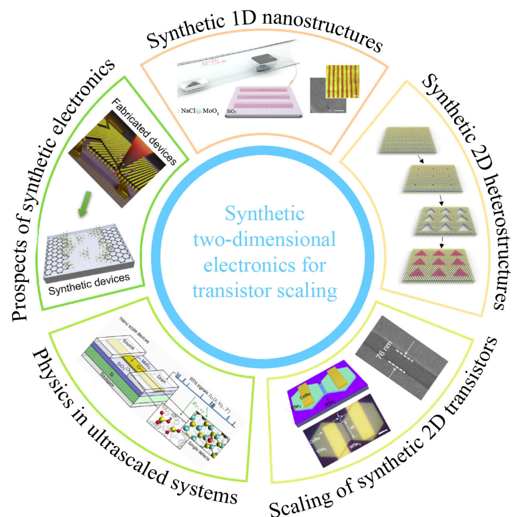
ABSTRACT

Two-dimensional (2D) materials have been considered to hold promise for transistor ultrascaling, thanks to their atomically thin body immune to short-channel effects. The lower channel size limit of 2D transistors is yet to be revealed, as this size is below the spatial resolution of most lithographic techniques. In recent years, chemical approaches such as chemical vapor deposition (CVD) and metalorganic CVD (MOCVD) have been established to grow atomically precise nanostructures and heterostructures, thus allowing for synthetic construction of ultrascaled transistors. In this review, we summarize recent developments on the precise synthesis and defect engineering of electronic nanostructures/heterostructures aiming for transistor applications. We demonstrate with rich examples that ultrascaled 2D transistors are achievable by finely tuning the "growth-as-fabrication" process and could host a plethora of new device physics. Finally, by plotting the scaling trend of 2D transistors, we conclude that synthetic electronics possess superior scaling capability and could facilitate the development of post-Moore nanoelectronics.



Keywords 2D materials, nanostructures, synthetic electronics, transistor scaling

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1 Introduction

Two-dimensional (2D) materials, such as semimetallic graphene [1, 2] and semiconducting MoS_2 [3, 4], have shown great promise in electronics [5–11], optoelectronics [12–15], sensors [16–18], catalysis [19–22] and other fields [23, 24]. Among them, 2D semiconductors have been anticipated to enable continuous downscaling of transistors, the building block of modern electronics, because their sizable bandgaps and atomic thickness could contribute to low current leakage [25] even for ultrascaled channel lengths. This benefit has been of great importance as the scaling of conventional silicon-based transistors (known as Moore's Law [26]) has been slowed down due

https://doi.org/10.1007/s11467-023-1305-3

to the prominent short-channel effect [27]. The short-channel effect can be understood in the context of electrostatic length $\lambda = \sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}} t_s t_{ox}}$, where ε and t denote the permittivity and thickness, respectively, and the subscript of "s" ("ox") indicates the semiconducting channel (gate oxide). As the source-drain leakage current is generally significant when the channel length (L_{ch}) decreases to $< 5\lambda$, an ultimately small t_s (that is, the 2D case) allows for the shortest λ and L_{ch} and hence hold promise to address the short-channel effect. Layered 2D materials are of particular interest for this purpose thanks to their dangling-bond-free surface with reduced carrier scatterings [28].

Among the 2D materials family, transition metal dichalcogenides (TMDs) in the monolayer form possess larger direct bandgaps [29] compared with silicon are particularly suitable for the purpose of transistor scaling [30], as well as for efficient and modulable optoelectronics [31–33]. Unlike the FinFET [34] and Gate-All-Around FET (GAAFET) architectures [35], the fabrication of 2D FETs can be as simple as that of conventional MOSFETs [Fig. 1(a)], while maintaining the downscaling capability [Fig. 2(b)] [36]. Moreover, 2D materials are compatible with most of the technologies developed for silicon electronics [Fig. 1(c)] [36], such as multichannel FETs (MCFETs), vertical-gate-all-around (VGAA) FETs, and hetero/homo tunnelling-FETs (hetero/homo-TFETs). The 2D devices can also be monolithically integrated with silicon FinFETs in the back-end-of-line process to harness the benefits from both sides (the maturity of silicon technology and the promise of 2D technology). It is anticipated that, in the post-Moore era, 2D materials could serve as ideal candidates for transistor scaling, as well as to spur new computing paradigms [37]. For example, pioneering works that use 2D devices to mimic biological functionalities have triggered an outburst of research on neuromorphic computing [38, 39].

Nevertheless, the downscaling of 2D transistors has been impeded by the spatial resolution of current microfabrication technologies such as photolithography (15 nm half pitch) [40, 41] and direct laser writing (DLW, with ~100 nm feature size) [42, 43]. Electron beam lithography (EBL, with 5 nm half pitch) [44, 45],

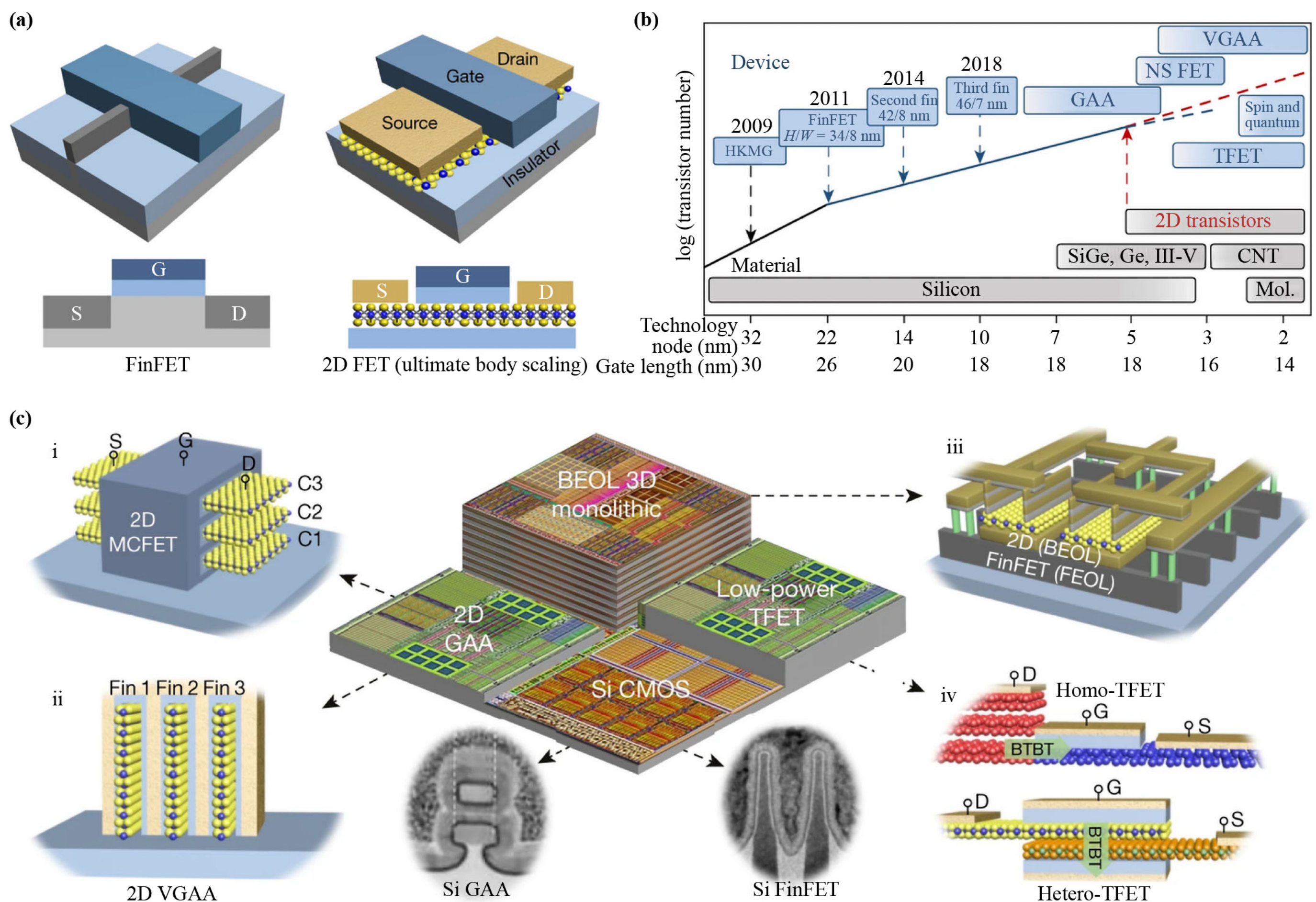

Fig. 1 2D technology for transistor scaling. **(a)** Comparison of 2D transistors and FinFETs [36]. **(b)** Transistor scaling trend versus technology node and physical gate length [36]. **(c)** Schematic illustration of possible technologies in future chips incorporating 2D materials [36].

on the other hand, can be used to fabricate ultrascaled devices, yet this low throughput process is incompatible with large-scale production of 2D integrated circuits. To evaluate the short-channel performance of 2D FETs, several strategies have been reported to achieve transistors with sub-10 nm channel lengths. For example, using the corrosion-cracked Bi_2O_3 film as the template, onto which monolayer MoS_2 was transferred, a 2D transistor with 8.2 nm channel length [Fig. 2(a)] was fabricated [46], exhibiting an on/off ratio of 10^6 and a subthreshold swing of 140 mV/dec. Similar methods by using the phase-separation patterns of a block copolymer [47] or the selectively etched grain boundaries of CVD-graphene [48] also enabled the fabrication of 2D FETs with sub-10

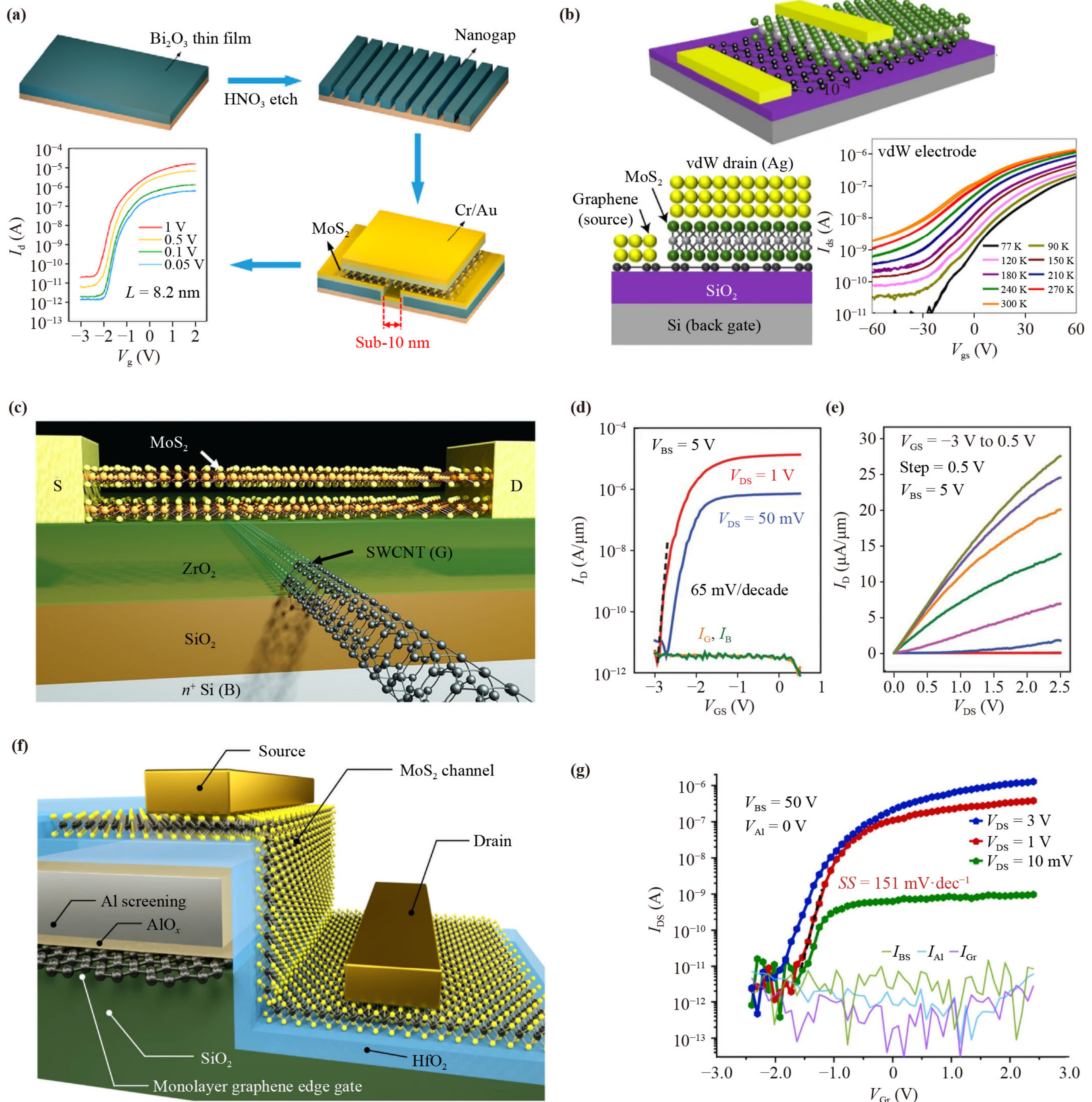

Fig. 2 Ultrascaled 2D transistors enabled by nanofabrication. **(a)** TMD transistors with sub-10-nm channel length fabricated by corrosion crack of Bi_2O_3 [46]. **(b)** Schematic and transfer curve of a vertical transistor [56]. **(c–e)** A carbon nanotube-gated TMD transistor with (c) corresponding device structure, (d) transfer curve, and (e) output characteristics [50]. **(f)** Schematic of a graphene edge-gated transistor with **(g)** corresponding transfer characteristics [51].

nm channel lengths. It should be noted that, these spontaneous nanopatterns (most are arrayed stripes) inherit from and are preset by their parent materials, thus lacking the designability for constructing complex circuits.

Considering the ultrathinness of 2D materials, an exquisite van der Waals (vdW) heterostructure by combining MoS_2 as the channel and graphene as the bottom electrode constitutes a vertical transistor, wherein the source-drain current flows in the vertical direction and the bottom graphene with weak screening allows for dielectric control of the device with Si back gates [Fig. 2(b)]. Using this setup, Liu *et al.* [49] reported that the on/off ratio decreased from 10^3 for 3.60 nm channel length to 26 for 0.65 nm channel length, possibly marking the scaling limit of transistors made of 2D semiconductors. It is noteworthy that the vertical transistors are naturally compatible with 3D monolithic integration but are less relevant to increasing the areal integration density. How the channel length limit in vertical transistors can be translated into the planar case remains an open question that requires further exploration.

With the channel lengths well beyond the nanometer scale, an alternative way to evaluate the short-channel performance of 2D transistors is by scaling the gate lengths (L_G). Recent works have introduced single-wall carbon nanotube [Fig. 2(c), L_G ~1 nm] [50] and graphene side edge [Fig. 2(d), L_G ~0.34 nm] [51] as the gate electrodes, both demonstrating effective dielectric control of the 2D channels. Notably, the carbon nanotube-gated device exhibited excellent transfer characteristics with an on/off ratio of ~10^6 and a nearly ideal subthreshold swing of ~65 mV/dec, while the graphene edge-gated device had a deteriorated subthreshold swing of ~117 mV/dec. Depending on the thickness of the high-k dielectrics, these ultrascaled gate electrodes can actually deplete carriers in a wider spatial range. TCAD modeling of the carbon nanotube-gated 2D transistor (ZrO_2 dielectric thickness ~10 nm) exhibited an effective depletion width of ~3.9 nm, verifying again the suitability of 2D semiconductors for device scaling down to the sub-10 nm regime.

The above pioneering works have well demonstrated the great promise and prospect of 2D materials, in particular 2D semiconductors, for downscaling transistors and extending Moore's law. Nevertheless, how small a 2D transistor can be remains an open question, as this size has gone below the spatial resolution limit of existing nanofabrication techniques. From a chemist's point of view, the sub-10-nm regime has fallen within the molecular scale, for which bottom-up synthesis could provide unrivaled precision in structural control and the capability for scale production. Indeed, recent advances in synthesizing precise nanostructures have shown that functional electronic devices can be directly evolved, many of them possessing characteristic sizes of nanometers and the potential for further downscaling. We therefore propose that synthetic 2D electronics, namely growing 2D electronic structures and devices in a bottom-up fashion, could be a new route, in supplement to top-down nanofabrication, to achieve transistor scaling at unprecedented length scales. Notably, early works on patterned growth and surface functionalization of 2D materials have laid a solid foundation to further establish the methodology of synthetic 2D electronics [52–55]. Summarized below are a few examples in the precise syntheses of graphene and TMD nanoribbons, heterostructures, superlattices and functional devices to illustrate the great prospects of synthetic 2D electronics. Effects of atomic defects and edge disorders for ultrascaled 2D transistors are also discussed. We conclude by pointing out the versatility of synthetic electronics and the efforts in need to achieve the transistor size limit.

2 Precise synthesis of electronic nanostructures

As mentioned above, chemical synthesis could provide unparalleled structural precision at molecular scale (1-10 nm), which is highly desired for further scaling the 2D transistors. Indeed, recent years have witnessed tremendous advancement in the precise synthesis of electronic nanostructures, including one-dimensional (1D) nanoribbons and 2D heterostructures and superlattices, which are amenable to being processed/fabricated into functional nanodevices. In this section, we discuss in detail the precise synthesis of these electronic nanostructures.

2.1 Synthetic 1D nanostructures

Early efforts in synthesizing 1D nanostructures of 2D materials mainly focused on graphene nanoribbons (GNRs), with the expectation of bandgap opening for transistor applications. Several methods have been developed to obtain GNRs with the ribbon widths below 50 nm. Conventionally, the fabrication of GNRs is by using EBL-derived PMMA masks that protect chosen areas during oxygen plasma etching, with which to carve graphene into desired geometries. Such GNR devices exhibited a confinement gap of up to 0.5 eV [57]. In 2010, Wang *et al.* [58] fabricated lithographically 20–30-nm-wide GNR arrays and implemented a gas-phase etching process to narrow the ribbons down to <10 nm [Fig. 3(a)]. The bandgap opening was manifested by a high on/off ratio of ~10^4 at room temperature with sub-5-nm-wide channels, indicating the feasibility of GNRs for digital transistors.

Another ingenious method for GNR fabrication was plasma etching and unzipping of multi-walled carbon nanotubes (MWCNTs) partially imbedded in a polymer

film [Fig. 3(b)] [59]. The GNRs synthesized as such reportedly had smooth edges and a narrow width distribution (10–20 nm), yet transport measurements revealed a low on/off ratio of 10, indicating insignificant bandgap opening. It is generally recognized that edge disorder in GNRs could cause carrier localization and contributes to a transport bandgap. However, atomically smooth graphene edges, particularly along the zigzag direction, could host metallic edge states and reduce the on/off ratios [60]. In this sense, a trade-off between carrier mobility and transport bandgap has to be considered by tuning the edge disorders.

To achieve even narrower GNRs, such as sub-5-nm-wide ones, bottom-up polymerization strategies have to be considered [61]. Not only the width of the GNR depends on the size of the organic precursor, the shape and edge configuration does as well. For example, 10,10'-dibromo-9,9'-bianthryl and 6,11-dibromo-1,2,3,4-tetraphenyltriphenylene monomers could precisely polymerize into straight and Chevron-type GNRs, respectively [Fig. 3(c)] [62]. This is a perfect example that showcases the capability of chemical synthesis to achieve precise electronic nanostructures. Another method to achieve ultranarrow GNRs, as reported by Wang *et al.* [63], is by creating nanotrenches in *h*-BN via nanoparticle etching, followed by templated graphene growth to fill the trenches. The obtained GNRs are embedded in an insulating *h*-BN matrix, with their edges being completely encapsulated and sub-10-nm ribbon widths pre-determined by the trench sizes (i.e., nanoparticle sizes). Reduced edge scatterings were revealed by transport measurements, exhibiting carrier mobilities nearly one order-of-magnitude higher than previously reported ones.

For scalable production, Sprinkle *et al.* [64] reported a self-organized growth of GNRs on a templated silicon carbide substrate prepared by photolithography and microelectronics processing [Fig. 3(d)]. With appropriate control of growth temperature, time and atmosphere, GNRs as narrow as 40 nm could be preferentially deposited on $(11\bar{0}n)$ nanofacets that evolved from the etching-induced surface steps. Prototype GNR devices exhibited quantum confinement at 4 K, an on/off ratio of 10, and carrier mobilities up to 2700 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature. The scalability of this approach was well demonstrated by the fabrication of 10 000 top-gated GNR transistors on a 0.24-cm^2 SiC chip.

Despite these achievements, the transistor application of GNRs, especially for digital electronics, have been hindered due to the stringent requirements in controlling both width and chirality of the GNRs for a sizable bandgap. To bypass this limitation, directly synthesizing 1D nanoribbons out of 2D semiconductors such as

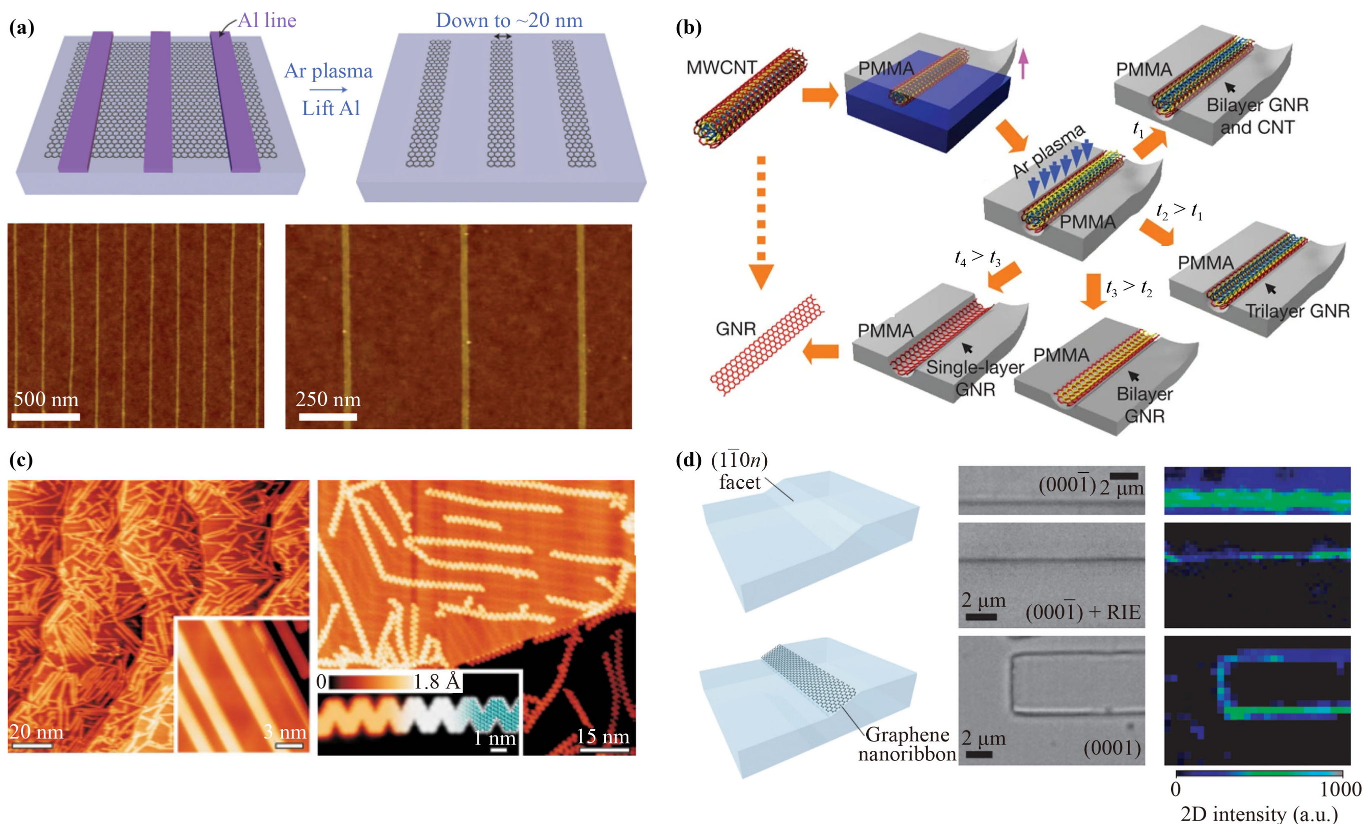

Fig. 3 Chemically derived GNRs. **(a)** Al ribbon-sheltered plasma etching of graphene for GNRs with width down to ~20 nm [58]. **(b)** PMMA-assisted plasma cutting of carbon nanotubes for GNRs [59]. **(c)** On-surface polymerization of organic monomers into GNRs [62]. **(d)** Step-induced CVD growth of GNRs [64].

TMDs could be a promising route for miniaturized transistors, and the synthetic strategies proposed for GNRs can serve as inspiring reference.

To this end, a lithography-free synthesis strategy exploiting a solid-liquid-vapor (SLV) process was reported to fabricate arrays of highly oriented TMD nanoribbons [Fig. 4(a)] [65]. During the CVD process, $MoTe_2$ flakes were controllably grown and etched by tuning the H_2 flow rates. The orderly etching was attributed to a synergistic effect of H_2 and NaCl promoters, where NaCl droplets moved preferentially along the [010] direction of 1T′-$MoTe_2$ and etched the crystal with assistance of H_2 into arrayed ribbons as narrow as 50-80 nm. While 1T′-$MoTe_2$ is metallic rather than semiconducting, the proposed strategy might be applicable to other anisotropic 2D semiconductors such as black phosphorous and ReS_2.

Similar to the selective growth of graphene on high-index nanofacets of SiC [64], a strategy called ledge-directed epitaxy (LDE) has been used to grow single-crystalline and self-aligned TMD nanoribbons [66]. In this case, MoS_2 synthesized on β-Ga_2O_3 (100) substrates adopted ribbon-like morphologies, with widths varying from 70 to 600 nm. The (100) plane of the exfoliated β-Ga_2O_3 presented atomically sharp steps along the $(\bar{2}01)$ facet (the so-called ledges) and guided the site-selective nanoribbon growth. Such step-induced growth can be more delicately controlled in ultra-high-vacuum (UHV) systems. For example, Xu *et al.* [66] reported that MoS_2 nanowires (nanoribbons with an extreme width of one unit cell) could be synthesized on Au(755) substrates [Fig. 4(b)]. The MoS_2 nanowire underwent strong interplay with Au(755) surface and gave rise to periodically oscillated edge states along its length, indicating the existence of Peierls instability. Notably, at this extreme width, strain modulation was prominent due to the decreased in-plane rigidity, which had a profound effect on the electronic properties of the nanowire/nanoribbon systems.

Chowdhury *et al.* [67] reported a gas-phase synthesis approach to control the dimensionality of TMD crystals, where steps/ledges were not a necessity [Fig. 4(c)]. Using Si(001) pretreated by phosphine as the growth substrate, CVD synthesis of MoS_2 on it yielded high-quality and width-tunable nanoribbons. By controlling the phosphine dosage, the width of MoS_2 nanoribbons could be varied from 50 to 430 nm. It was believed that the coarsened topography of the Si-P_x surface induced symmetry breaking of incipient MoS_2 nuclei and enabled rapid crystal growth in one direction, yet future studies are still needed to fully elucidate the 1D growth mechanism.

Inspired by conventional 1D growth systems such as silicon nanowires [68] and carbon nanotubes [69], Li *et al.* [70] reported that molten sodium molybdate droplets could trigger vapor-liquid-solid (VLS) growth of MoS_2 nanoribbons as well. In this case, NaCl salts reacted with MoO_3 precursors to form molten Na–Mo–O droplets. These droplets crawled on the substrate surface, reacted with sulfur vapor, and left behind MoS_2 ribbons on the trajectories. The widths of the ribbons were however less controlled, ranging from tens to thousands of nanometers. By introducing nickel nanoparticles to the VLS system, Li *et al.* [71] found that bilayer MoS_2 nanoribbons could be catalytically generated, with the second-layer ribbons as narrow as 8 nm, prescribed by Ni particle sizes [Fig. 4(d)]. This represents, to our knowledge, the narrowest MoS_2 ribbons ever achieved in a CVD system.

The above works demonstrate the great prospects of chemical approaches to synthesize high-quality nanoribbons, with the achieved widths even beyond the nanofabrication capabilities. Quantum confinement plays an increasingly vital role as the ribbon width decreases, contributing to tunable photoluminescence [67], significant transport bandgap [63], and related Coulomb blockade oscillation [71]. Nevertheless, to fabricate short-channel transistors using these 1D nanostructures, the source/drain electrodes have to form effective contacts on the two side edges, which requires ultrahigh alignment precision as well. A possible solution to this should be directly growing metallic epitaxial layers on the two ribbon edges (that is, edge epitaxy). This is indeed an essential technology to be addressed to fully realize the potential of synthetic electronics.

2.2 Synthetic 2D heterostructures

Heterostructures are the key component for modern electronics. Heterogeneous integration using 2D materials are quite unique in that their vdW surface allows for high-quality interface without the restriction of lattice matching. Additionally, conventional functionalization techniques such as substitutional doping can also be applied for the 2D materials to realize ultrathin planar electronics with designed doping profiles. Indeed, recent works have demonstrated that ultrathin heterostructure of 2D TMDs, either in-plane or out-of-plane, can be chemically synthesized and exhibit distinct electronic functionalities. In 2014, Duan *et al.* [72] successfully synthesized MoS_2–$MoSe_2$ and WS_2–WSe_2 in-plane heterostructures by the CVD method. The peripheral edges of the pre-grown 2D TMDs with unsaturated dangling bonds catalyzed the growth of the second TMD species and extend the 2D crystals in the lateral direction. Similar works have also been reported by other researchers [73–75]. By sequential edge epitaxy, planar multi-junctions could also be obtained [Fig. 5(d)] [76], exhibiting smooth and atomically sharp interfaces as characterized by HRTEM. Combining this edge epitaxy mechanism with a laser-patterning and thermal etching process, Duan *et al.* [77] also created periodically mosaic

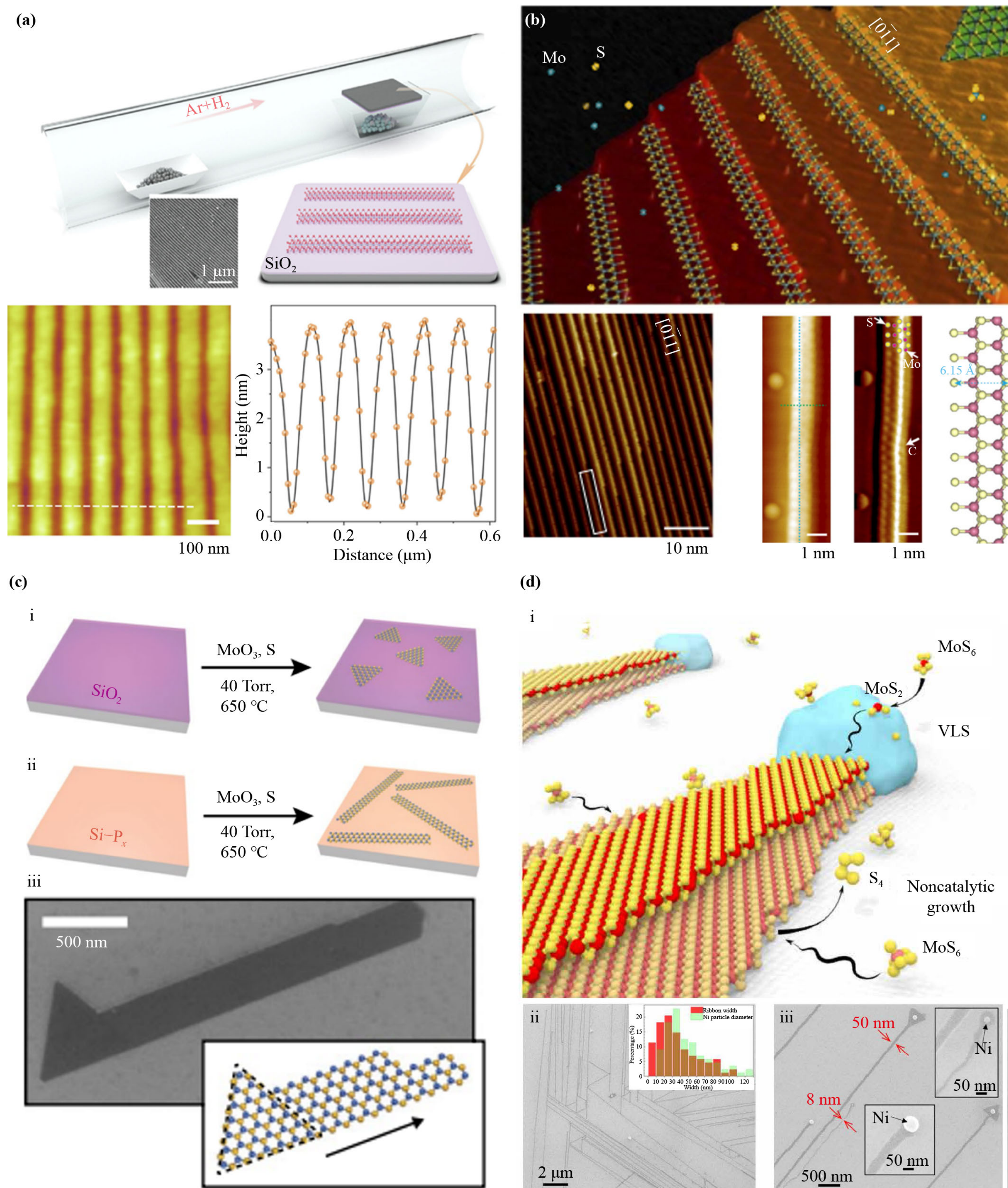

Fig. 4 Synthetic TMD nanoribbons. **(a)** Self-etching growth of $MoTe_2$ nanoribbon arrays and the AFM images [65]. **(b)** Step-guided growth of MoS_2 nanowires and the STM images [66]. **(c)** Growth of MoS_2 nanoribbons on (i) SiO_2/Si and (ii) phosphine-treated Si(001) substrates, together with (iii) the SEM image of MoS_2 nanoribbons [67]. **(d)** Growth of ultranarrow MoS_2 nanoribbons by Ni nanoparticle catalysis, with (i) showing the schematic of the growth process, and (ii, iii) the SEM images [71].

TMD heterostructures with atomically sharp boundaries [Fig. 5(f)]. Such highly robust growth of lateral monolayer heterostructure arrays with artificial mosaic patterns has opened an intriguing avenue to realize large-scale functionalization of 2D materials.

Van der Waals heterostructures created by stacking the 2D material "Legos" represent the ultimate device miniaturization in vertical direction, and have given rise to new device paradigms such as barristors [78] and vertical transistors [56] with even sub-1-nm channel lengths. Early works in this direction mainly focused on graphene-related vdW heterostructures fabricated by artificial stacking. The insulating components such as h-BN and TMDs served as the tunneling barrier between top and bottom graphene layers to modulate charge transport and/or photocarrier separation [79–83]. While this transfer preparation method is suitable for prototype device exploration, it lacks the desired scalability for batch production and device integration. CVD synthesis of high-quality vdW heterostructures are attractive for large-scale production, but are quite challenging in that at the high growth temperatures, atom mixing across

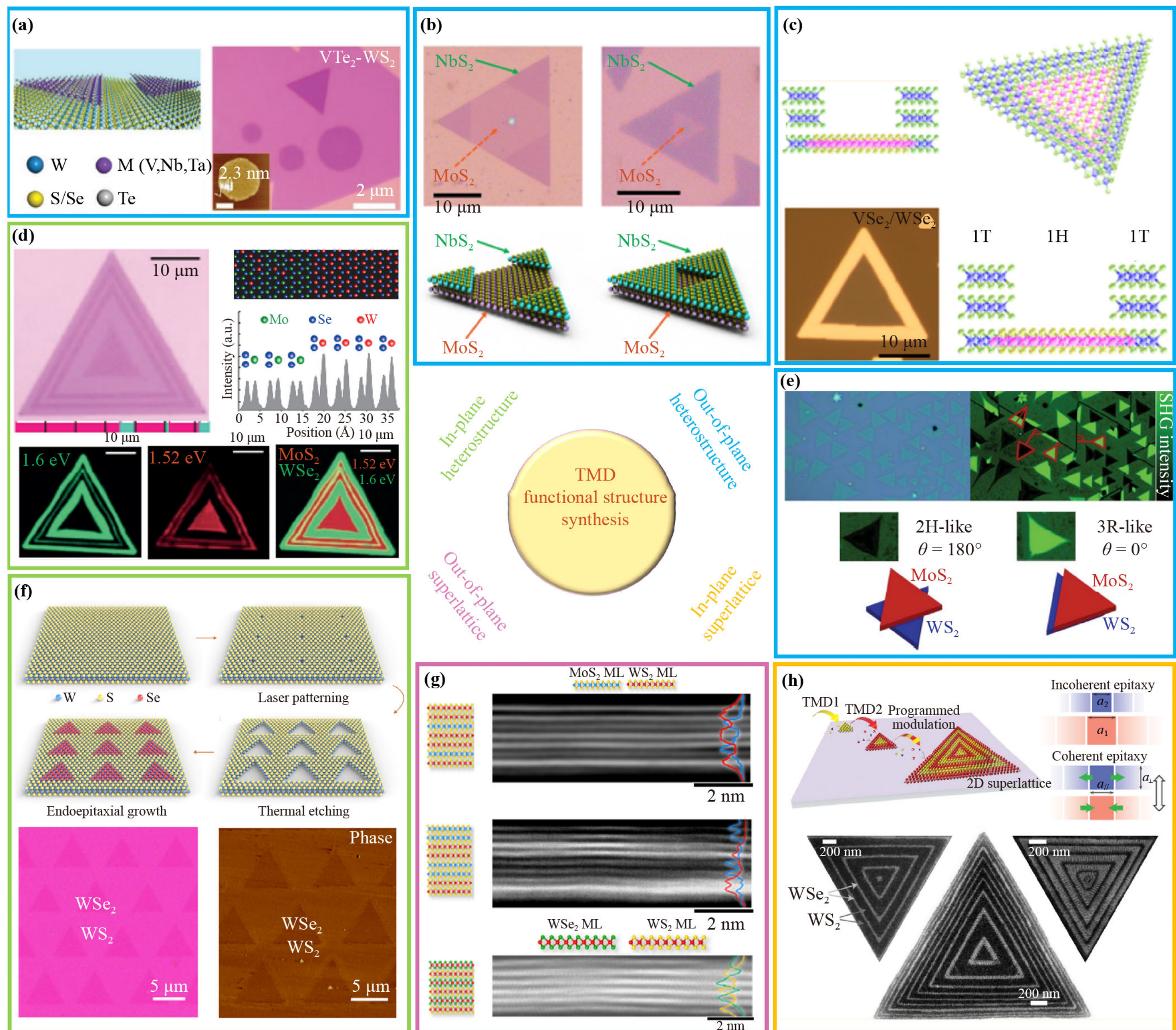

Fig. 5 Synthetic TMD heterostructures. **(a)** Two-step growth of vertical VTe_2/WS_2 heterostructures [84]. **(b)** One-step growth of vertical NbS_2/MoS_2 heterostructures [85]. **(c)** Two-step growth of vertical VSe_2/WSe_2 heterostructures [86]. The second-layer growth initialized at (a) in-plane defects, (b) vertices, and (c) edges, respectively, of the first layers. **(d)** One-pot synthesis of lateral TMD heterostructures and multi-heterostructures [76]. **(e)** MoS_2/WS_2 heterobilayers with tunable stacking orders [87]. **(f)** Mosaic patterns of lateral TMD heterostructures [77]. **(g)** Vertical TMD superlattices fabricated by MOCVD [89]. **(h)** In-plane TMD superlattices grown by modulated MOCVD [90].

different 2D planes is unavoidable and could degrade the precision of band engineering. Successful examples of synthetic vdW heterostructures [84–86] are mainly those composed of metallic and semiconducting TMDs with a large gap of growth temperatures [Figs. 5(a-c)]. The growth of the second TMD layer seemed to initialize at the in-plane defect sites [Fig. 5(a)], the vertices [Fig. 5(b)], or the edges of the first layer [Fig. 5(c)]. An undisturbed vdW gap exists in between and helps to suppress interfacial defect states and/or orbital hybridization-induced gap states. Devices with this contact mode exhibits more linear and much higher output currents than with conventional metal contacts, indicating the mitigation of Fermi level pinning [86]. Consequently, the synthetic vertical heterostructures of metallic/semiconducting TMDs shed light on a potential path for fabricating high-performance electronic devices. As for the semiconducting/semiconducting TMD vdW heterostructures, some interesting physical properties are uncovered as well. For example, Rogeé *et al.* [87] revealed that MoS_2/WS_2 heterobilayers synthesized by scalable one-step CVD presents out-of-plane ferroelectricity and piezoelectricity that can be tailored by the stacking order [Fig. 5(e)]. Such vdW heterostructures with staggered band alignment also contribute to ultrafast charge transfer due to the high-quality interface [88], which may enable novel 2D devices for optoelectronics and light harvesting.

Following the above achievements, periodic structures of TMD semiconductors in the superlattice form could further boost the electronic engineerability of these materials. Efforts in this direction include the construction of both vdW (vertical) and in-plane (lateral) superlattices, preferably by chemical synthesis rather than artificial stacking. By the programmable MOCVD growth of alternating MoS_2/WS_2 monolayers, Jin *et al.* [89] reported the successful construction of vdW superlattices for the first time [Fig. 5(g)]. The coherent $(MoS_2/WS_2)_n$ superlattices were demonstrated to facilitate the valley-polarized optical excitations, whose circular dichroism signals scaled linearly with the stack numbers n, showcasing rich opportunities of unexplored properties and functionalities in such synthetic structures. On the other hand, monolayer superlattices by alternately combining two TMD species in the 2D plane is even more challenging, since the lattice matching requirement might exert additional restriction for the successful synthesis. Among related efforts, Xie *et al.* [90] reported the first example of 2D superlattices via omnidirectional epitaxy of WS_2 and WSe_2. Despite the unmatched lattice constants of the two, the 2D superlattices surprisingly possessed coherent and dislocation-free lattices, and were capable of accommodating sufficient epitaxial strains via spontaneous self-rippling of compressed parts. Such coherent superlattices were asserted to provide building blocks with target functionalities at the atomically thin limit.

It should be noted that, both the vertical and the in-plane superlattices insofar were synthesized by the MOCVD method, thanks to its slow kinetics that enables atomically controlled growth, and the relatively low growth temperature to avoid atom mixing. Strikingly, one recent preprint work demonstrated that ultrathin lateral heterostructures with sub-nm stripe width can be precisely synthesized by MOCVD [91], revealing its superior controllability. We therefore anticipate that ultra-downscaled 2D electronics could be synthetically fabricated using the MOCVD technologies, and the industry-level application of 2D materials, in particular for those TMDs, will presumably replicate the development path of the III-VA semiconductors, whose success largely relies on MOCVD as well.

3 Atomic defects in ultrascaled systems

Previous works have shown explicitly that synthetic methods such as CVD and MOCVD are capable of fabricating atomically precise nanostructures/heterostructures of 2D materials, which can be further deployed into ultrascaled electronic devices. Considering that the density of native defects in 2D materials (such as chalcogen vacancies and oxygen substitution in CVD-grown TMDs [92]) is on the order of 10^{12} cm^{-2}, an ultrascaled channel could host only a finite number (several to tens) of atomic defects, making a statistic scenario invalid for such a small system. Indeed, discrete current responses of single defects were found in ultrascaled MoS_2 transistors with channel size of ~65 × 50 nm^2, manifesting the characteristics of random telegraph noise [Fig. 6(a)] [93]. The current noise was understood by hidden Markov models and was attributed to the charge capture and emission from individual atomic defects. This is a good example that highlights the difference of ultrascaled nanodevices from larger ones, where discreteness and stochasticity start to dominate.

Heteroatom substitution represents a type of artificial defects and is essential to modulate the doping profile of 2D materials. Taking substitutionally-doped TMDs as an example, the structural complexity of the heteroatom defects has been explored by HRTEM [Fig. 6(b)] [94], and the 2D nature of the materials makes these defects highly addressable by external fields. Interesting properties such as giant Zeeman shift of 7.8 meV/T [Fig. 6(c)] [95] and bound hole states with a diameter of ~2.2 nm [Fig. 6(d)] [96] have been uncovered on individual dopants, as verified by magneto-tunneling transport and scanning tunneling microscopy/spectroscopy (STM/S) measurements, respectively. Scaling down these substitutionally-doped 2D systems into functional nanodevices, however, remains rarely explored, where quantum fluctuations and random excitations of the heteroatoms cannot be averaged in a finite time, making their electronic properties

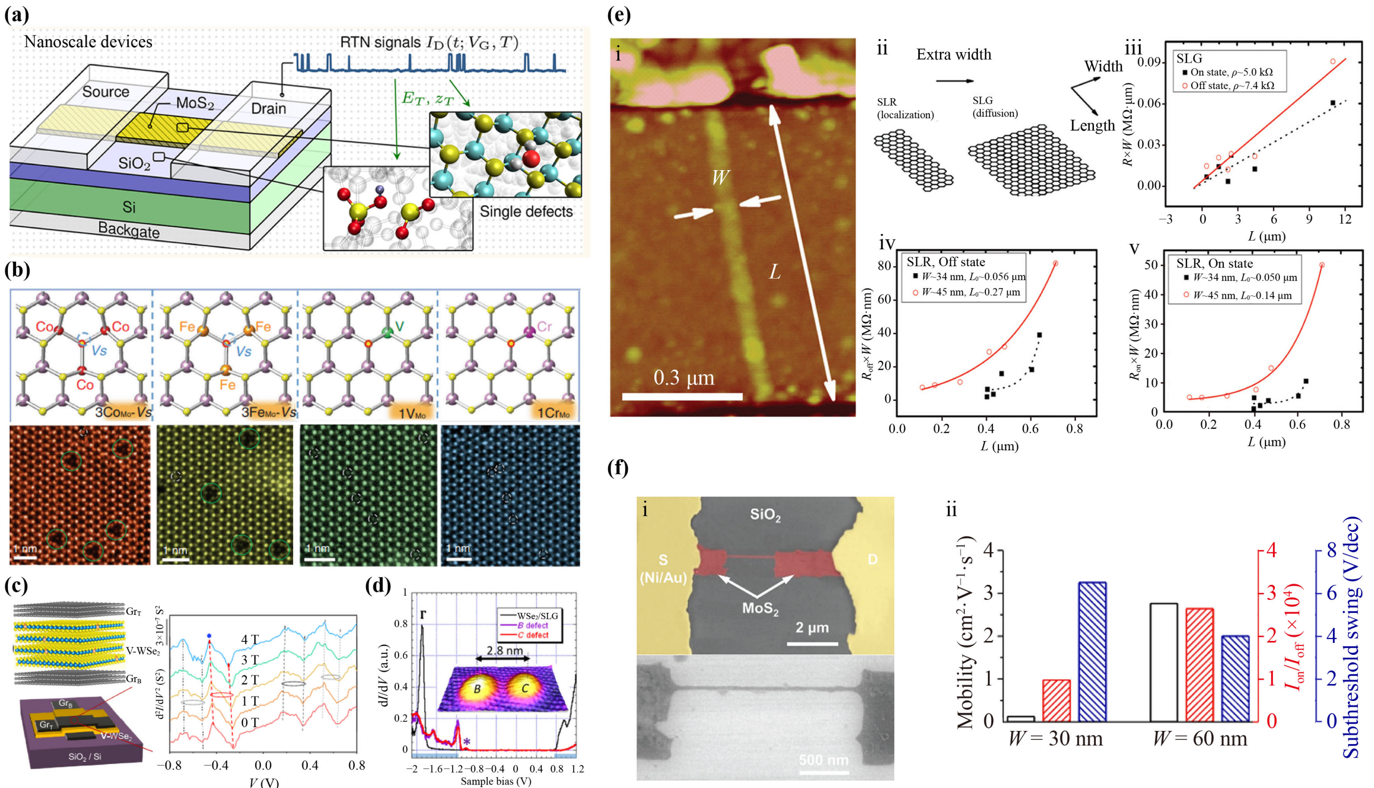

Fig. 6 Defects in ultrascaled monolayer systems. **(a)** Random telegraph noise of currents induced by individual defects in ultrascaled MoS_2 FETs [93]. **(b)** Configurations of atomic dopants in TMDs [94]. **(c)** Zeeman shifts observed in V-doped WSe_2 by transport measurements [95]. **(d)** Bound hole states in monolayer V-doped WSe_2 by STS measurements [96]. **(e)** Edge effects of (i) graphene nanoribbons, with (ii) showing the dimensional difference of single-layer graphene (SLG) and SLRs, (iii) linear resistance–length (R–L) relation of SLG, (iv) and (v) exponential R–L relation of SLRs at both low and high carrier densities [99]. **(f)** Monolayer MoS_2 nanoribbon transistors, with (i) optical and SEM images showing the device dimension and (ii) key transistor properties affected by ribbon widths [100].

deviate significantly from that of the larger-size counterparts, and possibly resemble that of single-electron transistors [97] and/or molecular electronics [98]. In this regard, not only can synthetic electronics provide ultrascaled nanostructures as device channels, but also conveniently incorporate heteroatoms through in-situ doping, both beneficial to the study of doped nanosystems.

For ultrascaled nanoribbon devices, edge disorders are the major defects that account for carrier scatterings. Early works of electrical measurements indeed found that single-layer ribbons (SLRs) of graphene exhibited resistance exponentially dependent on the SLR length, indicating a transport regime of strong localization rather than diffusion [Fig. 6(e)] [99]. Similarly, SLRs of MoS_2 also showed degradation in carrier mobility, on/off ratio, and subthreshold swing [Fig. 6(f)] [100], due to the increasingly severe edge scattering with reduced ribbon width. We note that existing nanoribbon works are primarily based on lithographically fabricated samples, which natively possess higher degree of edge disorders. By exploiting chemical approaches such as anisotropic etching [60] and edge-encapsulated synthesis [63], it is possible to eliminate/mitigate edge scatterings to probe the intrinsic transport properties of nanoribbon systems. In these cases, the fabricated nanoribbons possess atomically smooth edges with reduced structural disorder, and the edge states associated with dangling bonds can be further passivated by covalent encapsulation. This represents another key advantage of synthetic electronics, with a potential to further boost the development of nanodevice technologies.

4 Scaling of synthetic 2D transistors

The potential of synthetic electronics, particularly on 2D transistor scaling, has been gradually recognized in recent years. The key step is to form metal-semiconductor-metal heterostructures with low contact resistance (R_C) and narrow spacing between the metal electrodes (that is, small channel length, L_{ch}). Early attempts have been focused on synthetic graphene/MoS_2 heterostructures [101–104], with a tantalizing demonstration of batch-produced 2D transistor arrays [Fig. 7(a)] [103], thanks to the development of CVD techniques for growing large-area 2D materials. The second-step MoS_2 growth seemed

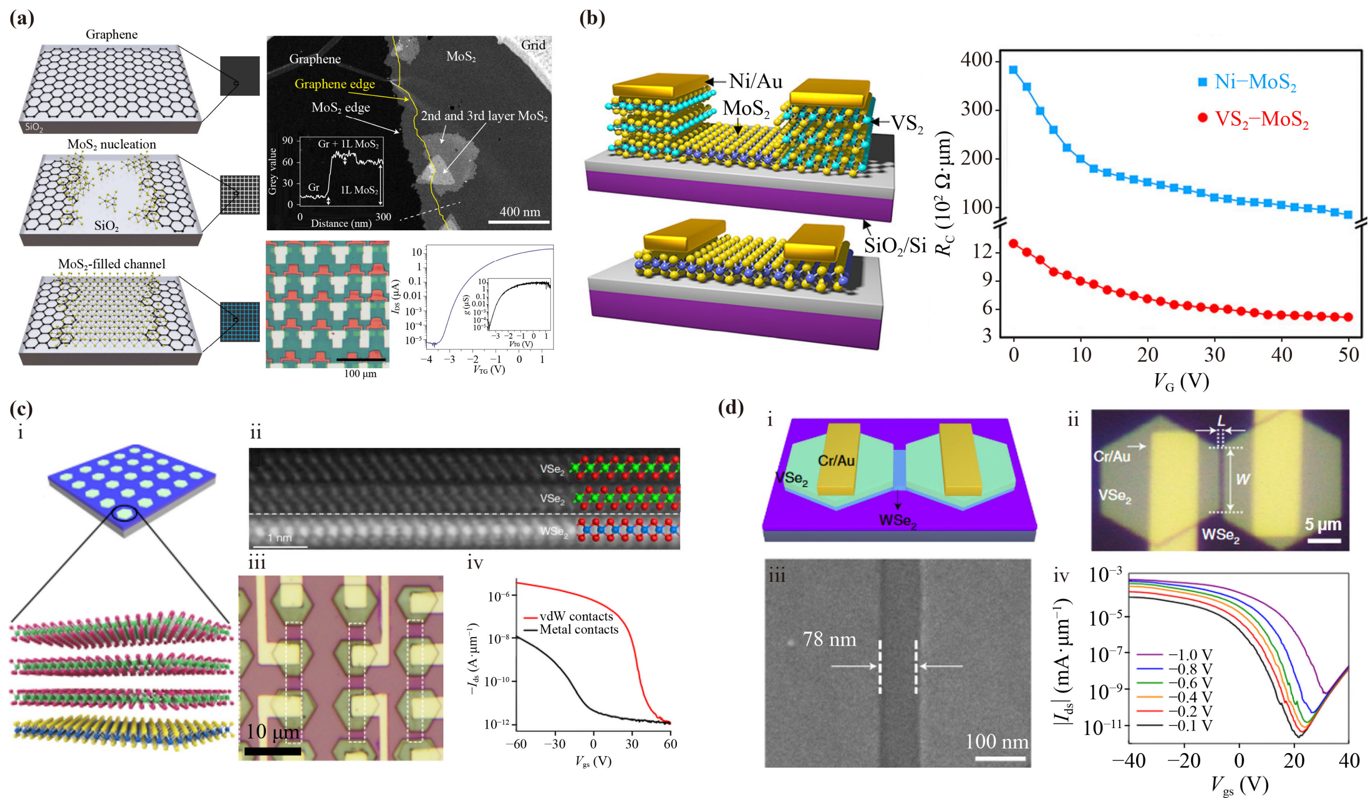

Fig. 7 Synthetic 2D transistors. **(a)** Large-scale chemical assembly of graphene/MoS_2 heterostructures as arrayed FETs [103]. **(b)** Lateral VS_2–MoS_2–VS_2 heterostructures as synthetic transistors with low contact resistances [105]. **(c)** Synthetic arrays of vertical m-TMD/s-TMD heterostructures, with (i) showing the schematic structure, (ii) cross-section STEM image, (iii) optical image of the device arrays, and (iv) improved transfer characteristics [107]. **(d)** Short-channel bilayer WSe_2 transistors by direct chemical synthesis, with (i, ii) showing the schematic and optical images, respectively, of the device, (iii) SEM image of a short-channel device with L_{ch}~76 nm, and (iv) corresponding transfer characteristics [108].

to initialize on the edges of pre-patterned graphene, yet their lattice dissimilarity prohibited covalent bonding of the two, leading to prominent contact resistances of >10 kΩ·μm. Notably, the MoS_2 channel lengths, as stipulated by the distance of neighboring graphene pads, were dependent on the spatial resolution of the patterning techniques, which set a limit for further device scaling. Nevertheless, the concept of synthetic transistors has been justified doable ever since.

Recent investigation on synthetic 2D transistors has switched to the construction of metal-semiconductor heterostructures within the TMD family. Considering their lattice similarity and electronic complementarity, a high-quality interface could be expectably generated with lower R_C in comparison to the graphene/TMD case. One representative work is the two-step synthesis of lateral MoS_2–VS_2 heterostructures [105]. The metallic VS_2 nanosheets grown in the first step cracked randomly during transfer, allowing for MoS_2 growth in the submicron cracks to form the desired device structure [Fig. 7(b)]. Electrical measurements on the VS_2-contacted MoS_2 transistors revealed a remarkably low R_C of ~0.5 kΩ·μm and a decent field-effect mobility (μ_{FE}) of ~35 $cm^2·V^{-1}·s^{-1}$. It was postulated that the covalent bonding at the 1D interface contributed to efficient coupling of the two materials and therefore the low-resistance contacts. Such an edge-contact strategy was recently highlighted with a record-high μ_{FE} of 358 000 $cm^2·V^{-1}·s^{-1}$ in WSe_2 [106], suggesting the ceiling performance to be achieved for 2D electronics based on TMDs.

The synthetic all-TMD electronics have been further developed by Duan *et al.* [107], with an emphasis on the general synthesis of vertical heterostructure arrays. Laser-patterned films of semiconducting TMDs (s-TMDs) was exploited to precisely control the nucleation and growth of diverse metallic TMDs (m-TMDs), yielding vertical heterostructure arrays with designable periodic arrangements and tunable lateral dimensions [Fig. 7(c)]. With atomically clean vdW interface, the m-TMDs could serve as reliable synthetic vdW contacts for underlying s-TMDs, capable of delivering high ON-currents of up to 900 μA/μm in bilayer WSe_2 transistors. This general synthesis strategy is promising for batch production and large-scale integration of 2D electronics, yet the ultrascaling capability is still limited by the patterning

technologies.

To tackle the ultrascaling issue, using the synthetic platform of vertical heterostructures, the same group designed a controlled domain merging and cracking process to create nanogaps between metallic VSe_2 nanoplates on WSe_2 [Fig. 7(d)] [108]. Short-channel transistors with L_{ch} <100 nm can thus be fabricated, exhibiting remarkable on-state current densities above 1.0 mA/μm and on-state resistances below 1.0 kΩ·μm at room temperature, both comparable to silicon transistors with similar L_{ch} and driving voltages. Although standardizing the crack formation process might be a daunting challenge provided the size distribution of the nanogaps, these results demonstrate unambiguously that synthetic 2D electronics can indeed provide the ultrascaling capability, together with excellent device performances.

5 Conclusion and outlook

In summary, we have reviewed recent developments on synthetic nanostructures and heterostructures targeting for transistor scaling. We demonstrate by showcasing some milestone works that, chemical approaches that utilize bottom-up synthesis, if well controlled, could provide unparallel precision in regulating the composition and structure of electronic nanosystems, in particular, for downscaling 2D transistors. In Fig. 8, we extract the key figures of merit for 2D transistors, either lithographically fabricated or chemically synthesized, reported in some representative works. It can be seen that the incorporation of chemical synthesis indeed accelerates the scaling trend of 2D transistors, while maintaining their electrical performance competitive to nanofabricated devices. However, challenges for synthetic 2D electronics remain to be addressed in the following aspects: (i) more general and precise synthetic strategies are yet to be developed, especially for constructing those ultrascaled nanostructures; (ii) new device physics associated with ultrascaling are still elusive and are limited by the size and quality of current synthetic nanodevices; (iii) trade-off between structure precision and growth rate is difficult, since high-rate growth is generally dynamics-controlled and manifests low atomic precision at the growth front; (iv) integration scale and complexity for synthetic electronics seems unachievable simultaneously, because delicate electronics require a larger number of component materials and more complicated fabrication processes, thus hindering their batch production with satisfactory performance uniformity. In any sense, with the post-Moore era approaching and the semiconductor industry heading into the deep nanometer regime, synthetic electronics undoubtedly provide a new paradigm for device fabrication and transistor scaling, therefore boosting the development of next-generation nanoelectronics.

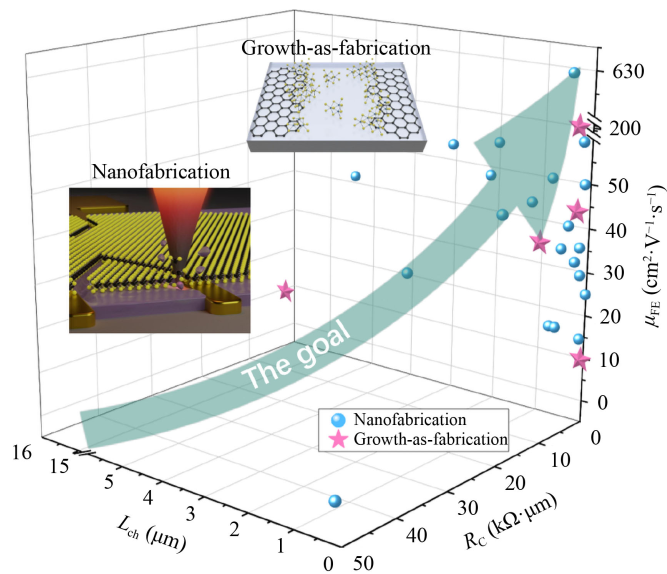

Fig. 8 Benchmarking 2D transistors. Three key parameters, namely channel length (L_{ch}, x-axis), contact resistance (R_C, y-axis) and field-effect mobility (μ_{FE}, z-axis), are extracted from previous works [47, 103, 105, 108–127]. The top right corner is the target being chased (stars: synthetic transistors; circles: nanofabricated transistors).

Acknowledgements This work was financially supported by the National Natural Science Foundation of China (No. 22205142) and the Science and Technology Commission of Shanghai Municipality (Nos. 21ZR1442100 and 21PJ1410200). The work was also supported by the Startup Fund and the Double First-Class Initiative Fund of ShanghaiTech University.

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