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COMMENT

Three-dimensional photonic neural networks: computing beyond the planar limit

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Photonic neural networks have long been recognized as a promising pathway toward next-generation high-speed and energy-efficient artificial-intelligence hardware. Unlike electronic processors, which increasingly face challenges from data movement, interconnect congestion, and energy dissipation, photonic systems can exploit propagation, interference, diffraction, and modal coupling to perform linear transformations with extremely low latency [1]. Over the past decade, hybrid optoelectronic accelerators [2], coherent interferometric meshes [3], and integrated photonic tensor cores [4] have demonstrated the native compatibility of optical systems with matrix–vector multiplication, convolution, and other operations central to modern neural-network workloads.

Existing photonic neural-network architectures face a fundamental trade-off among spatial parallelism, integration, scalability, and programmability, as summarized in Fig. 1. Free-space diffractive networks naturally exploit three-dimensional propagation and massive spatial parallelism, making them powerful platforms for optical image processing and parallel inference. However, they often require bulky optical paths, precise micrometre-scale alignment, and offer limited post-fabrication programmability. In comparison, integrated two-dimensional mesh networks provide compact footprints, single-chip integration, and electrical programmability, but their planar layouts constrain routing, interconnectivity, and direct processing of spatially structured data. Images are naturally two-dimensional, whereas many integrated photonic processors require them to be flattened or serialized before optical computation. This mismatch weakens optics' native spatial parallelism, one of its most powerful advantages.

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In a recent article in *Nature Communications*, Xinliang Zhang, Jianji Dong, and coworkers reported a programmable three-dimensional photonic neural-network chip that directly processes two-dimensional images on chip [5]. The device is fabricated in glass by femtosecond laser direct writing and consists of cascaded photonic-lantern waveguide arrays and phase-shifter arrays, forming a multilayer architecture for optical matrix operations. An eight-layer 8×8 prototype was reported to provide an architectural peak throughput of 6554 TOPS (trillions of operations per second, or tera-ops per second), 93% training accuracy on Modified National Institute of Standards and Technology (MNIST) classification, 91.7% test accuracy, and over 94% fidelity in optical pattern generation.

The key conceptual advance of this work is the transition from planar photonic computation to volumetric photonic computation. The authors use the internal volume of glass to construct three-dimensional waveguide networks instead of treating the chip surface as the only computational canvas. This is more than a geometric extension. In planar circuits, scaling is often achieved by adding waveguides, crossings, and routing paths, which rapidly increases layout complexity. In the reported architecture, an additional spatial degree of freedom for routing, coupling, and spatial mixing allows optical fields to evolve through a three-dimensional network before being reconfigured by phase-shifter arrays. This offers a physically intuitive route to increasing computational density without simply expanding the chip footprint.

A particularly attractive feature of the architecture is its combination of photonic-lantern-based mixing and active programmability. Photonic lanterns are well suited to connecting different spatial representations of light, transforming between multimode or spatially distributed fields and arrays of single-mode channels. Here, this concept is adapted for neural-network computation: the input image is coupled into a three-dimensional waveguide architecture in which propagation and inter-waveguide coupling participate directly in the computation, rather than serving only as

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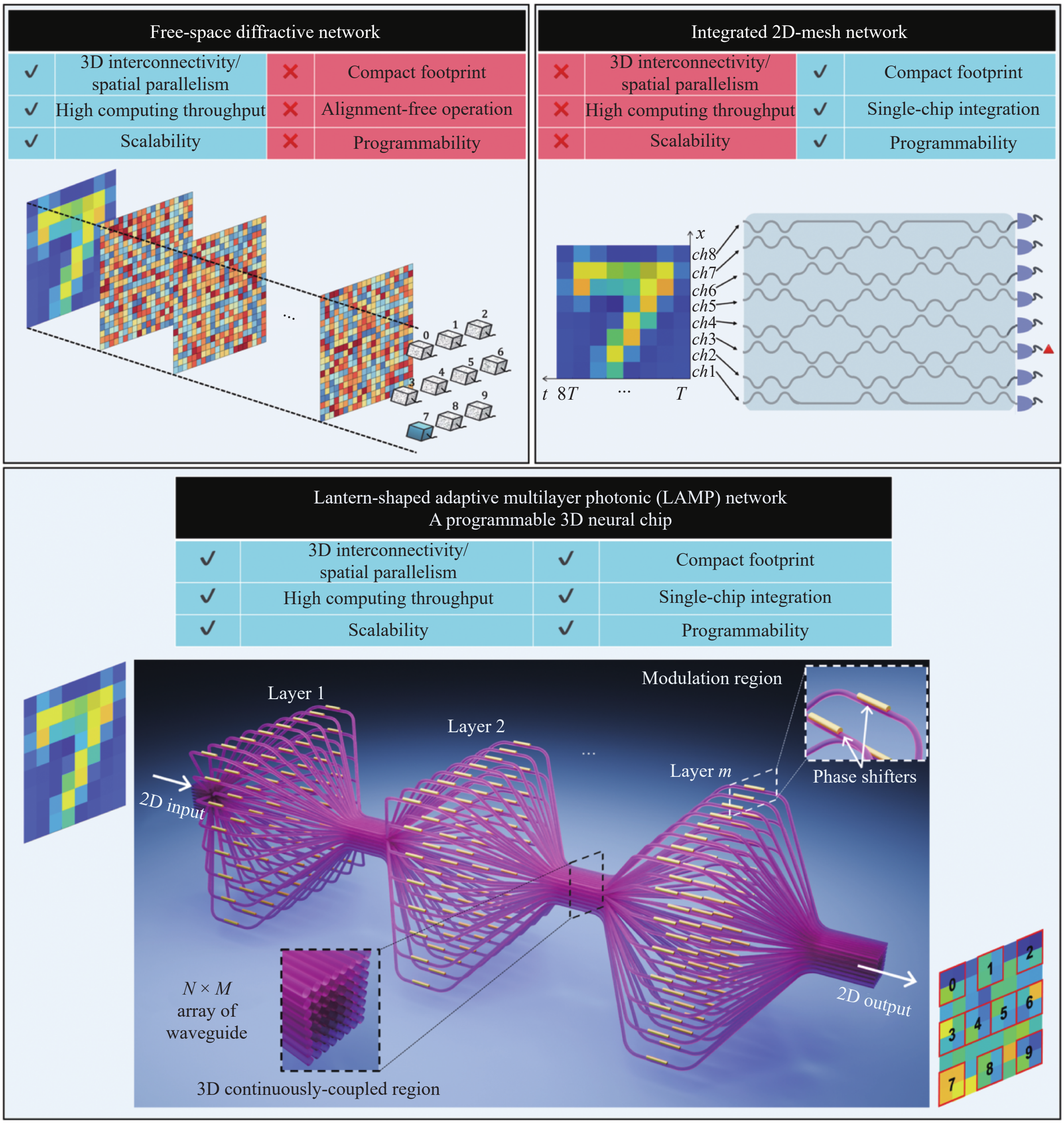

Fig. 1 From free-space and planar photonic neural networks to programmable three-dimensional photonic computing. Figure adapted with permission from Ref. [5].

preprocessing before conversion to a one-dimensional vector. Meanwhile, the integrated phase-shifter arrays enable task-specific reconfiguration and *in situ* optimization after fabrication. This hybrid strategy combines passive three-dimensional propagation for dense optical mixing with active modulation for programmability, avoiding both the rigidity of passive optical networks and the control complexity of fully interferometric mesh architectures.

The demonstrations of MNIST classification and optical pattern generation provide a clear proof of concept. Although MNIST is an early-stage benchmark rather than a stringent test of modern AI workloads, it remains useful for evaluating whether an optical system can implement trained transformations with sufficient stability, fidelity, and signal contrast. Importantly, the work demonstrates an integrated optical system that processes spatially structured inputs directly through a reconfigurable three-dimensional network, giving the architecture broader significance beyond the specific benchmark.

Looking forward, several questions remain open. As in many emerging photonic computing systems, future studies will need more comprehensive system-level evaluations, including light sources, modulation and detection, electronic control, calibration, and data movement. Scaling to larger networks will also require improved fabrication uniformity and loss management in deeply written glass waveguide arrays. Although femtosecond-laser-written glass provides a distinctive route to volumetric three-dimensional integration within a single substrate, increasing the writing depth can introduce spherical aberration and depth-dependent energy deposition, which should be mitigated through power compensation and wavefront correction. In the design of larger photonic networks, bend-induced radiation loss, path-length variations, and array-level insertion loss must be reduced through optimized routing, lower-curvature trajectories, and adiabatic bend designs. In addition, extending the present proof-of-concept demonstrations toward more complex visual tasks and deeper network models will be important for clarifying the most suitable application scenarios of this architecture. These challenges define the next stage of the work. By using the third dimension as a computational resource, this study opens a path toward optical processors that operate with the natural dimensionality and physical richness of optical visual information.

Author contribution All authors read and approved the final manuscript.

Declarations

Competing interests The authors declare that they have no competing interests.

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