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RESEARCH ARTICLE

Simulation study on the active layer thickness and the interface of a-IGZO-TFT with double active layers

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Abstract In this paper, ATLAS 2D device simulator of SILVACO was used for device simulation of inverted-staggered thin film transistor using amorphous indium gallium zinc oxide as active layer (a-IGZO-TFT) with double active layers, based on the density of states (DOS) model of amorphous material. The change of device performance induced by the thickness variation of each active layer was studied, and the interface between double active layers was analyzed. The best performance was found when the interface was near the edge of the channel, by optimizing the thickness of each active layers, the high performance device of threshold voltage (V_{th}) = −0.89 V, sub-threshold swing (SS)= 0.27, on/off current ratio (I_{ON}/I_{OFF}) = 6.98×10^{14} was obtained.

Keywords amorphous indium gallium zinc oxide (a-IGZO), double active layers, interface, density of states (DOS), ATLAS

1 Introduction

The recent discussion on amorphous oxide semiconductor (AOS) is extensive around the world. Thin film transistor using amorphous indium gallium zinc oxide as active layer (a-IGZO-TFT) has become one of the most popular topic due to its high mobility, high light transmission and low temperature process.

The electrical properties of a-IGZO-TFT are mainly determined by the contents of In and Ga in the active layer. On the one hand, the mobility of device enhances with the increase of In content, while the off current increases and the sub-threshold swing becomes worse at the same time. On the other hand, the increase of Ga content results in the decrease of off current and a better sub-threshold swing, but it also reduce the mobility of device. In order to resolve this problem, double active layer structures are proposed. In these structures, the material of high mobility and low electrical conductivity is used as front active layer, and the material of low mobility and high electrical conductivity is used as back active layer, such as IGZO/IGZO-N [1], IGZO/ZIO [2], ITO/IGZO [3], IGZO/CuGaInZnO [4], HfInZnO/HfInZnO (different In content) [5]. By using an ITO/IGZO double active stack, excellent TFT properties with a high mobility of 10^4 cm^2/(V·S), suitable threshold voltage (V_{th}) of 0.5 V, and a sub-threshold swing (SS) of 0.25 V/decade were demonstrated. Marrs et al. switched IGZO single layer structure to the IZO/IGZO dual active layer structure, the saturation mobility increased from 1.2 to 18 cm^2/(V·S) [2]. Maeng et al. effectively reduced the sub-threshold photocurrent by modulating the cation composition of the back channel layer [5]. As a result, the mobility of double active layers device is improved significantly compare to the single layer one, and the electrical stability has also been enhanced.

It is clear that the device with double active layers have better electrical performance. However, most researches of double active layer device only focused on some fixed structures, few of them take the thickness variation of each active layers and the interface between the two active layers into consideration. So we used ATLAS 2D device simulator of SILVACO for device simulation of inverted-staggered a-IGZO-TFT with double active layers, based on the density of states (DOS) model. In-rich front active layer was used to enhance the mobility and operating current, and the In-poor back active layer was used to improve the sub-threshold swing. The change of the device performance caused by modulating the thickness of each active layers and the position of the interface between the two active layers was investigated.

2 Device simulation

DOS we used in this paper is an important concept in

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amorphous thin film. It represents the number of states near some particular energy level. With Fermi-Dirac statistic, the effect carrier concentration of fixed material can be calculated. In a-IGZO system, the acceptor like conduction band-tail states g_{ta}, the donor-like valence band-tail states g_{td} and donor-like shallow-gap states g_{gd} are major factors influencing the performance. g_{ta} is known to originate from the disorder of metal cation s-bands and the conduction band minimum mainly consists of In 5s orbitals. As a result, g_{ta} increases with the increase of In content. Both g_{td} and g_{gd} are significantly affected by the oxygen vacancy. Since a Ga ion has a high ionic potential than In and Zn ions, it can combine the oxygen ions tightly. The formation of oxygen vacancies will be suppressed by the introduction of Ga. g_{td} and g_{gd} will decrease with the increase of Ga content. At last, the schematic of the proposed a-IGZO DOS model is shown in Fig. 1.

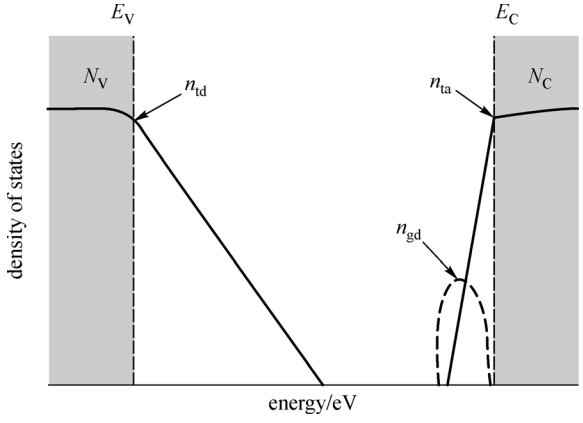

Fig. 1 Proposed density of states (DOS) model for a-IGZO. E_C and E_V are conduction and valence band edge energies, respectively. N_C and N_V are effective conduction and valence band DOS, respectively. Solid curves within the bandgap represent the exponentially distributed band-tail states (g_{ta}, g_{td}), while the dash curve near the conduction band edge represents the Gaussian-distributed donor-like oxygen vacancy (OV) states (g_{gd})

The exponentially distributed band-tail states (g_{ta}, g_{td}), and the Gaussian-distributed donor-like OV states (g_{gd}) are represented as a function of energy by the following expressions:

$$g_{ta}(E) = n_{ta}\exp[(E-E_C)/w_{ta}], \quad (1)$$

$$g_{td}(E) = n_{td}\exp[(E_V-E)/w_{td}], \quad (2)$$

$$g_{gd}(E) = n_{gd}\exp[-(E-E_{gd})^2/w_{gd}^2], \quad (3)$$

where E_C and E_V are conduction and valence band edge energies, n_{ta} and n_{td} are densities of states at $E = E_C$ and $E = E_V$, respectively, w_{ta} and w_{td} are characteristic slopes of conduction and valence band-tail states, respectively. n_{gd}, E_{gd} and w_{gd} are the peak value, the mean energy, and standard deviation of states, respectively.

The device architecture we adopted in simulation is illustrated in Fig. 2. The TFT is simulated with a bottom-gate inverted staggered design, the active layer consists of two thin films with a cumulative thickness of 40 nm. The gate insulator layer we used is 80 nm thick thermal SiO_2, and the channel width/channel length (W/L) is 180 μm/30 μm.

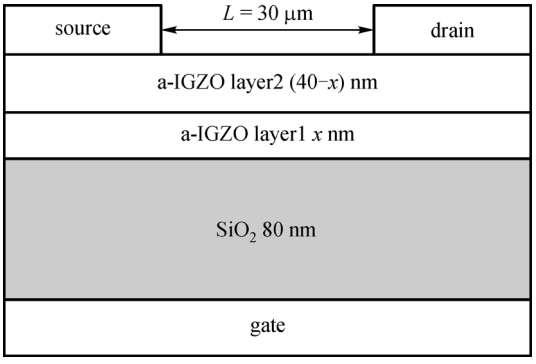

Fig. 2 Schematic of the TFT structure we adopt in this paper

To model the device, the homogeneous Neumann boundary condition was applied to the back-channel surface of the a-IGZO layer2. Such boundary condition prevents carriers from flowing outside of the back-channel surface and ensures that the current only flows in/out of the device through source/drain (S/D) contacts during simulation. Since the degenerate conduction might occur in the a-IGZO TFT, the Fermi-Dirac statistic was used in the active layer simulation. Contacts between S/D electrodes and the a-IGZO layer were assigned as ohmic in this work. Both thermionic emission and tunneling current are considered.

Since the overlap between the s-orbital in multi-component oxides affects the mobility and In content are more effective in s-orbital overlapping, the increase of the In content can increase the mobility [6]. To date, a-IGZO has an electron band mobility ranging from 10 to 20 $cm^2/(V \cdot s)$ in some researches [7–12], and the electron band mobility of a-IZO (indium zinc oxide) can reach 59 $cm^2/(V \cdot s)$ [13]. For high In content and negligible Ga content in layer1, we set the electron band mobility of layer1(In:Ga:Zn ≈ 1:0:1 in atomic ratio) to 50 $cm^2/(V \cdot s)$. And we set the electron band mobility of layer2 (In:Ga:Zn = 1:1:1 in atomic ratio) to 15 $cm^2/(V \cdot s)$.

There are many different factors that influence the DOS of material, including the process conditions, the content of each constituent element, and so on. We focused on the influence of different constituent elements content on DOS in this work. We consider the fact that the DOS has a continuous distribution from tail states to extended states. Therefore, it is reasonable for N_C (effective conduction band DOS) (or N_V (effective valence band DOS)) and n_{ta} (or n_{td}) to have a proportional relation. Since N_C of a-IGZO

(around $5 \times 10^{18}\,cm^{-3}$) is about an order smaller than a-Si:H (around $3 \times 10^{19}\,cm^{-3}$), we assumed n_{ta} of a-IGZO to be around $10^{20}\,cm^{-3}\cdot eV^{-1}$($n_{ta}$ for a-Si:H is $10^{21}\,cm^{-3}\cdot eV^{-1}$) [8]. Since there are more In and less Ga in layer1 than layer2, and the DOS theory we mentioned above, the n_{ta}, n_{td} and n_{gd} of layer1 are higher than layer2. We set both the n_{ta}, n_{td} of layer1 to $2 \times 10^{20}\,cm^{-3}\cdot eV^{-1}$ (n_{ta}, n_{td} of layer2 are both $1.55 \times 10^{20}\,cm^{-3}\cdot eV^{-1}$). We set the n_{gd} of layer1 to $3 \times 10^{17}\,cm^{-3}\cdot eV^{-1}$ (n_{gd} of layer2 is $6.5 \times 10^{16}\,cm^{-3}\cdot eV^{-1}$).

To calculate the electron affinity, we estimated $\chi_{a\text{-IGZO}}$ from a simple linear relation between electron affinities of its three elementary compounds [8]:

$$\chi_{a\text{-IGZO}} = a * \chi_{In_2O_3} + b * \chi_{Ga_2O_3} + c * \chi_{ZnO}, \qquad (4)$$

where a, b and c are molar percentages (mol %); $\chi_{In_2O_3}$, $\chi_{Ga_2O_3}$ and χ_{ZnO} are 4.45, 3.19 and 4.5 eV, respectively. For layer2, In:Ga:Zn = 1:1:1 (a, b and c are 0.25, 0.25 and 0.5, respectively), $\chi_{a\text{-IGZO}}$ is calculated to be 4.16 eV. For layer1, the content of Ga is negligible, so In:Ga:Zn = 1:0:1 (a, b and c are 0.33, 0 and 0.67, respectively), $\chi_{a\text{-IGZO}}$ is calculated to be 4.48 eV.

The key simulation parameters in this study are summarized in Table 1.

3 Results and discussion

We designed the IGZO-TFT with two active layers with different thickness, and different x (thickness of layer1) represent the variation of device thickness. Schematic of the TFT structure is shown in Fig. 2. Layer1 is the thin layer around the gate insulator, and layer2 is the back layer on the layer1. The active layer consists of these two layers with a cumulative thickness of 40 nm, x = 0 nm and x = 40 nm represent the TFT with 40 nm layer2 as active layer and the TFT with 40 nm layer1 as active layer respectively. We simulated each device, and the transfer characteristic curves are shown in Fig. 3.

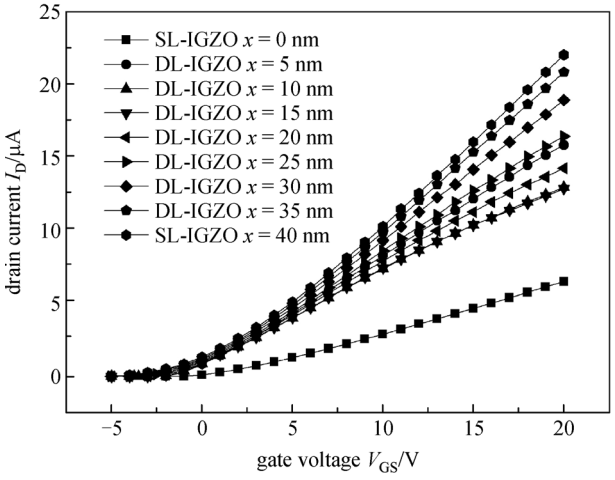

Fig. 3 Transfer characteristic curves of IGZO-TFT with different x (DL and SL represent double layers and single layer, respectively)

Then, we analyzed the result with the "extract" function of atlas, which is based on the standard metal-oxide-semiconductor field-effect transistor (MOSFET) equation. The threshold voltage (V_{th}), sub-threshold swing (SS), on/off current ratio (I_{ON}/I_{OFF}), minimum drain current (I_{Dmin}) and maximum drain current (I_{Dmax}) are listed in Table 2.

According to Table 2,when x = 40 nm (TFT with layer1 as active layer), the device has a maximum I_{Dmax} but a relatively bad performance in sub-threshold region because both mobility, density of tail states and donor-like states of layer1 are higher than layer2. On the contrary, the device has a minimum I_{Dmax} but a relatively good performance in sub-threshold region when x = 0 nm (TFT with layer2 as active layer).The I_{Dmax} of the other devices are between them, but the performances in sub-threshold region are better than them. The result is similar to other papers of TFT with double active layers [1 – 5].This is because that

Table 1 Key simulation parameters of a-IGZO (based on Ref. [8])

symbol	layer1	layer2	unit	description
n_{ta}	2×10^{20}	1.55×10^{20}	$cm^{-3}\cdot eV^{-1}$	density of tail states as $E = E_C$
n_{td}	2×10^{20}	1.55×10^{20}	$cm^{-3}\cdot eV^{-1}$	density of tail states as $E = E_V$
w_{ta}	0.013	0.013	eV	conduction-band-tail slope
w_{td}	0.12	0.12	eV	valence-band-tail slope
n_{gd}	3×10^{17}	6.5×10^{16}	$cm^{-3}\cdot eV^{-1}$	peak of OV states
E_{gd}	2.9	2.9	eV	mean energy of OV states
w_{gd}	0.1	0.1	eV	standard deviation of OV states
χ	4.48	4.16	eV	electronic affinity
μ_n	50	15	$cm^2/(V\cdot s)$	band mobility (electron)
μ_p	0.1	0.1	$cm^2/(V\cdot s)$	band mobility (hole)
E_g	3.25	3.05	eV	bandgap

Table 2 Electrical properties of each a-IGZO TFT with different x

symbol	x of a-IGZO layer1/nm									unit
	0	5	10	15	20	25	30	35	40	
V_{th}	2.26	−0.41	−0.88	−0.89	−0.66	−0.23	0.36	1.16	1.72	V
SS	2.27	1.99	0.46	0.27	5.22	5.46	5.76	6.01	6.25	V/decade
I_{ON}/I_{OFF}	2.22	2.2	17.5	69.8	14.5	1.37	0.02	10^{-9}	10^{-9}	10^{13}
I_{Dmin}	2.96	7.27	0.74	0.18	0.99	12.12	955	10^{10}	10^{10}	10^{-19}A
I_{Dmax}	6.51	16	13	12.9	14.3	16.6	19.1	21	22.1	10^{-6}A

the TFT using high mobility material as front channel, the drain current is increased when the device is on. While with low mobility material as back channel, the drain current is decreased when the device is off.

Then, we considered the variation of threshold voltage, we found that, by introducing 5 nm layer1, the threshold voltage is suddenly changed from 2.26 V (x = 0 nm) to −0.41 (x = 5 nm). This is because that the main charge conductance channel is around the gate insulator interfaces [3], the 5 nm layer1 is either in this area or contains this area. As a result, the main charge conductance of x = 5 nm device has a higher mobility and density of defect states than that of x = 0 nm device , due to the high mobility and density of defect states, the channel region can be formed when low negative gate bias or no gate bias is applied. When x increases (ranging from x = 0 to 15 nm), the threshold voltage decreases (the absolute value is increased). We thought that the main charge conductance channels in this situation are layer1 and the interface region between layer1 and layer2 (since the interface between layer1 and layer2 is something like heterojunction, there is lattice mismatch between two layers, the dangling bonds will appear in the interface between two layers. That means interface trap density is introduced, and some carriers will accumulate in the interface [14]). Because of the increase in the thickness of layer1, the total density of defect states in the whole active layer are increased, the number of carriers in conductive areas is increased; a more negative gate bias is required to turn off the TFT by depleting the carriers from the conductive areas [5]. The threshold voltage is increased with the increase in x (ranging from x = 15 to 40 nm). We thought the main charge conductance channels in this situation are some part of layer1 near gate insulator and the interface region between layer1 and layer2; with the increase in the thickness of layer1, the interface between layer1 and layer2 is no longer near the gate insulator. The carriers only accumulate in the some part of layer1 near the gate insulator when positive gate voltage is applied, and relatively low negative gate bias (or even positive gate bias) is required to turn off the device.

On the other hand, the sub-threshold swing (SS) and on/off current ratio (I_{ON}/I_{OFF}) showed the same trend on x, the electrical performance improves when x increases from 0 to 15 nm, but declines when x increases from 15 to 40 nm. We thought that the electrical performance of device is determined by relative position between the main charge conductance channels (the active layer near the gate insulator) and the interface (between layer1 and layer2).

Further studies have been carried out on the influence of gate voltage on the distribution of carriers. We found similar characteristics of each device. For instance, we simulated the device of x = 10, 15 and 20 nm. The distribution of carriers in the whole active layer when −5 and 20 V gate voltages are applied respectively are illustrated as Figs. 4 and 5.

It can be seen from Figs. 4 and 5 that carriers will accumulate in the interface between two layers when negative gate voltage is applied. On the other hand, carriers will accumulate in the interface between two active layers and the areas of layer1 near gate insulator when positive gate voltage is applied.

So we infer that the device with the interface (between layer1 and layer2) located in or near the main conductive channel has a low turn-on voltage because there already is large number of carriers in main conductive channel when positive gate voltage is applied. And it also has a good electrical performance as most of the carriers can get through the interface between layer1 and layer2 when negative gate voltage is applied; even when the carriers accumulate in the high resistive back active layer, the drain current that occurs is negligible, that means a low turn-off current. On contrary, the device with the interface (between layer1 and layer2) located far from the main conductive channel has a higher turn-on current because there are relatively more carriers ranging from the main conductive channel to the regions between layer1 and layer2, which have a low resistive. But when negative voltage is applied, most of the carriers may accumulate in the regions near the interface between layer1 and layer2, such regions have a relatively low resistive, so relatively large drain current will occur, that means a large turn-off current and poor electrical performance. By adjusting the thickness of layer1, we found a best device performance in x = 15 nm (V_{th} = −0.89 V, SS = 0.27, I_{ON}/I_{OFF} = 6.98 × 10^{14}).

4 Conclusions

The thickness variation of each active layer in a-IGZO TFT with double layers and the interface between two active

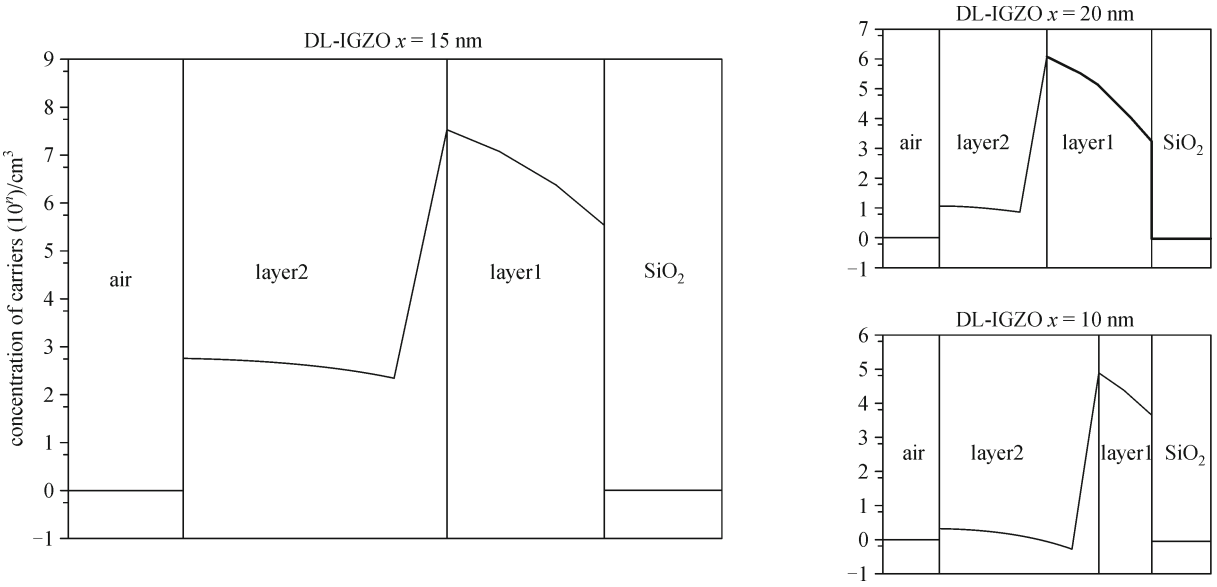

Fig. 4 Carrier distribution of carriers when –5 V gate voltage is applied

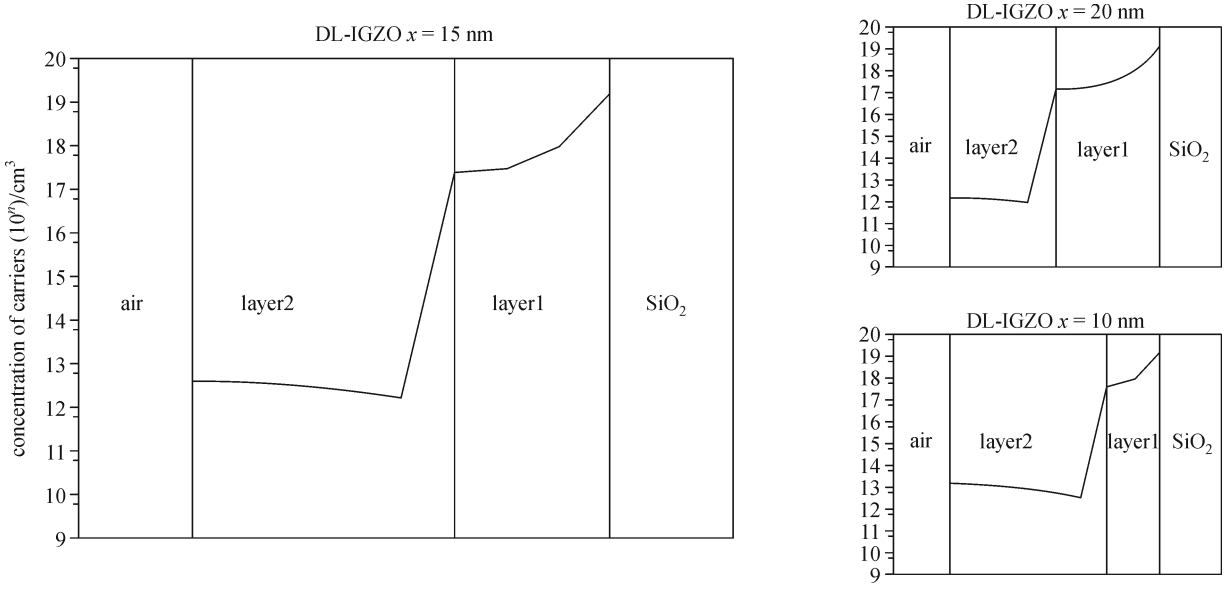

Fig. 5 Carrier distribution of carriers when 20 V gate voltage is applied

layers has been studied in this paper. It is found that the main conductive regions in double layer device are some active layer areas near gate insulator and the areas near the interface between two active layers. When negative voltage is applied, most of the carriers will accumulate in the interface between two active layers. On the other hand, most of the carriers will accumulate in the interface between two active layers and the areas of layer1 near gate insulator when positive gate voltage is applied. The electrical performance of device changes with the changing location of the interface between two active layers and we found the best performance of $V_{th} = -0.89$ V, $SS = 0.27$, $I_{ON}/I_{OFF} = 6.98 \times 10^{14}$ when $x = 15$ nm.

References

1. Liu P T, Chou Y T, Teng L F, Li F H, Fuh C S, Shieh H P D. Ambient stability enhancement of thin-film transistor with InGaZnO capped with InGaZnO:N bilayer stack channel layers. IEEE Electron Device Letters, 2011, 32(10): 1397–1399
2. Marrs M A, Moyer C D, Bawolek E J, Cordova R J, Trujillo J,

Raupp G B, Vogt B D. Control of threshold voltage and saturation mobility using dual-active-layer device based on amorphous mixed metal–oxide–semiconductor on flexible plastic substrates. IEEE Transactions on Electron Devices, 2011, 58(10): 3428–3434

3. Kim S I, Kim C J. High performance oxide thin film transistors with double active layers. In: Proceedings of IEEE International Electron Devices Meeting, 2008
4. Kim S I, Park J S, Kim C J, Park J C, Song I, Park Y S. High reliable and manufacturable gallium indium zinc oxide thin-film transistors using the double layers as an active layer. In: Journal of the Electrochemical Society, 2009, 156(3): H184–H187
5. Maeng W J, Park J S, Kim H S, Lee K H, Park K B, Son K S, Kim T S, Kim E S, Ham Y N, Ryu M, Lee S Y. Photo and thermal stability enhancement of amorphous Hf-In-Zn-O thin-film transistors by the modulation of back channel composition. Applied Physics Letters, 2011, 98(7): 073503
6. Kim C E, Moon P. Density-of-states modeling of solution-processed InGaZnO thin-film transistors. IEEE Electron Device Letters, 2010, 31(10): 1131–1133
7. Kim Y, Bae M, Kim W, Kong D, Jung H K, Kim H, Kim S, Kim D M, Kim D H. Amorphous InGaZnO thin-film transistors—part I: complete extraction of density of states over the full subband-gap energy range. IEEE Transactions on Electron Devices, 2012, 59(10): 2689–2698
8. Fung T C, Chuang C S, Chen C, Abe K, Cottle R, Townsend M, Kumomi H, Kanicki J. Two-dimensional numerical simulation of radio frequency sputter amorphous In-Ga-Zn-O thin-film transistors. Journal of Applied Physics, 2009, 106(8): 084511
9. Bae H, Choi H, Oh S, Kim D H, Bae J, Kim J, Kim Y H, Kim D M. Extraction technique for intrinsic subgap DOS in a-IGZO TFTs by de-embedding the parasitic capacitance through the photonic *C–V* measurement. IEEE Electron Device Letters, 2013, 34(1): 57–59
10. Bae M, Lee K M, Cho E S, Kwon H I, Kim D M, Kim D H. Analytical current and capacitance models for amorphous indium-gallium-zinc-oxide thin-film transistors. IEEE Transactions on Electron Devices, 2013, 60(10): 3465–3473
11. Kim Y, Kim S, Kim W, Bae M, Jeong H K, Kong D, Choi S, Kim D M, Kim D H. Amorphous InGaZnO thin-film transistors—part II: modeling and simulation of negative bias illumination stress-induced instability. IEEE Transactions on Electron Devices, 2012, 59(10): 2699–2706
12. Bae M, Kim Y, Kong D, Jeong H K, Kim W, Kim J, Hur I, Kim D M, Kim D H. Analytical models for drain current and gate capacitance in amorphous InGaZnO thin-film transistors with effective carrier density. IEEE Electron Device Letters, 2011, 32 (11): 1546–1548
13. Kim H S, Park J S, Jeong H K, Son K S, Kim T S, Seon J B, Lee E, Chung J G, Kim D H, Ryu M, Lee S Y. Density of states-based design of metal oxide thin-film transistors for high mobility and superior photostability. Applied Materials Interfaces, 2012, 4(10): 5416–5421
14. Oldham W G, Milnes A G. Interface states in abrupt semiconductor heterojunctions. Solid-State Electronics, 1964, 7(2): 153–165

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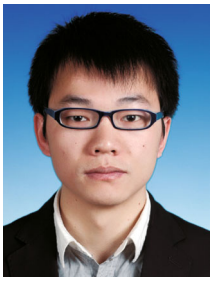

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