

Texturization and rounded process of silicon wafers for heterojunction with intrinsic thin-layer solar cells

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Abstract Heterojunction with intrinsic thin-layer (HIT) solar cells are sensitive to interface state density. Traditional texture process for silicon solar cells is not suitable for HIT one. Thus, sodium hydroxide (NaOH), isopropanol (IPA) and mixed additive were tentatively introduced for the texturization of HIT solar cells in this study. Then, a mixture including nitric acid (HNO₃), hydrofluoric acid (HF) and glacial acetic acid (CH₃COOH) was employed to round pyramid structure. The morphology of textured surface and the influence of etching time on surface reflectance were studied, and the relationship between etching time and surface reflectance, vertex angle of pyramid structure was analyzed. It was found that the mixture consisting of 1.1 wt% NaOH, 3 vol% IPA and 0.3 vol% additives with etching time of 22.5 min is the best for HIT solar cells under the condition of 80°C. Uniform pyramid structure was observed and the base width of pyramid was about 2–4 μm. The average surface reflectance was 11.68%. Finally the effect of different processes on the performance of HIT solar cells was investigated. It was shown that these texturization and rounding techniques used in this study can increase short circuit current (J_{sc}), but they have little influence on fill factor (FF) and open circuit voltage (V_{oc}) of HIT solar cells.

Keywords texturization, reflectance, pyramid, heterojunction with intrinsic thin-layer (HIT) solar cells

1 Introduction

Conventional crystalline silicon (c-Si) solar cells suffer from high processing temperature (800°C–900°C) and sophisticated process. Both are obviously detrimental for

the costs of production [1]. A underlying cheap alternative to c-Si solar cells is thin film silicon based heterojunction with intrinsic thin-layer (HIT) solar cells, consisting of hydrogenated amorphous silicon (a-Si:H). The advantages of HITs are simple structure, simple process, high efficiency, high stability and low cost [2]. The first c-Si/a-Si:H heterojunction structure was studied in 1974 by Fuhs et al. [3]. An essential breakthrough came with the introduction of a thin buffer layer of a-Si:H between wafer and doped emitter, a so-called HIT structure, to reduce the interface state density. This brought the efficiency of cells up to 14.5% [4]. Recently, Panasonic Corporation has announced a record conversion efficiency of 24.7% at the research level, for its HIT solar cell with thin Si substrate of 98 μm thickness [5].

Texturization is an important process for HIT solar cells as same as for silicon solar cells. By this texturization, pyramid structure can be formed on silicon surface. The pyramid structure can make surface reflectance reduced, thus the loss of light can be declined and device current output can be improved. A variety of basic solutions such as sodium hydroxide (NaOH) [6,7], potassium hydroxide (KOH) [8], trisodium orthophosphate (Na₃PO₄) [9], sodium metasilicate (Na₂SiO₃) [10], tetramethylammonium hydroxide (TMAH) [11], sodium carbonate (Na₂CO₃) [12], and sodium bicarbonate (NaHCO₃) [12] have been used for texturization. In those texturization processes, there is a big gap between large pyramids and small pyramids, and small pyramids can be easily founded on the boundary of large pyramids. The inconformity in size, shape and distribution of pyramids can also be observed by those traditional texturization processes. Compared with traditional Si solar cells, HIT solar cells are very sensitive to interface state density. The improvements of both traditional texture method and the previous rounded process are crucial to increase the convert efficiency of HIT solar cells.

In this paper, we mixed a kind of complex additives with NaOH and isopropanol (IPA) for texturization. The relationship between etching time and surface reflectance was investigated. The pyramid structure with conformity size, shape and distribution was achieved. The acid solution, which was introduced to etching the pyramid structure, can efficiently round the pyramid. It was found that both texturization and rounding processes can increase the short circuit current (J_{sc}) of HIT solar cells. These results give a process direction for silicon surface texturization of HIT solar cells in industry.

2 Experiments

The c-Si substrates (FZ, N-type, $1-10 \Omega \cdot \text{cm}$) with (100) surface orientation were used. Before texturization, the c-Si substrate was cleaned with acetone and alcohol (analytical reagent) in ultrasonic cleaning equipment, in order to wipe off organic contaminations. For wafer saw damage etching, 10 wt% NaOH was used at 80°C for 150 s. For the pyramidal texturing, 1.1 wt% NaOH solution with 3 vol% IPA as a wetting agent and 0.3 vol% additives were used. Following etching in NaOH, the wafers went with an RCA2 clean, or both RCA2 clean and acid etching. The RCA2 solution consisted of 1:1:6 HCl : H_2O_2 : H_2O , heated to 80°C for 10 min. Following wafer surface treatment, the samples were immediately transferred into plasma enhanced chemical vapor deposition (PECVD) and a-Si:H buffer layers were deposited on the both sides of the wafer. Then, a pa-Si:H layer was deposited on the front, and an n^+ a-Si:H layer was deposited on the back. Finally, the contacts were attached, consisting of indium tin oxide (ITO) and Al grids on the front, and a full coverage of Al on the back. The surface morphology of the wafers was analyzed with a SUPERTM 55VP scanning electron microscope (SEM). The reflectance of the textured silicon surfaces were measured from 400 to 1100 nm by equipment with an integrating sphere. The current–voltage characteristics (I - V) of the HIT solar cells were measured under calibrated $100 \text{ mW}/\text{cm}^2$ AM 1.5G irradiance at room temperature (25°C). This illumination was provided with a solar simulator (Oriol Sol2A ABA). The main photovoltaic parameters including short circuit current (J_{sc}), open circuit voltage (V_{oc}), fill factor (FF) and transfer efficiency (η) were got in the usual way.

3 Results and discussion

3.1 Effect of additives on texturization

For convenience, the reading number at 950 nm wavelength was used to indicate the reflectance of a measured point [13]. To evaluate the uniformity of the reflectance, five spots were measured across the surface of each sample

wafer and then an average value along with standard deviation was calculated, as show in Fig. 1. With the increase of etching time, the standard deviation showed a trend of decrease after the increase. Gosálvez and Nieminen had developed a mechanistic model to describe the nucleation and growth of pyramids during anisotropic etching of c-Si, and Monte Carlo simulation was used to calculate the texturing process with results coincident with published experimental observations [14]. The nucleation and growth of pyramids can be used to explain the standard deviation trends. During the first paragraph of the curve (14–16 min), the nucleation pyramids dominated the reaction. Some pyramids grown fast, become bigger than others. The reflectance shows inconformity. During the second paragraph of the curve (16–17.5 min), the nucleation and growth of pyramids tended to be balanced. Pyramid size changed toward uniform. The standard deviation showed a low numerical value. When it came to 22.5 min, the standard deviation was less than 0.1%. Pyramids distributed uniformly. The spectra of different wafers were shown in Fig. 2. Reflectance of textured samples was much lower than those polished and as-cut wafers for wavelengths between 400 and 1100 nm.

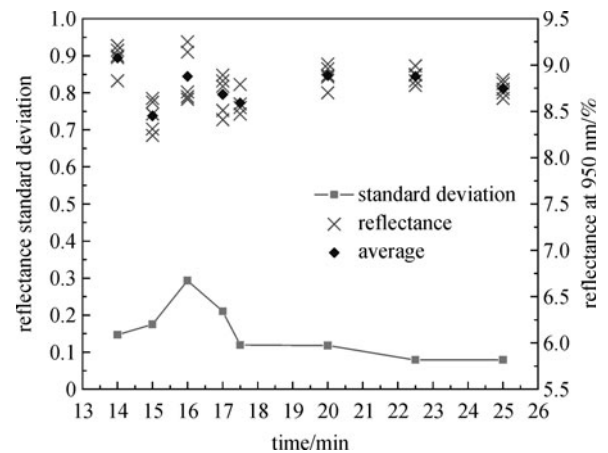


Fig. 1 Effects of etching time on the uniformity of reflectance across a wafer by five-point measurement

As HIT solar cells are sensitive to interface state density, the best etching time of HIT solar cells was 22.5 min using alkaline solutions to etch. SEM micrographs of HIT substrate sample with 22.5 min etching time were shown in Fig. 3. As it can be seen, pyramid structure completely covered the surface of silicon wafers and distributed uniformly. The gap between large pyramids and small pyramids is not big. The exceeding small pyramids on the boundary of large pyramids in traditional texture process can cause epitaxial grown [15]. A mixed phase of a-Si:H and epitaxial Si were proved invariably detrimental to the solar cell's V_{oc} , particularly when the mixed phase formed the back interface [16]. The exceeding small pyramids on the boundary of large pyramids were not found in Fig. 2.

Some process of HIT solar cells coincided with traditional crystalline silicon solar cells, so the size of pyramids used for silicon solar cells can also be applied to HIT solar cells. The base width of pyramids, which is lower than $4\ \mu\text{m}$, was demonstrated to be best for silicon solar cells [17]. The extreme small size of pyramid cannot be used, because it can be easily destroyed in follow-up processes. As it can be seen in Fig. 3, the base width of pyramids was about $2\text{--}4\ \mu\text{m}$. Only few pyramids were about 5 and $1\ \mu\text{m}$, the textured wafers can be used for HIT solar cells. The average surface reflectance is 11.68% , compared with 28.55% for as-cut sample and 43.72% for polished sample, which is smaller. It indicates that the reflectance characteristics of HIT substrate were improved using this texturing process.

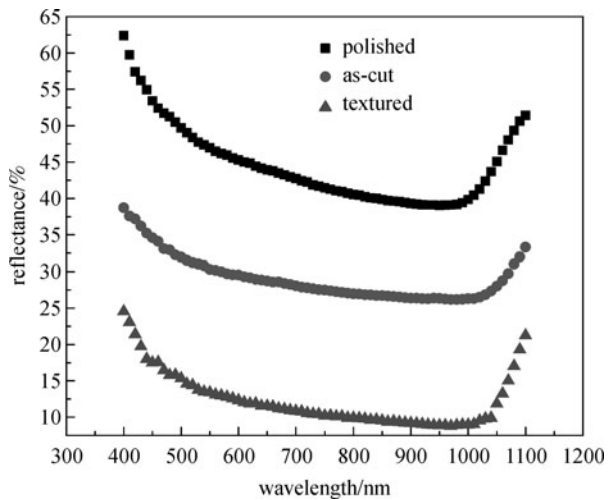


Fig. 2 Reflectance spectra of polished, as-cut and textured wafers

The mechanism of alkaline etching is shown below [18]:



As the density of silicon atoms of each crystal orientation is different, the etching rate of different crystal orientation with NaOH varies widely. The ratio of etching rate in the (100) orientation and (111) orientation is defined as anisotropic factor (AF). The AF depends on the etching temperature and the concentration of NaOH and IPA. When $\text{AF} = 1$, the etching rate of different orientation is close, flat wafer surface is reached. The reaction is used to etching the saw damage layer. When $\text{AF} = 10$, the pyramid structure formed by (111) orientation was corroded out through the reaction. When additives were added into alkaline solution, the etching process became less sensitive to the concentration of NaOH and IPA. Additives can also act as corrosion inhibitor in etching process. Then, AF and the growth of pyramid can be effectively controlled. Macromolecular organic matters and polymeric surfactants were contained in additives, which can work as nucleation agent in texturization and reduce the surface tension of the solution. Due to the controlling of nucleation and etching rate easily, pyramid size can be effectively controlled using the special additives as a buffer in corrosion solution.

3.2 Effect of acid etching time on wafer surface reflectance and vertex angles of pyramids

Figure 4 is the relationship between average reflectance of textured wafers and different etching time. The critical value of the vertex angle of pyramid should be mentioned, which is about 85° [19]. When the vertex angle is higher than the critical value, the reflectance of textured surface comes to a quickly increasing. After 2 s acid etching, the height of small pyramids dropped. The vertex angle of small pyramids increased and became higher than the

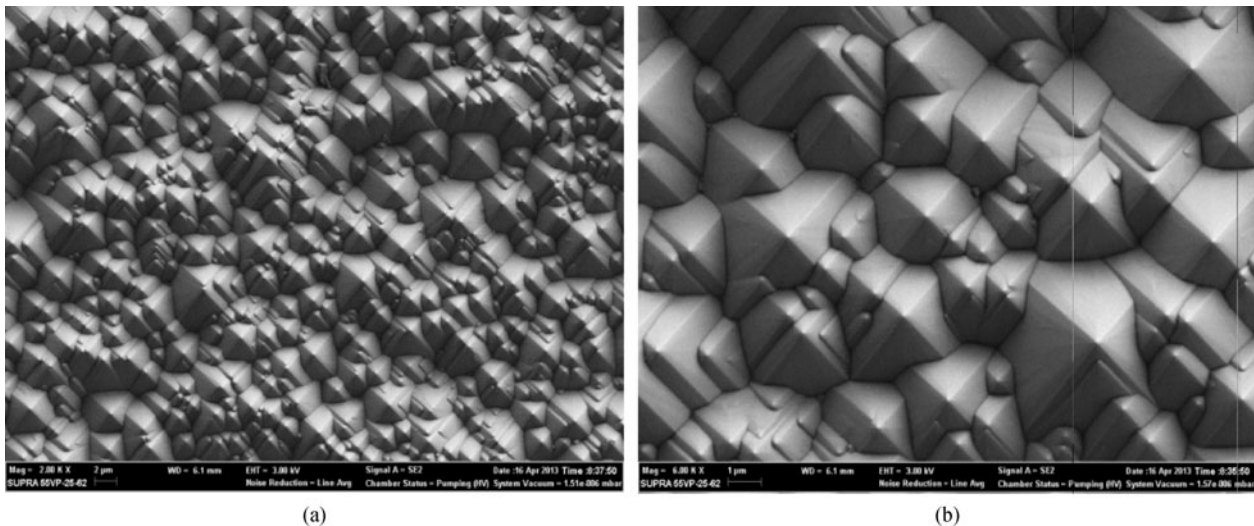


Fig. 3 SEM micrographs of silicon wafer with 22.5 min etching. (a) $\times 2000$; (b) $\times 6000$

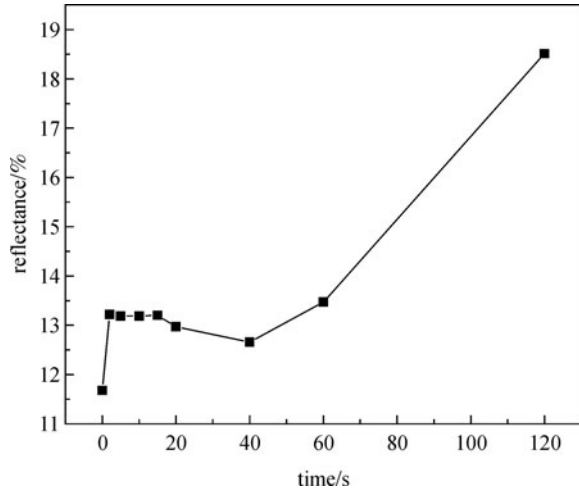
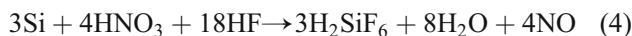
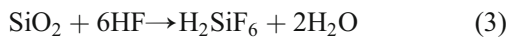
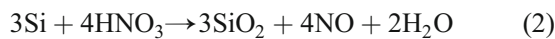


Fig. 4 Average reflectance of textured wafers at different etching times

critical value. The small pyramids lose their light trapping function, and the reflectance of silicon wafer increase to 13.62%. Prolonging the acid etching time to 60 s, the big pyramids act strongly against the etching, and the vertex angle of these pyramids was lower than the critical value. These pyramids also keep the function of light trapping, and the reflectance did not show any change. When the etching time was longer than 60 s, the vertex angle of some big pyramids became higher than the critical value. The reflectance keeps increasing. After 120 s' etching, the reflectance increased to 18.51%. SEM profiles of the textured wafers of different etching time were shown in Figs. 5(a)–5(d) corresponding to etching time 0, 2, 40 and 60 s respectively. For longer etching time, it can be observed the obvious reduction of pyramids height in Fig. 5(c), and compared with Figs. 5(a) and 5(b), the edges and corners of pyramids were also rounded. The vertex angle of pyramid was linearly increased from 78° to about 85° with etching time from 0 to 60 s. This further proved the critical value of the vertex angle we mentioned above is right.

Nitric acid (HNO_3), hydrofluoric acid (HF) and glacial acetic acid (CH_3COOH) mixture can etch silicon wafer in room temperature. The mechanism of acidic etching is shown below [20]:



First, SiO_2 occurs upon exposure to HNO_3 . Then, HF removes the oxidized layer, thereby forms H_2SiF_6 . At the same time, acetic acid acts as a buffer agent that prevents HNO_3 from decomposing into NO_3^- or NO_2^- [21]. A dilution with acetic acid also improves the wetting of the

hydrophobic c-Si surface and thus increases and homogenizes the etching rate.

The etching process typically involves the following steps: 1) transport of the reactants from the solution to the wafer surface, 2) effective reaction on the wafer surface, and 3) transportation of products from the wafer surface to the solution. Reactants had to pass through a stationary liquid film, which offers a constant resistance for mass-transfer before reactants reaches the surface of the wafer. Products also had to pass through the mass-transfer film. Hence, the mass-transfer film affects the etching rate. Figure 6 shows the influence of mass-transfer film on the acidic etching. The mass-transfer resistance is directly proportional to the thickness of the stagnant film. The mass-transfer resistance at the peaks (R_p) is lower than that at valleys (R_v) as a result of varying mass-transfer film thickness. Removal rates at peaks (V_p) are higher than that at valleys (V_v) [22]. As a result of selective etching at peaks and valleys, reduction in the height of pyramids is observed.

3.3 Effect of different processes on main photovoltaic parameters

As it can be seen in Fig. 7, in the cells made from polished wafer and textured wafer, J_{sc} increased when the substrates were textured, and V_{oc} and FF diminished. The increase of J_{sc} was mainly due to the trapping of light from pyramid structure. The reduction of V_{oc} and FF can be explained as follow: 1) HIT solar cells made with polished wafer and textured wafer had different effective cell thickness. HIT solar cells had strict demand for the thickness of a-Si:H, pa-Si:H and n^+ a-Si:H. A thinner a-Si:H layer passivates the c-Si surface inadequately, whereas the inadequate deposition thickness of the pa-Si:H layer suppresses the development of its specific microstructure and its corresponding high conductivity. Furthermore, the effective thickness is different in the peaks and the valleys. 2) V_{oc} diminished when the substrates were textured. This affect is attributed to an increase in recombination velocity, due to the rise of the effective surface area derived from the formation of the pyramids.

To improve the V_{oc} and FF of HIT cells with textured wafer, rounding process is introduced. In the cells made from textured wafer and rounded wafer, J_{sc} did not show any change, and the rounded wafer had better V_{oc} and FF than textured wafer. Either size reduction of pyramids or smoothing the pyramids is proved to be effective to decrease the contact resistance [23]. The contact resistance of the rounded wafer is lower than that of polished and textured wafer. The rounded process had little effect on reflectance. The decrease of the contact resistance and the increase of the reflectance can explain the change of J_{sc} . The acid etching process can reduce the height of pyramids and round the edges and corners of pyramids. The rounded pyramids promotes a proper a-Si:H deposition and a better

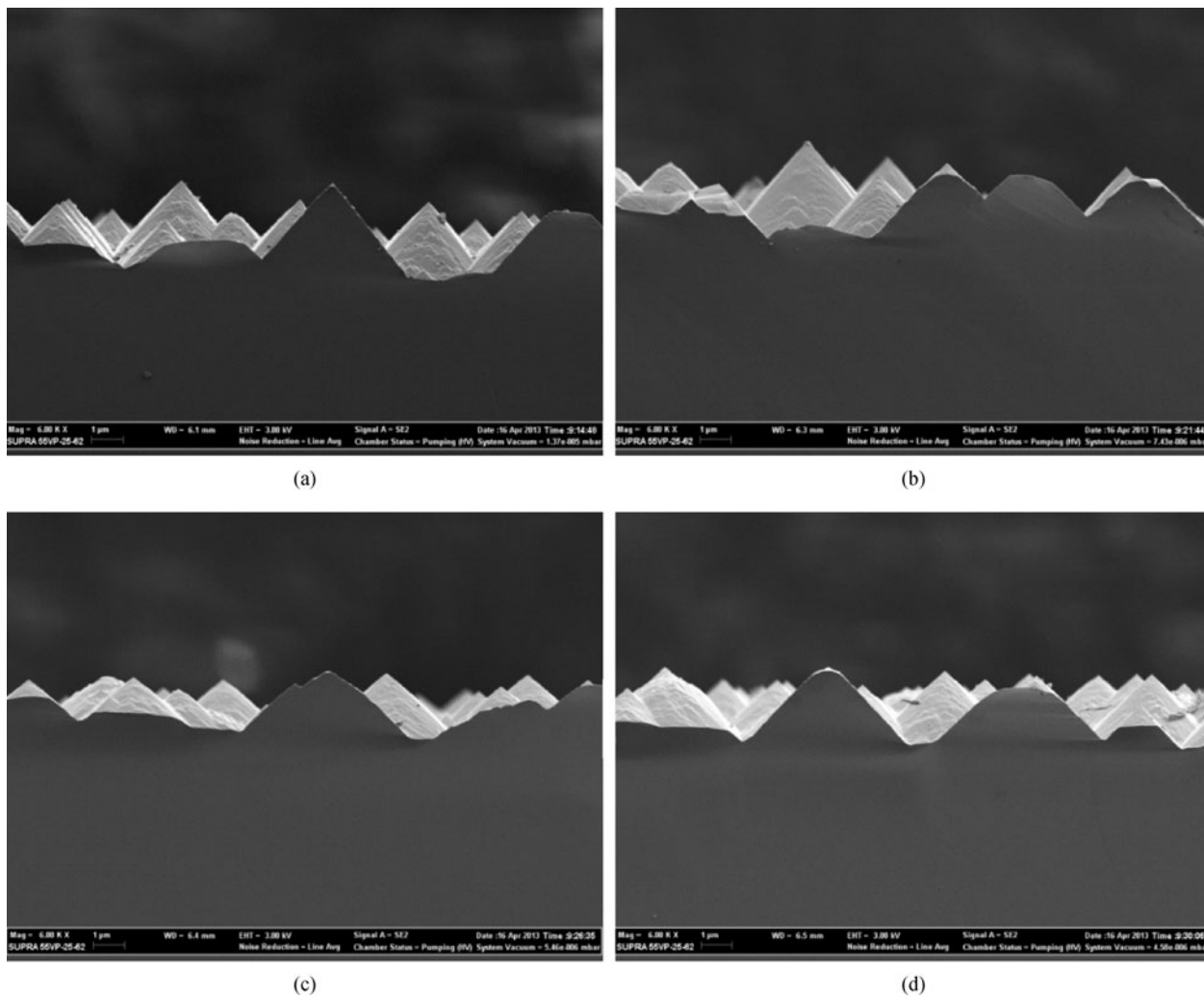


Fig. 5 SEM profiles of textured wafers for different etching times. (a) 0 s; (b) 2 s; (c) 40 s; (d) 60 s

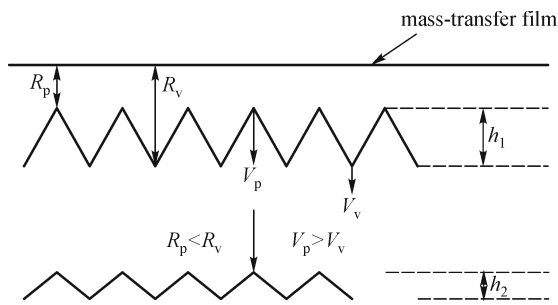


Fig. 6 Mass-transfer influenced etching

surface passivation. The post treatment restrained the negative influence imported by texturization. The rounded process has an evident improvement of V_{oc} and FF of solar cells; therefore it is an effective approach to promote characteristics of HIT solar cell with textured structure. It can also be used in other silicon solar cells including c-Si and poly-Si solar cells.

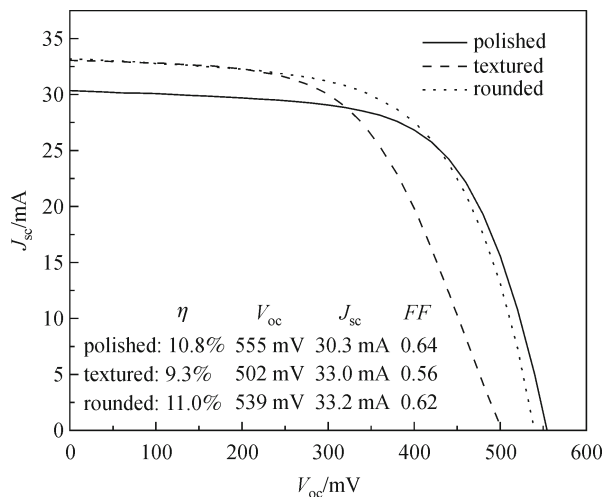


Fig. 7 $I-V$ curves of solar cells on polished wafer, and textured wafers with or without rounded process

4 Conclusions

The buffer additives were introduced into NaOH and IPA etching solution in textured process of HIT cell. Reflectance measurement and SEM photos showed that the additives can effectively increase the uniform of pyramid structure, reduce the etching time and the reflectance. Uniform pyramid structure was observed. The average surface reflectance from 400–1100 nm is 11.68%. The base width of pyramid is about 2–4 μm . The optimized texturization and rounding technique of HIT solar cell was reached. Texturization can effectively increase the short circuit current J_{sc} of HIT solar cells. J_{sc} of the cell made by textured wafer increases about 2.7 mA, which compared with the cell made by polished wafer. The rounded process has an evident improvement of V_{oc} and FF of cell. V_{oc} and FF of the cell made by rounded wafer increases about 53 mV and 0.08 respectively, compared with the cell made by textured wafer. It is an effective way to promote characteristics of HIT solar cell using texturization and rounding technique.

Acknowledgements This work was supported by Ministry of Education of China (No. 62501040202) and the Special Fund for the Development of Strategic Emerging Industries of Shenzhen, China (No. JCYJ20120831110939098). We thank all members of the thin films group at the Photonics and Information System Integration Institute and Hisunpy Technology Co., Ltd for their support of this work and helpful discussion. We also acknowledge the Analytical and Testing Center of Huazhong University of Science and Technology for SEM spectra measurements and Wuhan National Laboratory for Optoelectronics for the reflectance spectra measurement.

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