

High performance of low voltage controlled ring oscillator with reverse body bias technology

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Abstract In complementary metal oxide semiconductor (CMOS) nanoscale technology, power dissipation is becoming important metric. In this work low leakage voltage controlled ring oscillator circuit system was proposed for critical communication systems with high oscillation frequency. An ideal approach has been presented with substrate biasing technique for reduction of power consumption. The simulation have been completed using cadence virtuoso 45 nm standard CMOS technology at room temperature 27°C with supply voltage $V_{dd} = 0.7$ V. The simulation results suggest that voltage controlled ring oscillator has characterized with efficient low power voltage controlled oscillator (VCO) in term of minimum leakage power (1.23 nW) and maximum oscillation frequency (4.76 GHz) with joint positive channel metal oxide semiconductor and negative channel metal oxide semiconductor (PMOS and NMOS) reverse substrate bias technique. PMOS, NMOS and joint reverse body bias techniques have been compared in the presented work.

Keywords voltage controlled oscillator (VCO), leakage power, active power, oscillation frequency, efficiency, cadence tool

1 Introduction

Voltage controlled oscillators (VCOs) are critical and important component in the field of the communication network in electronics. Two traditionally used VCOs are complementary metal oxide semiconductor (CMOS) ring and inductor-capacitor (LC) tank based circuits, which are basic form of oscillators [1,2]. In the LC tank, oscillator on-chip combination of capacitors and inductors create large layout area [3]. On other hand, CMOS ring inverter

oscillators have provided advantage in controlling tuning range and no need for on-chip inductors [4,5]. Due to these reasons, CMOS ring oscillators provide flexibility for on-chip fabrication. CMOS based ring oscillator has become important building blocks in very large scale integration (VLSI) system with widely used in battery operated mobile devices and other communication and data processing systems with low power dissipation [6]. A ring oscillator is combination of many delay stages with feedback element from output to input stage [7]. In the electronic system, different types of ring VCO have been investigated using different types of delay cells like multiple feedback, dual delay paths and single ended delay cells [7]. There are some drawbacks of ring oscillators, like phase noise, power consumption and low oscillation frequency, which are important parameters in VCO [8–10]. Increasing the demand of portable devices including cellular phones, personal communication devices have aggressively improved attention for the low power consumption. Total power dissipation in VLSI circuits is combination of dynamic, static and leakage power. Dynamic power consumption due to switching of capacitance and static power is created by direct path between power supply (V_{dd}) to ground (V_{ss}) [6], minimum leakage power is also important in VLSI technology, it is known as off state power dissipation that arises from substrate injection and sub threshold currents, and the scaling of gate length further increases the leakage power. In the metal oxide semiconductor field effect transistors (MOSFETs) are controlling the bulk terminal of device, which offers enhanced performance parameter in term of power consumption [11], to improve the standby leakage in CMOS circuits a reverse body biasing was normally used. In body biasing techniques, it makes utilization of body terminal as another control mechanism to dynamically tune the threshold voltage [12]. Body bias technique defines the negative channel metal oxide semiconductor (NMOS) body bias, positive channel metal oxide semiconductor (PMOS) body bias, NMOS and PMOS joint body bias

technique with ring oscillator. In NMOS and PMOS reverse body bias technique, all substrate terminals are connected to input supply, which reduce the leakage or wastage of power supply. In presented work, main objective is to reduce sub threshold leakage power consumption in VCO during off-to-on mode transition using reverse bias voltage. In Section 2, 45 nm low leakage ring VCO with three modified structures using reverse body biasing technique has been presented. The performance analysis and simulation results of VCO with reduction technique are presented in Section 3, comparison of presented technique and previous technique are shown in Section 4. Summary of the reported work is provided by Section 5.

2 Circuit description

2.1 Five stage ring VCO

Ring oscillator is cascaded combination of delay stages, connected in a close loop series shown in Fig. 1, the ring oscillators calculated with a chain of delay stages have created great interest because of their numerous useful features [13]. These attractive features are as follows: 1) It can be effortlessly designed with the state-of-art integrated circuit technology (CMOS), bipolar complementary metal oxide semiconductor (BiCMOS); 2) It can accomplish its oscillations at low voltage; 3) It can give high-frequency oscillations with dissipating low power; 4) It can be electrically tuned; 5) It can provide wide tuning range; 6) It can provide multiphase outputs because of their basic structure [14]. Output waveform of ring oscillator is shown in Fig. 2, and Fig. 1 presented schematic diagram of five stage ring oscillator with inverter configuration with capacitor (0.01 pf) and feedback arrangement generates oscillations.

In Fig. 1, P1, P2,....., P5 stand for positive channel metal oxide semiconductors (PMOSs), N1, N2,...., N5 stand for

negative channel metal oxide semiconductors (NMOSs), voltage control (V_{ctrl}) stands for input of ring oscillator, C indicates capacitor and Gnd is ground with the supply voltage $V_{dd} = 0.7$ V.

2.2 Sub circuit of VCO ring oscillator (inverter)

Five stage delay cell VCO ring oscillator consists of five inverters [15]. Inverter is designed by using one NMOS and one PMOS transistor. PMOS transistor works as a pull-up network and NMOS transistor works as a pull-down network. In this combination, PMOS transistor is connected to power supply ($V_{dd} = 0.7$ V) and NMOS transistor is connected to ground ($V_{Gnd} = 0$ V). Inverter schematic is shown in Fig. 3 and its working region is given as.

$$I_D = 0 \text{ (off : } |V_{GS}| < |V_{TH}|). \quad (1)$$

Equation (1) presents the cut off region of inverter, where I_D is drain current, V_{GS} is gate to source voltage and V_{TH} is threshold voltage, the gate source voltage that is less than some critical voltage in this region $V_{out} = 0$ V due to this no power is wasted.

$$I_D = k \left(\frac{W}{L} \right) \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$\text{(triode : } |V_{DS}| \leq |V_{GS}| - |V_{TH}|). \quad (2)$$

Equation (2) is known as saturation region of inverter, where k is constant, W is width, L is length, V_{DS} stands for drain to source voltage.

$$I_D = \left(\frac{k}{2} \right) \left(\frac{W}{L} \right) (V_{GS} - V_{TH})^2 (1 + \lambda_{n,p} V_{DS})$$

$$\text{(saturation : } |V_{DS}| \geq |V_{GS}| - |V_{TH}|). \quad (3)$$

Equation (3) present non saturation region of CMOS inverter, where $\lambda_{n,p}$ stands for channel length modulation

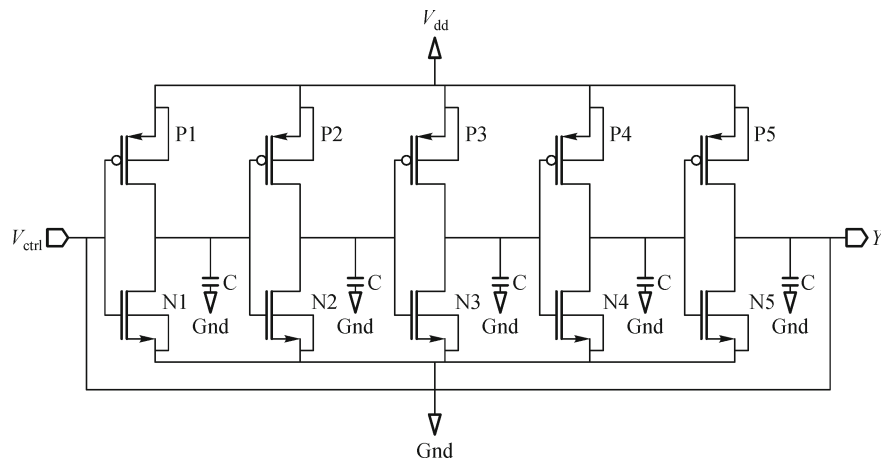


Fig. 1 Five stage VCO ring oscillator

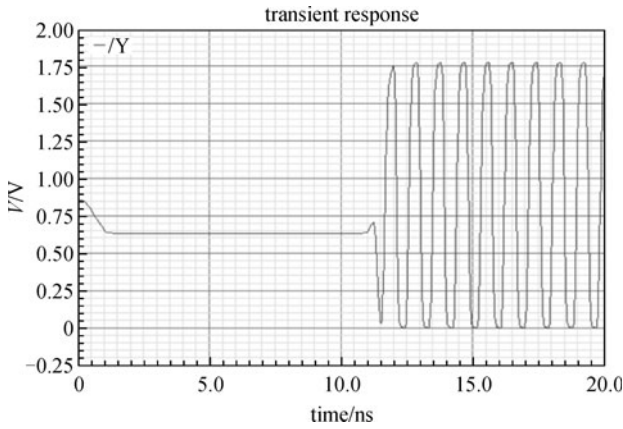


Fig. 2 Waveform of VCO ring oscillator

parameter and drain current mainly depends upon the value of gate to source voltage (V_{GS}) and drain to source voltage (V_{DS}).

We have regional relation as following:

$$\text{NMOS} \begin{cases} V_{\text{out}} > V_{\text{DD}} - V_{\text{Tn}} : \text{off}, \\ V_{\text{in}} \leq V_{\text{DD}} - V_{\text{Tn}} : \text{triode}, \\ V_{\text{in}} \geq V_{\text{DD}} - V_{\text{Tn}} : \text{saturation}, \end{cases} \quad (4)$$

where, V_{in} is input voltage, V_{DD} is drain voltage, and V_{Tn} stands for threshold voltage of NMOS.

$$\text{PMOS} \begin{cases} V_{\text{in}} < -V_{\text{Tp}} : \text{off}, \\ V_{\text{out}} \geq -V_{\text{Tp}} : \text{triode}, \\ V_{\text{out}} \leq -V_{\text{Tp}} : \text{saturation}. \end{cases} \quad (5)$$

In Eq. (5), V_{out} is output voltage and V_{Tp} stands for threshold voltage of PMOS.

Figure 3 shows that voltage control (V_{ctrl}) is input of inverter and Gnd is ground with the supply voltage $V_{\text{dd}} = 0.7 \text{ V}$.

CMOS inverter structure has been used as delay cell in this proposed circuit, inverter circuit has PMOS and NMOS as sub circuits, which is shown in Fig. 3. CMOS ring oscillator has used 0.01pf capacitance at output of each delay stage. Joint PMOS and NMOS reverse body bias, PMOS reverse body bias and NMOS reverse body bias has been presented with low leakage power and high oscillation frequency [12]. In VCO, oscillation frequency has been controlled by bulk terminal of PMOS and NMOS for reduction in the power dissipation. VCO with reverse substrate bias, threshold voltage is increased by Eq. (6), which extremely reduces the sub threshold leakage currents [16,17].

As a result of controlling bulk voltage (V_{sb}) leakage current is reduced and hence power dissipation is minimized.

$$V_t = V_{t0} + \gamma(\sqrt{2\phi_f + V_{\text{sb}}} - \sqrt{2\phi_f}), \quad (6)$$

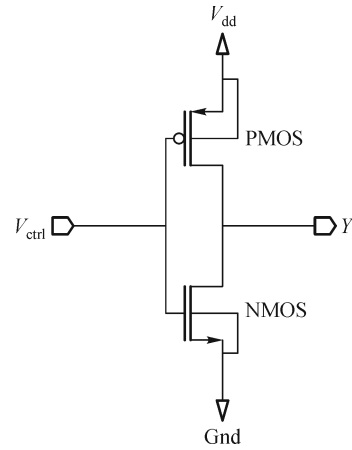


Fig. 3 Inverter schematic diagram using PMOS and NMOS, where V_{ctrl} varies from 0.7 to 1.8 V

where V_{t0} is threshold voltage for $V_{\text{sb}} = 0 \text{ V}$; ϕ_f is Fermi potential and γ is substrate bias coefficient.

2.3 Five stage ring VCO with NMOS reverse body bias technique

Five stage rings VCO using NMOS reverse substrate bias technique is shown in Fig. 4.

In the presented VCO, substrates of PMOS (pull up n/w) have been connected to V_{dd} power supply; and in NMOS transistors, substrates have been connected to V_{ctrl} which is varied from 0.7 to 1.8 V, Supply voltage have been kept constant to $V_{\text{dd}} = 0.7 \text{ V}$.

In Fig. 4, V_{ctrl} is control input voltage, V_{dd} is supply voltage (0.7 V for 45 nm technology), P1, P2, ..., P5 is positive channel metal oxide semiconductor (PMOS), N1, N2, ..., N5 is negative channel metal oxide semiconductor (NMOS).

2.4 Five stage ring VCO with PMOS reverse body bias technique

NMOS substrate bias technique with VCO has provided high leakage and small oscillation frequency in comparison to standard parameters. To overcome this problem, PMOS reverse substrate bias technique has been applied to the five stage ring VCO. In modified design NMOS, substrate terminal bias is connected to ground, and PMOS body terminal is connected to bias control voltage (V_{cbp}), which ranged from 0.7 to 1.8 V and power supply V_{dd} is constant at 0.7 V in Fig. 5. Oscillation frequency and power consumption are obtained for a variety of values of PMOS body bias voltage.

In Fig. 5, P1, P2, ..., P5 is positive channel metal oxide semiconductor (PMOS) with reverse body bias technique, N1, N2, ..., N5 is negative channel metal oxide semiconductor (NMOS), in which substrates have been

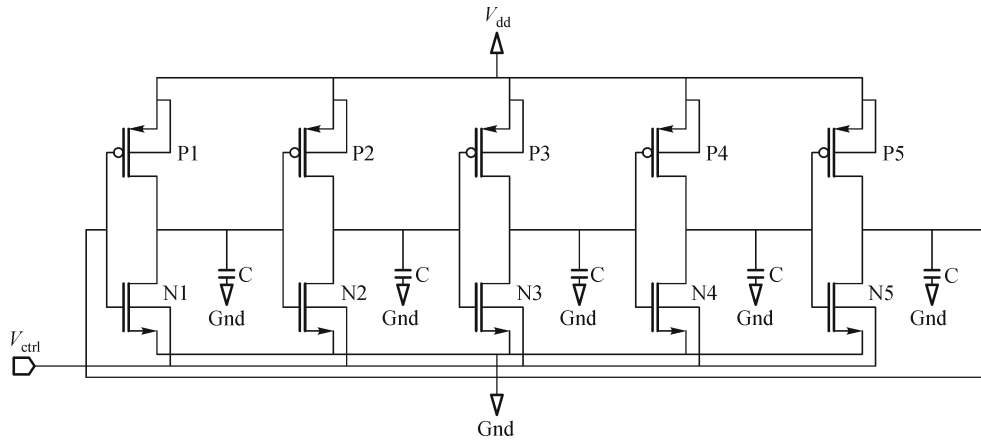


Fig. 4 Ring oscillator schematic diagram using PMOS and NMOS, with NMOS reverse substrate bias, where V_{ctrl} varies from 0.7 to 1.8 V

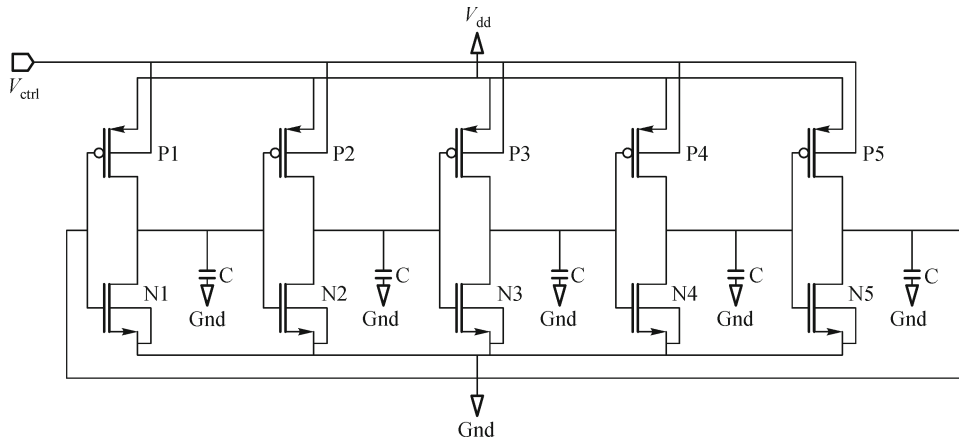


Fig. 5 Ring oscillator schematic diagram using PMOS and NMOS, with PMOS reverse substrate bias, where V_{ctrl} varies from 0.7 to 1.8 V

connected to ground, voltage control (V_{ctrl}) is input of ring oscillator, C indicates capacitor with 0.01 pf rating and Gnd indicates the ground supply and the supply voltage $V_{dd} = 0.7$ V.

2.5 Five stage ring VCO with joint PMOS and NMOS reverse body bias technique

In the third design PMOS substrate bias (V_{cbp}) and NMOS substrate bias (V_{cbn}) have been varied simultaneously. All PMOS and NMOS transistor substrate terminals are connected to reverse bias voltage as shown in Fig. 6, and reverse bias voltage is varying from 0.7 to 1.8 V at room temperature. Supply voltage has been fixed at 0.7 V. Power consumption and output frequency have been controlled by combination of NMOS and PMOS reverse bias voltage with constant power supply. New design of joint reverse body bias is presented in Fig. 6.

In Fig. 6, P1, P2,..., P5 is positive channel metal oxide semiconductor (PMOS), N1,N2,...,N5 is indicate negative channel metal oxide semiconductor (NMOS), and NMOS & PMOS substrates have been connected to reverse body bias voltage, voltage control (V_{ctrl}) is input of ring oscillator varying from 0.7 to 1.8 V, C indicates capacitor and Gnd is ground supply and the supply voltage $V_{dd} = 0.7$ V.

3 Simulation results

The presented work is simulated in cadence virtuoso for 45 nm technology, with the help of result table. In joint PMOS and NMOS reverse body bias technique, we got valuable percentage reduction in parameter (leakage power, active power and oscillation frequency) as compared to PMOS reverse body bias and NMOS reverse body bias technique. The circuit for new design is simulated and

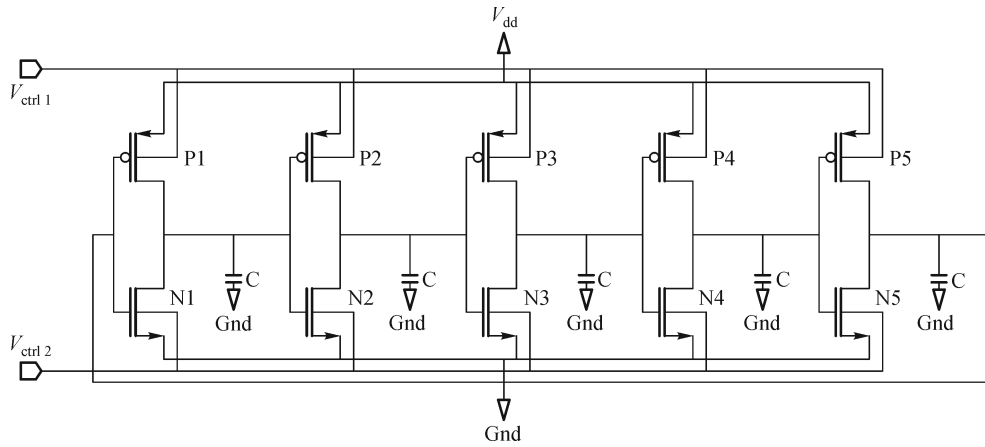


Fig. 6 Ring oscillator schematic diagram using PMOS and NMOS, with joint PMOS and NMOS reverse substrate bias, where V_{ctrl} varies from 0.7 to 1.8 V

analyzed with reverse body bias voltage ranged from 0.7 to 1.8 V and constant supply power at 0.7 V.

3.1 Oscillation frequency

Frequency of oscillation for N stage delay VCO is given by following equation.

$$F_{osc} = \frac{1}{2NT_d}, \tag{7}$$

were N is the number of delay stages and T_d is delay of each stage [13]. Max oscillation frequency of five stage VCO ring oscillator with joint PMOS and NMOS reverse substrate bias technique in 45 nm technology at 0.7 V, where $N = 5$, delay $T_d = 0.21$ ps so the oscillation frequency $F_{osc} = 4.76$ GHz.

Table 1 shows the oscillation frequency of five stage

VCO ring oscillator. Joint reverse substrate bias techniques provide 4.76 GHz oscillation frequency at 0.7 V input supply, which is comparatively better than those of PMOS and NMOS reverse substrate bias technique.

3.2 Active power

Active power dissipation explains during when VCO is on state. Mainly active power is estimated by giving input voltage and current consumption of the device and then calculating the average power dissipation [18]. The simulation time for calculate active power is 200 ns. The active power is combination of dynamic and static power. As shown in Table 2, PMOS and NMOS reverse substrate bias have been compared to joint PMOS and NMOS reverse body bias technique and provided effective reduction in active power (12.03 nW).

Table 1 Oscillation frequency of five stages VCO ring oscillator

voltage/V	oscillation frequency		
	NMOS reverse body bias/MHz	PMOS reverse body bias/MHz	joint PMOS and NMOS reverse body bias/GHz
0.7	3.8	5.33	4.76
1.0	3.3	8.92	4.92
1.2	2.8	11.64	4.73
1.8	1.79	13.01	3.0

Table 2 Active power of ring oscillator with NMOS, PMOS, joint PMOS & NMOS reverse substrate bias techniques

voltage/V	active power		
	NMOS reverse body bias/ μ W	PMOS reverse body bias/ μ W	joint PMOS and NMOS reverse body bias/nW
0.7	5.68	2.68	12.03
1.0	8.4	4.72	16.25
1.2	21.32	19.37	23.15
1.8	31.01	24.78	29.68

3.3 Leakage power

Leakage power is given by off state device, when providing input voltage 0 V. In other words, we can say that leakage power is a wastage charge of any device, which is regularly discharging from the device even the device in off state. Leakage power reduces the ability of the device, so this became the reason of poor performance of device. Leakage power of CMOS device is given by

$$P_{leak} = I_{leak} V_{dd} \tag{8}$$

In the case of joint PMOS and NMOS reverse substrate bias leakage power is (1.23 pW) at 0.7 V supply voltage, which is minimum in comparison to other two design (Table 3).

Leakage power in VCO with NMOS substrate bias

$$= 9.49 \text{ nW.} \tag{9}$$

In Eq. (9), the leakage current in the NMOS substrate bias is $I_{leak} = 1.35 \text{ nA}$, and $V_{dd} = 0.7 \text{ V}$.

Leakage power in VCO with PMOS substrate bias

$$= 6.19 \text{ nW.} \tag{10}$$

In Eq. (10), the leakage current in the PMOS substrate bias is $I_{leak} = 8.84 \text{ nA}$, with supply $V_{dd} = 0.7 \text{ V}$.

This type of oscillator mainly used in form of fiber optical parametric oscillators (FOPO).

3.4 Smith chart

The Smith chart can be used for simultaneously expressing multiple performance parameters, such as counting admittances, impedances and reflection coefficients. These are often called Y, Z, Y-Z, Smith charts. In ring VCO, Y, Z, Smith chart are given as follows (see Figs. 7 and 8).

The admittance will be written as

$$Y_L = \frac{1}{Z_L} = C + iS, \tag{11}$$

Table 3 Leakage power of ring oscillator with NMOS, PMOS joint PMOS and NMOS reverse subtract bias techniques

volatge/V	leakage power		
	NMOS reverse body bias/nW	PMOS reverse body bias/nW	joint PMOS and NMOS reverse body bias/pW
0.7	9.49	6.19	1.23
1.0	11.84	8.24	1.88
1.2	15.53	10.13	2.94
1.8	24.22	14.22	3.59

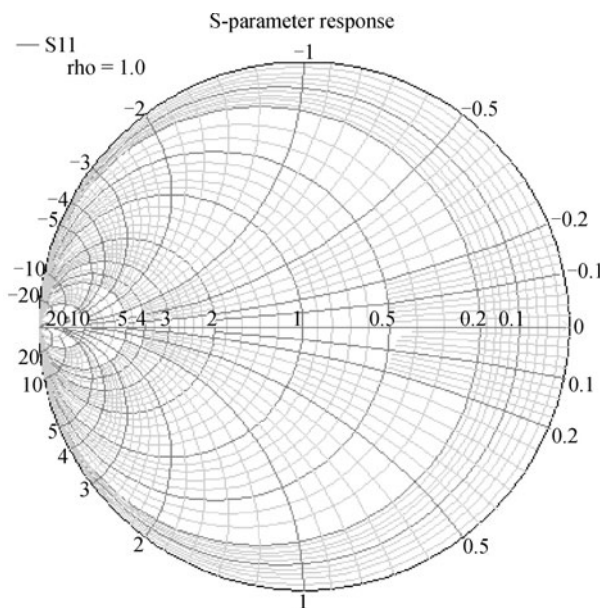


Fig. 7 Y parameter of Smith chart

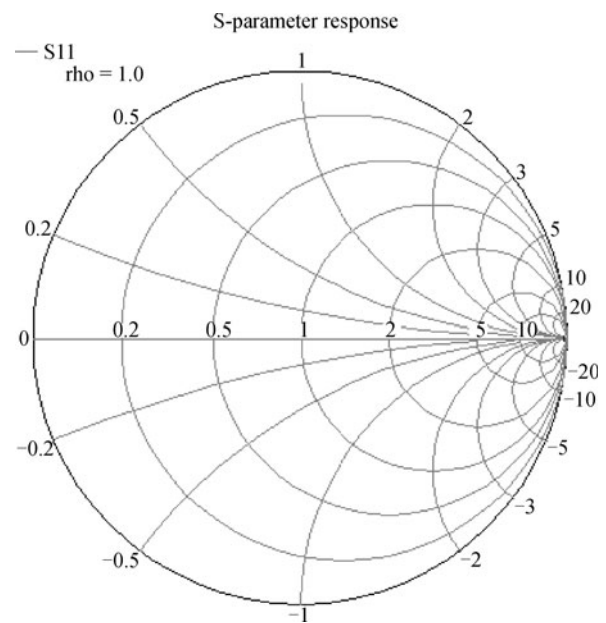


Fig. 8 Z parameter of Smith chart

Y_L is admittance of load, which is the inverse of impedance of load Z_L , real part of Y_L is written as C , and is known as the conductance, the imaginary part of Y_L is written as S and is known as susceptance.

3.5 Efficiency

Efficiency is provided the capacity of any device. The perfect efficiency means, fewer drain power and the input supply, and allowing small lighter power supplies and structure enclosures. Efficiency is calculated by Eq. (12) as below.

$$\text{Efficiency} = (\text{output value}/\text{input value}) * 100. \quad (12)$$

By Eq. (12), we have calculated the efficiency of joint PMOS and NMOS reverse body bias voltage controlled oscillator with supply voltage $V_{dd} = 0.7$ V.

Figure 9 shows that the max efficiency of five stage ring VCO is 76.84% at $V_{dd} = 0.7$ V and input supply $V_{ctrl} = 0.7$ V. Efficiency provide the input/output ratio of device, high efficiency provide high significant uses of circuit.

4 Discussion

Presented work in this paper has been compared to previously published paper (Ref. [18]) with simulation program with integrated circuit emphasis (SPICE) based on Taiwan semiconductor manufacturing company (TSMC) with $0.18 \mu\text{m}$ ($V_{dd} = 1.8$ V) CMOS technology (Table 4). Power consumption of reverse substrate bias is in mile watt (mW) and maximum oscillation frequency is

0.8 GHz in joint reverse body bias technique with input control voltage varies from 0 to 1.5 V; on the other hand, in the presented work, applied supply voltage is $V_{dd} = 0.7$ V in nano meter technology (nm), in which input voltage varies from 0.7 to 1.8 V and minimum active power, leakage power and maximum oscillation frequency are 12.03 nW, 1.23 pW and 4.76 GHz respectively in joint PMOS & NMOS reverse body bias technique, which are excellent in comparison to previous work.

5 Conclusions

In this reported work, low power leakage VCO cell is proposed for low power application with high oscillation frequency. Minimum power consumption has been provided by reverse substrate bias technique in five stage ring VCO. By controlling the body terminal provide alternative method to control the oscillation frequency with significant power dissipation. NMOS reverse substrate bias technique has been used to provide the total leakage power (9.49 nW), active power (5.68 μW) and oscillation frequency (3.8 MHz), PMOS reverse body bias technique has been given oscillation frequency (5.33 MHz), minimum total leakage power (6.19 nW) and active power (2.68 μW), joint PMOS and NMOS reverse substrate has been provided active power consumption (12.03 nW), total leakage power (1.23 pW) and oscillation frequency (4.76 GHz), which is better in comparison to PMOS and NMOS reverse body bias technique. Power saving can be gained by applying reverse biasing with fixed supply voltage ($V_{dd} = 0.7$ V), for those applications in which restricted frequency variation is preferred.

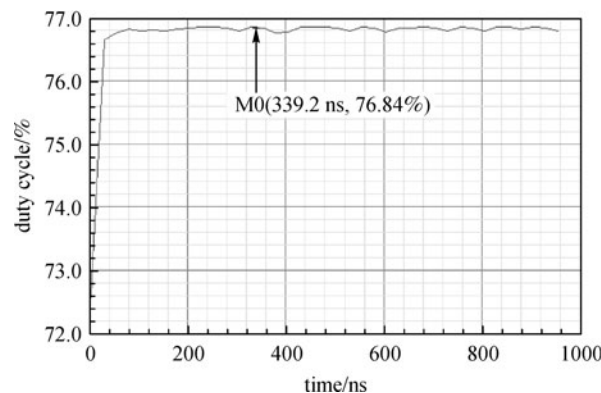


Fig. 9 Efficiency of Voltage controlled oscillator with joint reverse substrate bias

Table 4 Comparison of joint PMOS and NMOS reverse body bias between previous published paper and presented paper

joint PMOS and NMOS reverse body bias/GHz	technology	supply (V_{dd})	power consumption	oscillation frequency/GHz
previous paper	micro meter (μm)	1.8 V	mile watt (mW)	4.76
presented paper	nano meter (nm)	0.7 V	nano watt (nW)	0.8

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