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RESEARCH ARTICLE

Ground bounce noise reduction aware combinational multi threshold CMOS circuits for nanoscale CMOS multiplier

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Abstract Multi-threshold complementary metal-oxide-semiconductor (MTCMOS) is often used to reduce the leakage current in idle circuit. Ground bounce noise produced during a transition mode (sleep-to-active) is an important challenge in MTCMOS. In this paper, various noise-aware combinational MTCMOS circuit was used to evaluate the ground bounce noise. An intermediate mode was applied in the sleep-to-active mode transition to reduce the charge stored on virtual lines to real ground. The dependence of ground bounce noise on voltage, transistor size and temperature was investigated with different MTCMOS circuit technique. The peak amplitude of ground bounce noise was reduced up to 78.82%. The leakage current of the circuit was decreased up to 99.73% and the active power of the circuit was reduced up to 62.32%. Simulation of multiplier with different MTCMOS circuit techniques was performed on 45 nm CMOS technology.

Keywords multi-threshold complementary metal-oxide-semiconductor (MTCMOS), mode transition, ground bounce noise, sleep transistor

1 Introduction

In today's semiconductor device industries, it has been challenged to develop high performance portable systems with reliability in data transmission. Metal-oxide-semiconductor field-effect transistor (MOSFET) scaling deep into sub-100 nm regime leads to shrink operating voltage, and causes larger leakage current and ground bounce noise [1]. In resent year, leakage current and ground bounce noise have been considered as critical design parameters in wireless communication systems [2,3].

Multi-threshold complementary metal-oxide-semiconductor (MTCMOS) is commonly used technique for leakage current suppression [4,5]. In MTCMOS circuit, high threshold voltage (high-V_{TH}) sleep transistors are used at header and footer of the circuit. It is used to cutoff the power supply and ground connection of the idle low threshold voltage (low-V_{TH}) circuit blocks [6]. These sleep transistors are either high-V_{TH} p-type metal-oxide-semiconductor (pMOS) transistor or a high-V_{TH} n-type metal-oxide-semiconductor (nMOS) transistor. A high-V_{TH} pMOS sleep transistor is attached between a real power line (power supply) and a virtual power line (low-V_{TH} circuit blocks), as shown in Fig. 1. Alternatively, a high-V_{TH} nMOS sleep transistor is connected between actual ground and virtual ground (low-V_{TH} circuit blocks). These sleep transistors at header and footer are turned off to reduce the sub-threshold leakage current in idle circuits.

When the circuit is transited from sleep-to-active mode, ground bounce noise is occurring due to the large voltage fluctuation on both real power line and real ground line, as shown in Fig. 1. In this paper, ground bounce noise in MTCMOS circuit with multiplier is evaluated. Multipliers are the fundamental and essential building blocks of very-large-scale-integration (VLSI) systems, microprocessor (μP), digital signal processing (DSP), etc. The profile growth in semiconductor device industry has led to the development of high performance portable systems with low power modules [7]. Multiplier has three input sequences: parallel, serial and hybrid (parallel-serial) approach. Parallel approach multiplier has higher speed and better performance [8,9]. The operation of parallel multiplier can be divided into two parts: 1) formation of the partial products, and 2) summation of these partial products to form final products, as shown in Fig. 2.

The multiplier is a complex adder array structure. The performance and characteristics of multiplier depend on the algorithm, in which they are operated [7]. Bit array multiplier has regular and simple structure. Figure 3 shows

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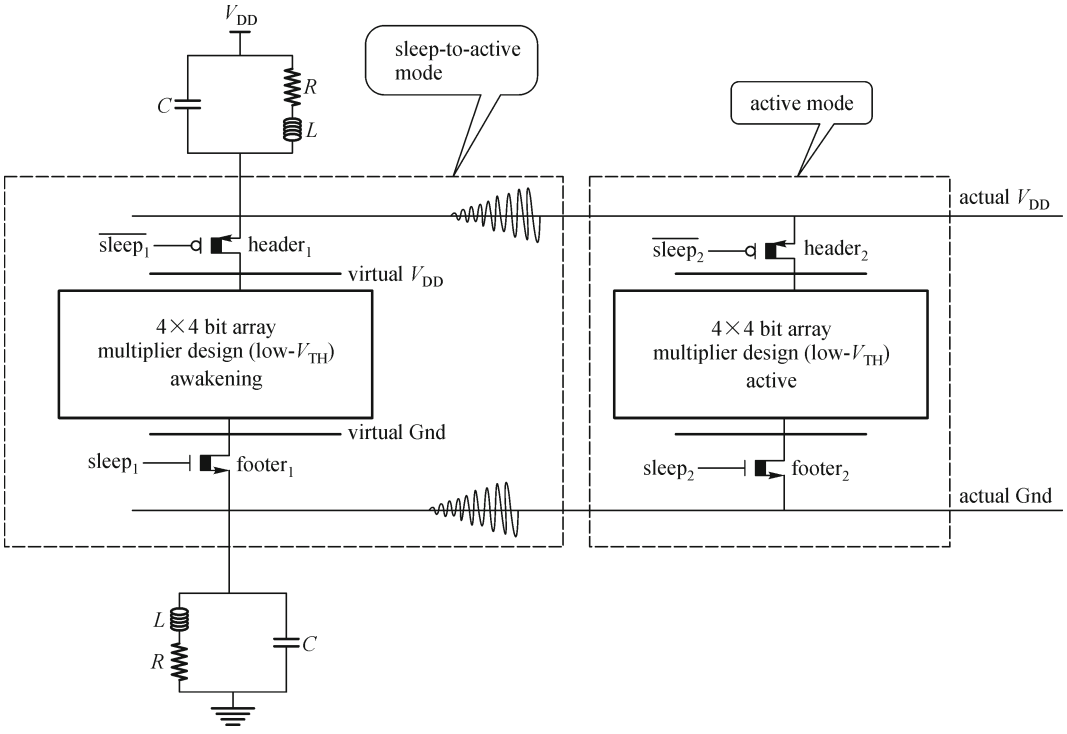

Fig. 1 Power and ground bounce noise generated in conventional MTCMOS technique on multiplier circuit

$$
\begin{array}{cccccccc}
 & & & X_3 & X_2 & X_1 & X_0 & \\
 & & \times & Y_3 & Y_2 & Y_1 & Y_0 & \\
\hline
 & & & X_3Y_0 & X_2Y_0 & X_1Y_0 & X_0Y_0 & \\
 & & X_3Y_1 & X_2Y_1 & X_1Y_1 & X_0Y_1 & & \\
 & X_3Y_2 & X_2Y_2 & X_1Y_2 & X_0Y_2 & & & \\
+ & X_3Y_3 & X_2Y_3 & X_1Y_3 & X_0Y_3 & & & \\
\hline
P_7 & P_6 & P_5 & P_4 & P_3 & P_2 & P_1 & P_0
\end{array}
$$

Fig. 2 Basic operation of multiplier

block diagram of 4 × 4 bit-array multiplier. The partial product is generated by multiplying, multiplicand and multiplier bits [8]. The partial products are shifted to their bit orders and then added by adders. If there are N numbers of partial products in multiplier, then $(N-1)$ bit adders are required. The paper is organized as follows: different noise aware MTCMOS techniques introduced in Section 2; simulation and results are explained in Section 3; this paper is concluded in Section 4.

2 Noise aware MTCMOS techniques

In this section, different noise-aware MTCMOS techniques are presented. Tri-mode MTCMOS circuit techniques are presented in Section 2.1. Dual-switch MTCMOS technique is shown in Section 2.2. Tri-transistor-controlled MTCMOS circuit technique is introduced in Section 2.3.

2.1 Tri-mode MTCMOS technique

In this section, we designed our circuit with tri-mode MTCMOS technique [10]. An additional intermediate park (wait) mode is introduced between mode transitions (sleep-to-active). A high-V_{TH} pMOS transistor is attached in parallel with high-V_{TH} nMOS transistor in the footer of the circuit, as shown in Fig. 4.

In standby mode, both N_1 and park transistor are turned off to reduce the sub-threshold leakage current. In sleep mode, the voltage at virtual ground (GND/V_{Gnd1}) is maintained at ~V_{DD} (supply voltage). The mode transitions are divided into two parts, such as sleep-to-park mode and park-to-active mode transition. In sleep-to-park mode transition, the park transistor is turned on while N_1 is maintaining cutoff. The virtual ground line voltage is discharged through the P1 transistor [parker (V_{TP})]. The ground bounce noise is suppressed due to lower voltage swings on the virtual ground in park mode transition, as shown in Fig. 4. In park-to-active mode transition, the footer transistor N_1 is turned on and the park transistor is turned off. In active mode, the virtual ground voltage discharges up to ~V_{DD}.

2.2 Dual-switch MTCMOS technique

In this section, we designed a circuit with dual-switch

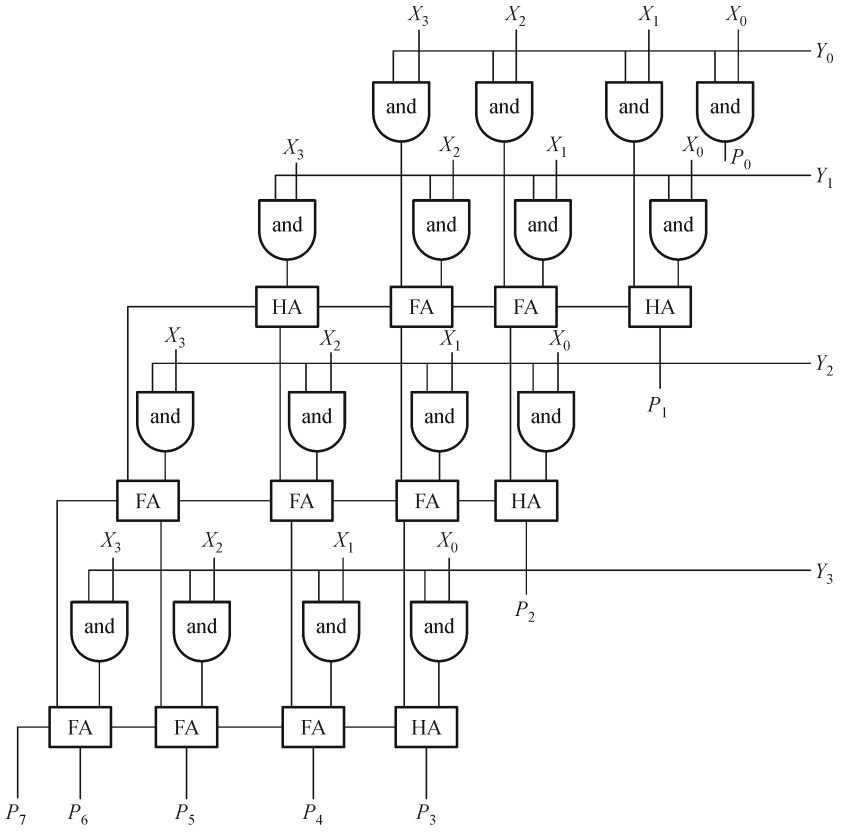

Fig. 3 Design of 4 × 4 bit-array multiplier (HA = half adder, FA = full adder)

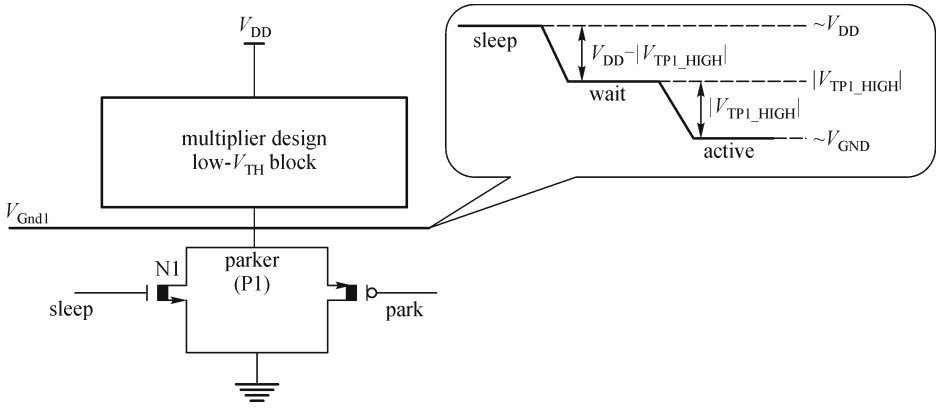

Fig. 4 Tri-mode MTCMOS technique [10]

MTCMOS technique [10,11]. A high-V_{TH} nMOS transistor (N_2) is connected parallel to header sleep transistor (P_1) between virtual V_{DD} and real V_{DD}. Similarly, a high-V_{TH} pMOS transistor (P_2) is connected parallel to footer sleep transistor (N_1) between virtual ground and real ground line, as shown in Fig. 5. An intermediate hold mode is introduced with the help of extra transistors.

In sleep mode, transistors P_1, N_1, P_2 and N_2 are turned off to reduce the sub-threshold leakage current. The voltages at virtual power (V_{DD}) and virtual GND are approximately equalized (V_{MID}). In first transition (sleep-to-hold) mode, transistors P_2 and N_2 are turned on, and transistors P_1 and N_1 are turned off. A differential voltage of $V_{DD}-V_{MIN}-V_{TN}$ is produced at virtual V_{DD}, and $V_{MIN}-V_{TP}$ is produced at virtual GND. In second transition (hold-to-active) mode, transistors P_1 and N_1 are later activated. In active mode, the virtual power line is discharging up to $\sim V_{DD}$ and virtual ground line is discharging up to $\sim V_{GND}$. The ground bounce noise is alleviated by reducing voltage fluctuation on virtual lines during transition from sleep mode to active mode through hold mode, as shown in Fig. 5.

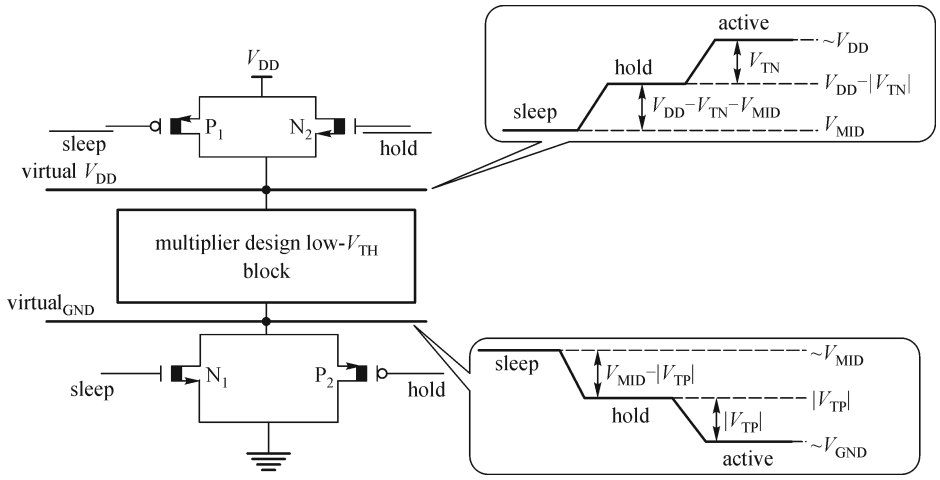

Fig. 5 Dual-switch MTCMOS technique [11]. High-V_{TH} sleep transistors are represented by thick channel length. $0\ V < V_{MIN} < V_{DD}$

2.3 Tri-transistor-controlled MTCMOS technique

In this section, we designed our circuit with tri-transistor-controlled MTCMOS technique [12] to suppress the ground bounce noise in sleep-to-active mode transition. A high-V_{TH} pMOS transistor is connected parallel to footer for introducing a doze mode in MTCMOS circuit, as shown in Fig. 6(a).

In sleep mode, the sleep transistors (header and footer) and doze transistor are turned off to reduce the sub-

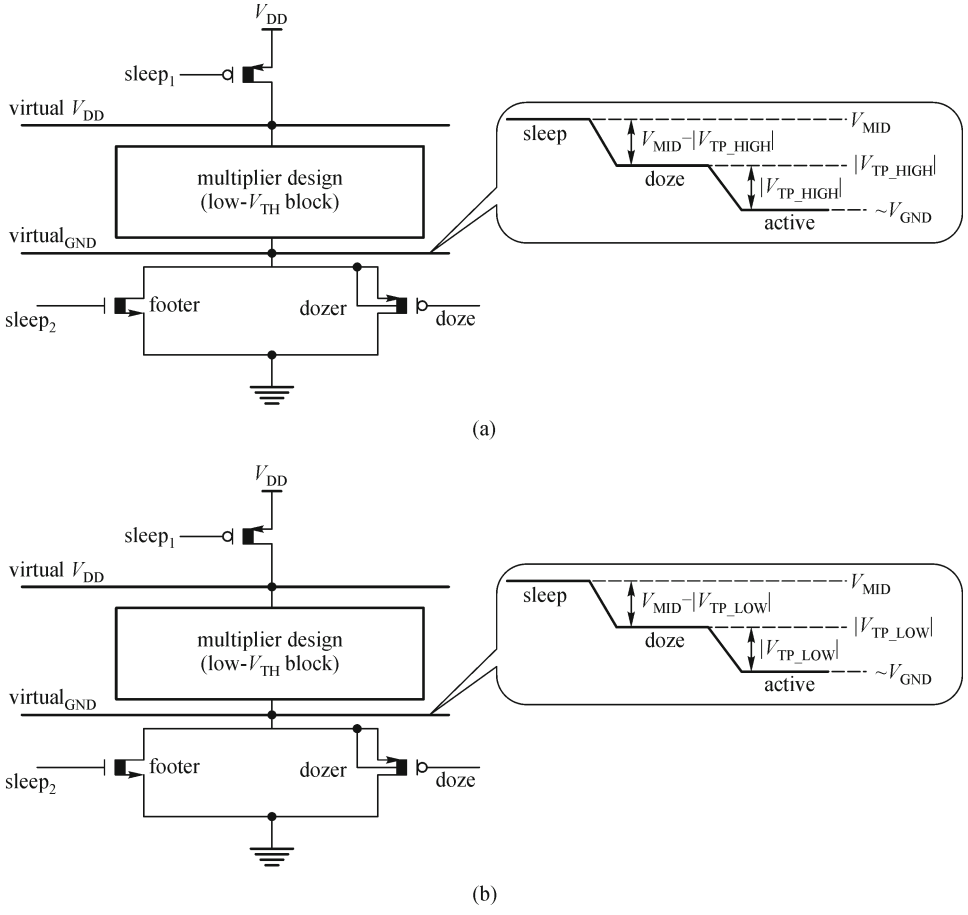

Fig. 6 Tri-transistor-controlled MTCMOS circuit. (a) TTH; (b) TTL [12]. High-V_{TH} sleep transistors are represented by thick channel length. $0\ V < V_{MIN} < V_{DD}$

threshold leakage current. In sleep mode, the virtual GND voltage is $\sim V_{MIN}$. The sleep-to-active mode transition is divided into sleep-to-doze mode and doze-to-active mode. In sleep-to-doze mode, the header and doze transistors are turned on and footer transistor is turned off. The virtual GND voltage is discharged up-to the threshold voltage of doze transistor (V_{TP}). In doze-to-active mode transition, the header and footer transistors are turned on and doze transistor is turned off. The virtual GND voltage is discharged from V_{TP} to $\sim V_{GND}$. By reducing the voltage fluctuation, on virtual GND, we reduced the ground bounce noise in each mode transition with two-step wake-up process. To reduce transition delay from sleep-to-doze mode, a low-V_{TH} doze transistor is used, as shown in Fig. 6 (b). Tri-transistor-controlled MTCMOS technique (high-V_{TH} doze transistor (TTH) and low-V_{TH} doze transistor (TTL)) is evaluated in this section.

3 Simulation and results

In this section, we simulated our low power multiplier with following techniques: tri-mode MTCMOS [10], dual-switch MTCMOS [11] and tri-transistor-controlled MTCMOS [12]. In this paper, we characterized on ground bounce noise, leakage current and active power consumption.

3.1 Ground bounce noise

In this section, we analyzed ground bounce noise on transistor sizes, temperature and voltage scaling for different MTCMOS techniques. The commonly used 40-pin dual-in-line package (DIP-40) model is used to calculate the ground bounce noise for different MTCMOS circuit techniques [13,14]. The basic model of DIP-40 model is shown in Fig. 7.

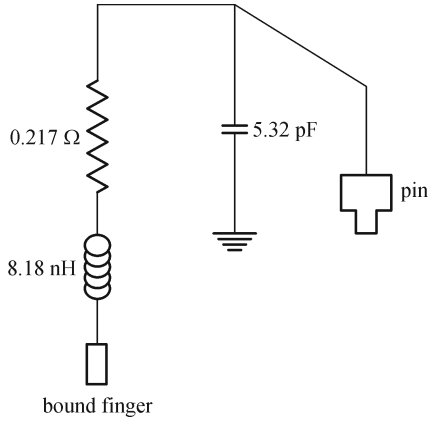

Fig. 7 DIP-40 package pin ground bounce noise model

3.1.1 Effect of voltage scaling on ground bounce noise

In this section, the dependence of ground bounce noise on the voltage was evaluated. The peak of ground bounce noise with tri-mode, dual-switch and tri-transistor-controlled (TTH and TTL) circuit for various voltages is shown in Table 1.

As shown in Fig. 8, tri-mode, dual-switch and tri-transistor-controlled (TTH and TTL) circuits reduce the ground bounce noise by 68%, 78.74%, 78.82% and 78.94% respectively compared to conventional circuit.

The intensity of ground bounce noise is dependent on the rate of change of the instantaneous current (dI/dt) conducted by sleep transistor during sleep-to-active mode transition [15]. The peak amplitude of ground bounce noise is directly proportional to supply voltage. If we increase the supply voltage of circuit, ground bounce noise will also increase. When higher supply voltage is applied, then voltage fluctuation on virtual line increases and the ground bounce noise also increases. Figure 9 shows the effect of ground bounce noise with different circuit techniques on multiplier. In Fig. 9(a), it is clear that the ground bounce noise is produced by the voltage fluctuation. Due to voltage fluctuation, the peak amplitude of ground bounce noise is varies every time. When the ground bounce noise reduction technique are used, the voltage fluctuation at virtual ground is reduced which reduced the peak amplitude of ground bounce noise, as shown in Figs. 9(b), 9(c), 9(d) and 9(e).

3.1.2 Effect of transistor size on ground bounce noise

The ground bounce noises with different size of the controlling transistor (park for tri-mode, dual-switch for dual-switch circuits and dozer for tri-transistor-controlled (TTH and TTL) circuits) were evaluated in this section. The different sizes of transistor are determining the charging and discharging speed during the transition from sleep-to-intermediate mode (park, hold and doze). The effect of dozer size on ground bounce noise was evaluated. The waveform of virtual ground line voltage and real ground line voltage is shown in Figs. 10 and 11, respectively.

When the size of dozer is small, the virtual GND line voltages discharge slowly during sleep-to-doze mode transition. Hence, it reduces the rate of change of the instantaneous current. In steady-state doze mode, virtual ground line voltage is higher with a smaller dozer, the voltage fluctuation on virtual ground line in sleep-to-doze mode is narrower. At higher steady-state doze mode, virtual ground line voltage has higher fluctuation at virtual ground line during doze-to-active mode transition. The relaxation time for the different circuit techniques are shown in Table 2.

When the dozer size is larger, the virtual ground line

Table 1 Effect of voltage scaling on ground bounce noise (unit: mV)

	voltage								
	0.7 V			0.9 V			1 V		
transistor size/nm	2.67	10	15	2.67	10	15	2.67	10	15
conventional		2.149			4.156			3.511	
tri-mode	0.122	0.125	0.127	1.299	1.3	1.286	2.616	2.593	2.51
dual switch	0.117	0.115	0.115	0.883	0.876	0.890	1.628	1.62	1.603
TTH	0.115	0.113	0.112	0.879	0.892	0.895	1.629	1.614	1.624
TTL	0.112	0.111	0.110	0.874	0.905	0.901	1.625	1.617	1.614

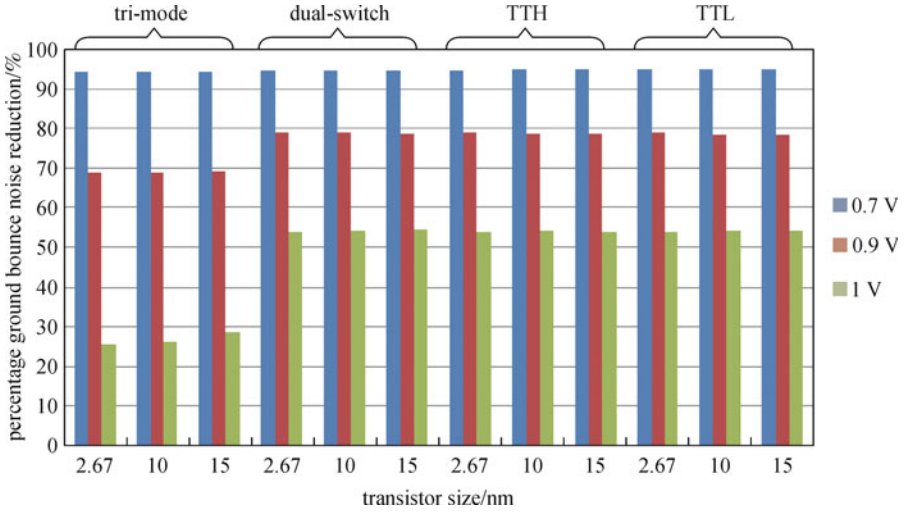

Fig. 8 Percentage ground bounces noise reduction provided by different MTCMOS circuit techniques as compared to conventional circuit

voltages discharge faster during sleep-to-doze mode transition. In steady-state doze mode, the voltage fluctuation at virtual ground line is increased. Alternatively, during doze-to-active mode transition, the voltage fluctuation on virtual ground line is reduced with larger dozer, as shown in Fig. 10.

As shown in Table 3, if we increase the size of the controlling transistor, then it affects the ground bounce noise of the circuit. Tri-mode, dual-switch and tri-transistor-controlled (TTH and TTL) MTCMOS circuit reduced the ground bounce noise by 68.74%, 78.75%, 78.84% and 78.97% respectively compared to conventional circuits.

3.1.3 Effect of temperature on ground bounce noise

In this section, the dependence of ground bounce noise on temperature was studied. The peak of ground bounce noise with tri-mode, dual-switch and tri-transistor-controlled (TTH and TTL) circuit for 27°C, 70°C and 110°C are shown in Fig. 12.

At higher temperature, the saturation current of sleep transistor is decreased because of reduction in carrier mobility [16]. A smaller size sleep transistor current trends to lower the peak amplitude of the ground bounce noise when these sleep transistors are activated. However, the virtual ground line voltage is changed with the voltage fluctuation. The effective resistance of the parker and dozer are increased with higher temperature. In the steady-state intermediate mode, virtual ground line voltage is increased with higher temperature. The range of virtual ground line voltage increased during the transition from intermediate-to-active mode. Therefore, there are tends that the peak ground bounce noise of tri-mode, dual-switch and tri-transistor-controlled circuit increases with higher temperature.

The increased in steady-state virtual ground line voltage and the reduction in saturation current of sleep transistor have opposite effect on peak ground bounce noise with higher temperature. The variation of ground bounce noise on temperature with transistor size is shown in Fig. 12. Due to opposite effect of steady-state virtual ground line voltage and saturation current, the ground bounce noise is weaker dependence on temperature. The tri–mode, dual-

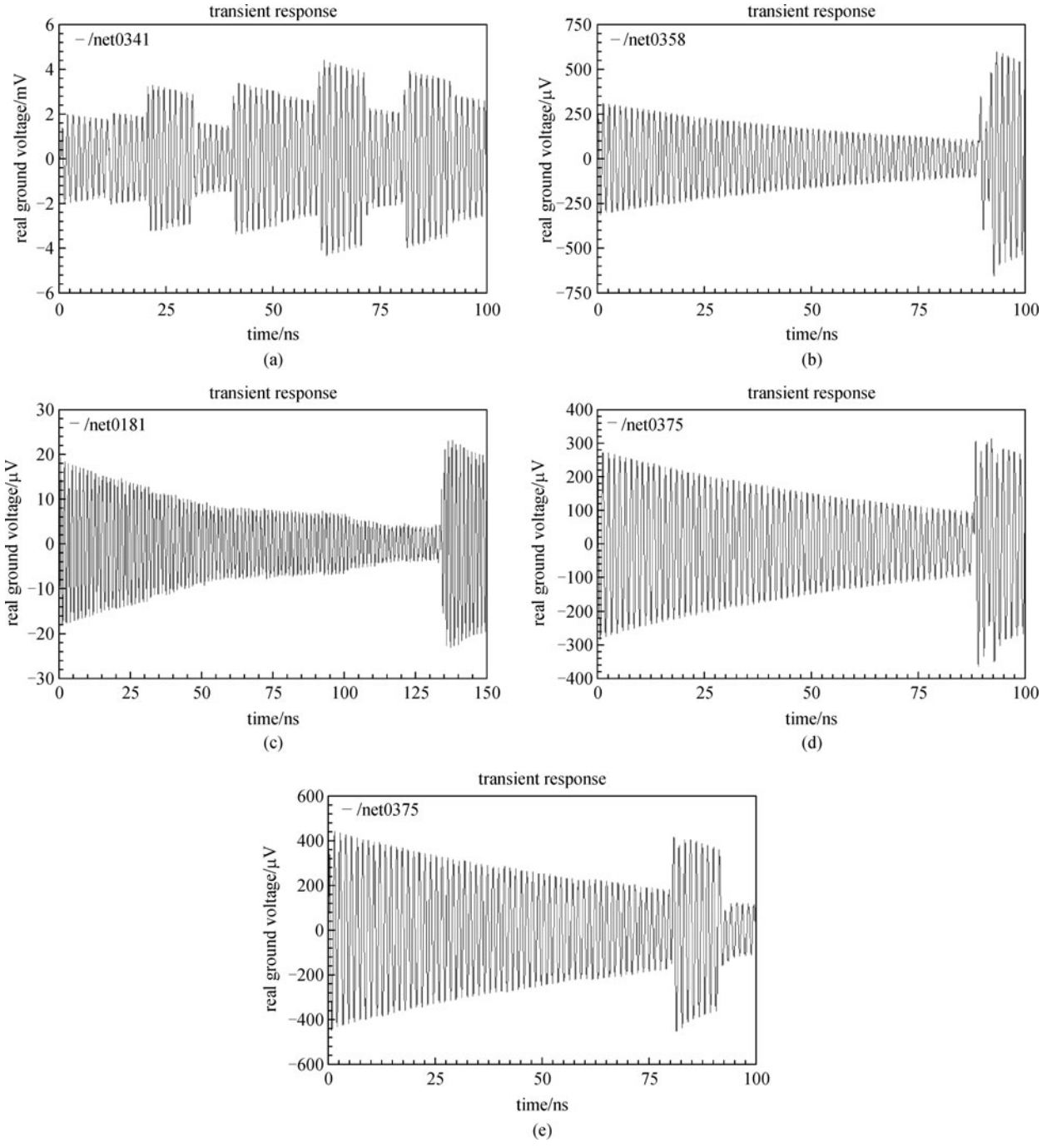

Fig. 9 Waveform showing ground bounce noise at real ground (0.9 V and W/L = 2.67 nm). (a) Conventional design; (b) tri-mode design; (c) dual-switch design; (d) TTH; (e) TTL

switch and tri–transistor–controlled (TTH and TTL) circuit reduced the ground bounce noise by 41%, 59.93%, 60.09% and 60.32% respectively compared to conventional circuit.

3.2 Leakage current

The leakage current of multiplier with tri-mode, dual-switch and tri-transistor-controlled (TTH and TTL) techniques was evaluated in this section. The size of parker in tri-mode, dozer in tri-transistor-controlled and dual–switch in dual–switch circuits is minimum (W/L = 2.67 nm). The leakage current of different circuits are shown in Table 4. The sub-threshold leakage current is produced by high-V_{TH} sleep transistors in MTCMOS circuit. The gate tunneling currents are primary leakage, produced by low-V_{TH} transistors of logic block. The basic equation of leakage current is shown in Eq. (1) [17].

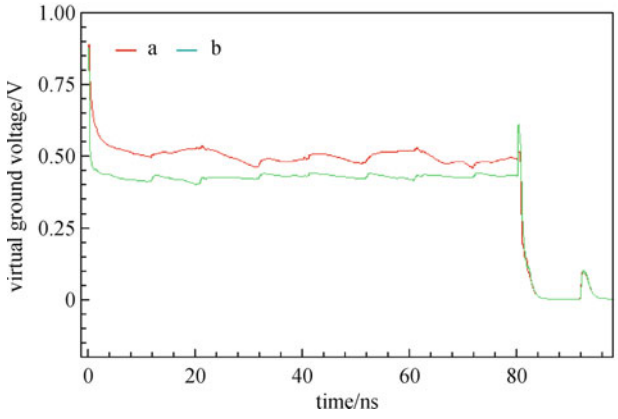

Fig. 10 Waveform of virtual ground line voltage of TTH circuit during transitions from sleep-to-active mode through doze mode. The duration of doze mode is 87.41 ns. (a) Virtual ground line voltage with small doze ($dozer_{small}$ = 2.67 nm); (b) virtual ground line voltage with larger doze ($dozer_{large}$ = 15 nm)

$$I_{leakage} = I_{sub} + I_{ox}, \tag{1}$$

where I_{sub} = sub-threshold leakage current, I_{ox} = gate-oxide leakage current.

$$I_{sub} = K_1 W e^{\frac{-V_{TH}}{nV_\theta}} \left(1 - e^{\frac{-V}{V_\theta}}\right), \tag{2}$$

where K_1 = transconductance parameter ($k = \mu C_{ox}$), W = gate width, V_{TH} = threshold voltage, n = slope shape factor, V_θ = thermal voltage.

$$I_{ox} = K_2 W \left(\frac{V}{T_{ox}}\right)^2 e^{\frac{-\alpha T_{ox}}{V}}, \tag{3}$$

where K_2 = transconductance parameter ($k = \mu C_{ox}$), α = experimentally derived factor, T_{ox} = oxide thickness.

The noise aware MTCMOS techniques provided maximum reduction of leakage current in sleep mode, as shown in Fig. 13. Tri-mode, dual-switch and tri-transistor-controlled (TTH and TTL) circuit reduce the leakage current by 99.72%, 99.73%, 99.74% and 99.7% respectively, as compared to conventional circuit at 25°C. The dependence of sub-threshold leakage current on temperature is stronger than the gate leakage current [13]. At 110°C, the sub-threshold leakage current of a circuit is major power consumption in sleep mode. Tri-mode, dual-switch and tri-transistor-controlled (TTH and TTL) are reduced leakage current by 99.62%, 99.65%, 99.66% and 99.6% respectively, as compared to conventional circuit.

3.3 Active power

The active power of multiplier with tri-mode, dual–switch and tri–controlled–transistor (TTH and TTL) circuit techniques was evaluated in this section. The active power consumption of different circuits is shown in Table 5, at room temperature (27°C).

Table 2 Relaxation time for different circuits (unit: ns)

	transistor size			
	2.67 nm	10 nm	15 nm	20 nm
tri–mode	88.56	20.51	52.45	64.57
dual–switch	133.82	37.53	28.47	27.68
TTH	87.41	22.98	25.32	39.45
TTL	79.66	25.67	30.74	38.46

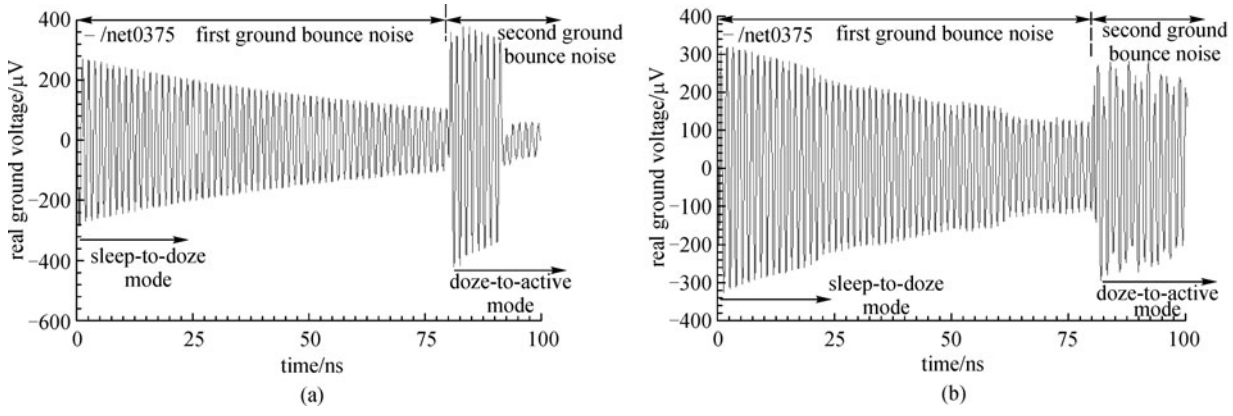

Fig. 11 Waveform of real ground voltage of TTH circuit during transitions from the sleep-to-active mode through doze mode. The duration of doze mode is 87.41 ns. (a) Ground bounce noise on real ground with smaller doze ($dozer_{smaller}$ = 2.67 nm); (b) ground bounce noise on real ground with larger doze ($dozer_{large}$ = 15 nm)

Table 3 Effect of transistor size on ground bounce noise (unit: mV)

	transistor size			
	2.67 nm	10 nm	15 nm	20 nm
conventional	4.156			
tri-mode	1.299	1.3	1.286	1.265
dual-switch	0.883	0.876	0.890	0.883
TTH	0.879	0.892	0.895	0.893
TTL	0.874	0.905	0.901	0.899

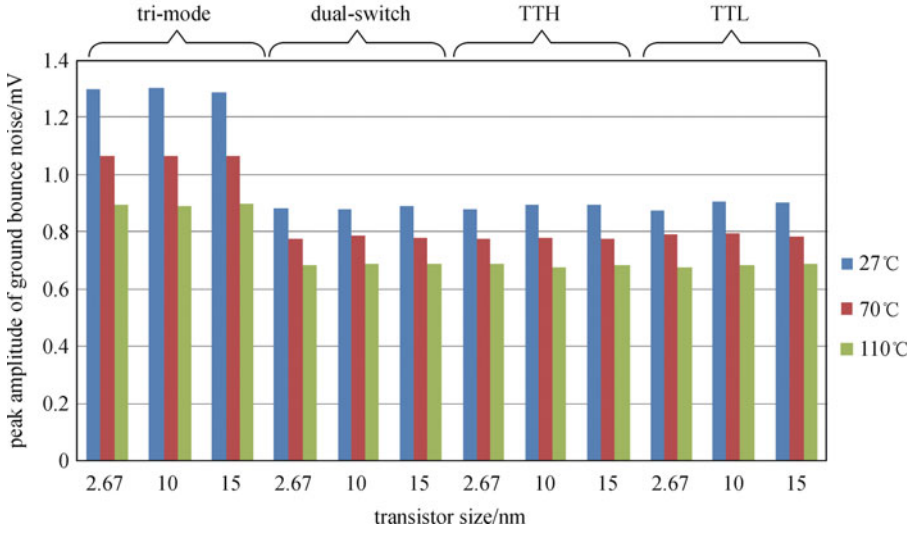

Fig. 12 Peak amplitude of ground bounces noise for tri-mode, dual-switch, TTH and TTL at different temperatures

Table 4 Leakage current consumption (unit: nA)

	temperature					
	27°C			110°C		
voltage/V	0.7	0.9	1	0.7	0.9	1
conventional	4761	18250	27747	4284	14116	21475
tri-mode	27.86	48.42	89.07	27.43	53.33	92.46
dual-switch	43.73	47.97	49.72	42.72	47.35	49.71
TTH	43.94	48.15	50.19	43.14	47.81	50.03
TTL	48.96	53.15	55.32	50.92	56.31	58.81

The dynamic switching power consumption of CMOS circuit is [18]

$$P = C_{\mathrm{L}} V_{\mathrm{DD}}^2 f, \tag{4}$$

where C_{L} is load capacitance, V_{DD} is supply voltage, and f is operating frequency.

Due to resistive voltage drop across the parker, dozer and dual-switch transistors, the effective supply voltage is lower in MTCMOS multiplier as compared to conventional multiplier. The active power consumed by the circuits is explained in Table 5. It is clear from table that, tri-mode, dual-switch and tri-transistor-controlled (TTH and TTL) technique reduced active power by 62.32%, 44.06%, 43.44% and 43.73% respectively, as compared to conventional circuit.

4 Conclusions

In this paper, ground bounce noise was investigated for

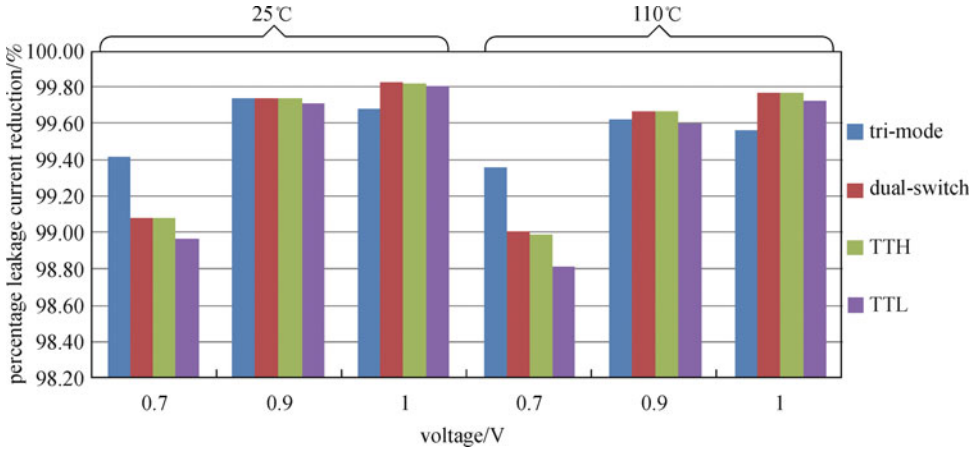

Fig. 13 Percentage leakage current reduction provided by different MTCMOS circuit techniques as compared to conventional circuit (sleep mode)

Table 5 Active power consumption (unit: mW)

	transistor size		
	2.67 nm	10 nm	15 nm
conventional		74.03	
tri-mode	27.89	27.93	27.94
dual-switch	41.41	41.84	41.67
TTH	41.87	41.77	41.87
TTL	41.65	41.83	41.95

Table 6 Performance comparison of different MTCMOS circuits

primary design metric		best technique	worst technique
ground bounce noise	voltage scaling	TTL	tri-mode
	transistor size	dual-switch	tri-mode
	temperature	TTL	tri-mode
leakage current	27°C, 0.7 V	tri-mode	TTL
	27°C, 0.9 V or 1 V	dual-switch	tri-mode
active power consumption		tri-mode	TTL

standard MTCMOS circuit. Different MTCMOS techniques were used to reduce the ground bounce noise of the circuit. The ground bounce noise generation mechanisms during the sleep-to-active mode transition were identified. A two-step activation scheme with an intermediate mode was used in MTCMOS.

Dependence of the size of additional controlled transistor, the lowest ground bounce noise was produced by TTL technique among the MTCMOS circuits. The TTL technique reduced the ground bounce noise by 78.82% compared to conventional circuit. Dual-switch technique reduced the leakage current by 99.73% compared to conventional circuit. Tri-mode technique reduced the active power by 62.32% compared to conventional circuit. Table 6, shows the different noise aware combinational MTCMOS circuits with different metric. It is clear from Table 6, that ground bounce noise is greatly reduced by TTL circuit in comparison to tri-mode circuit in voltage scaling and temperature variation. The dual-switch circuit is best to reduce the leakage current in comparison to other techniques. Tri-mode circuit is the best technique to reduce the active power of the circuit as comparison to other circuit techniques.

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