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REVIEW ARTICLE

Emerging trend for LED wafer level packaging

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Abstract Currently most light emitting diode (LED) components are made with individual chip packaging technology. The main manufacturing processes follow conventional chip-based IC packaging. In the past several years, there has been an uprising trend in the IC industry to migrate from chip-based packaging to wafer level packaging (WLP). Therefore, there is a need for LEDs to catch up. This paper introduces advanced LED WLP technologies. The contents cover key enabling processes such as preparation of silicon sub-mount wafer, implementation of interconnection, deposition of phosphor, wafer level encapsulation, and their integration. The emphasis is placed on how to achieve high throughput, low cost manufacturing through WLP.

Keywords light emitting diode (LED), wafer level packaging (WLP)

1 Introduction

A light emitting diode (LED) is a semiconductor device based on the electroluminescence effect. Although such an effect was discovered in 1907, LEDs did not become practical industrial products until early 1960s. In the subsequent 30 years, LEDs were basically used for signaling, decoration, and simple display. In 1990s, with the invention of high-brightness blue LED and the development of color tuning technologies, a new trend of solid-state lighting (SSL) using LEDs started to evolve. Nowadays LED SSL has become a commercially available option to replace the conventional light sources such as incandescent and fluorescent lamps.

LEDs typically have a chip size of 0.2–1.0 mm. Such tiny devices usually have to be turned into packaged components before they can be used for the intended applications. Currently most of LED packaging processes are adopted from conventional IC packaging. Figure 1 illustrates some commonly seen LED components and their relevant packaging process flows, all packaged on a "single chip" basis. However, in the past decade, the IC packaging industries have been migrating to wafer level packaging (WLP) [1]. Therefore, there is an emerging need for LED packaging to catch up.

The basic concept of WLP is to package the whole wafer instead of individual chips. This packaging technology is very suitable for low I/O devices. WLP has the merits of high throughput and low cost. It has been evidenced by many case studies in the IC and MEMS packaging industries that WLP technologies may lead to 20%–30% cost reduction in components at high volume productions [2]. Typical applications of WLP include mobile phones, digital cameras, laptop computers, image sensors, DRAM, and integrated passive devices. According to a recent industrial survey [3], WLP reach an amazing compound annual growth rate (CAGR) of 20% (see Fig. 2). This is a solid indication showing how well the industries adopt WLP technologies.

In this paper, certain enabling technologies for LED WLP are introduced. Preliminary results of prototyping will be presented. In addition, some current industrial practices on LED WLP will be reviewed.

2 WLP with LED chip mounting on a silicon sub-mount wafer

In the past few years, some efforts have been initiated at The Hong Kong University of Science & Technology (HKUST) to introduce the WLP concept to the arena of LED packaging. Evidenced activities include the development of certain key enabling technologies for LED WLP, such as wafer level phosphor printing [4] and moldless dispensing [5] processes (see Figs. 3 and 4, respectively). A further effort was made to integrate these two enabling technologies together for prototyping [6].

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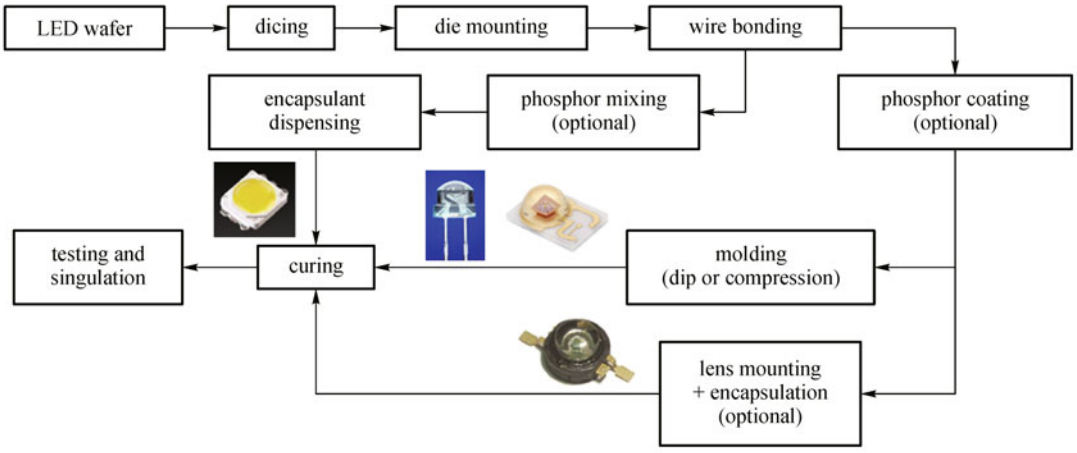


Fig. 1 Some common types of LEDs and their relevant packaging process flows (does not include the flip chip version of LEDs)

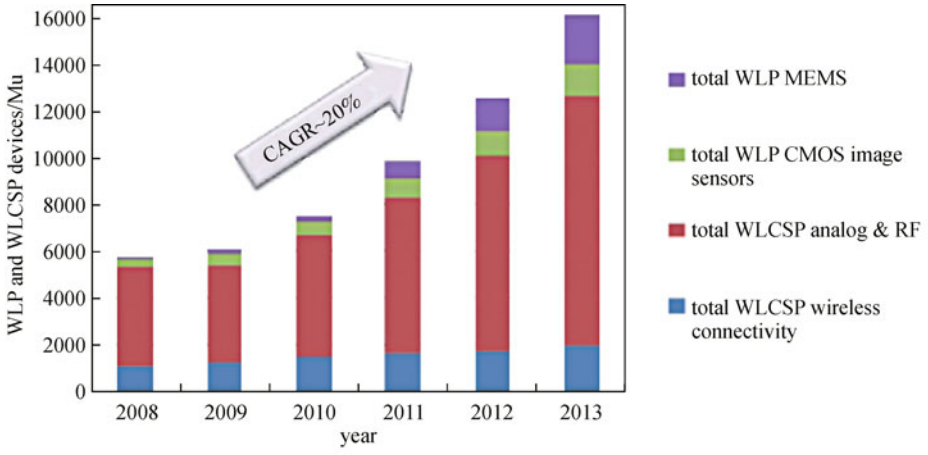


Fig. 2 Industrial survey projects a high CAGR for WLP [3]

The integrated process flow is given in Fig. 5. The results of prototyping are presented in Figs. 6 and 7. These enabling technologies were proven to be effective and useful for implementing LED WLP.

On the other hand, the industry also started to become aware of the importance of WLP technologies for LEDs. One of the major industrial leaders, TSMC, has announced an investment of USD80M to build a LED fab in two years. At their website (http://www.tsmc.com/english/lighting/index.htm), it is highlighted: "TSMC's LED chip and packaging processes are executed at the wafer level, rather than the individual LED chip level to create significant potential cost reduction… silicon-based manufacturing to deliver a fast ramp, high yield and narrow bin distribution." It is obvious that "low cost, fast throughput and high yield" are the incentives for the LED industry to move toward WLP. TSMC and its subsidiary VisEra have announced their first version of LED WLP as shown in Fig. 8.

The aforementioned LED WLP processes are basically mounting LED chips on a patterned silicon sub-mount wafer which serves as a carrier. There may be through silicon vias (TSVs) built in the sub-mount for vertical interconnection. But the silicon sub-mount wafer is flat in principle. There also exist some other versions with etched cavities built in the silicon sub-mount wafer. There are two examples of industrial practices shown in Figs. 9 and 10[1),2)]. These designs may have merits in form factors

1) http://www.tmt-mems.com/solutions.html
2) http://www.shinko.co.jp/english/corporate/outline.html

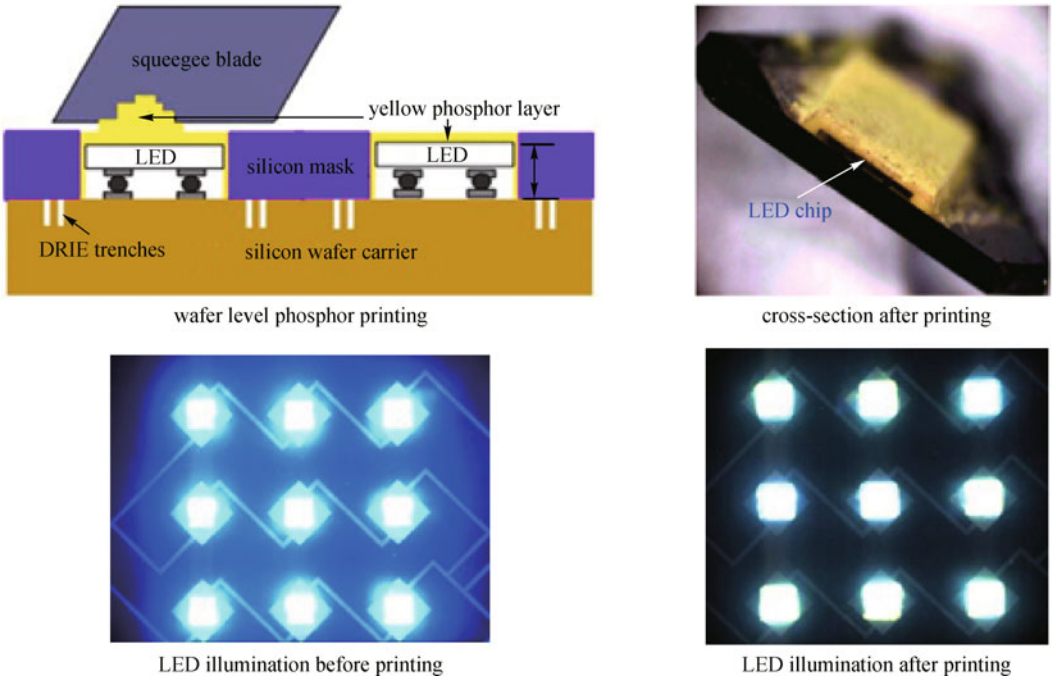


Fig. 3 Wafer level phosphor printing for LED color tuning [4]

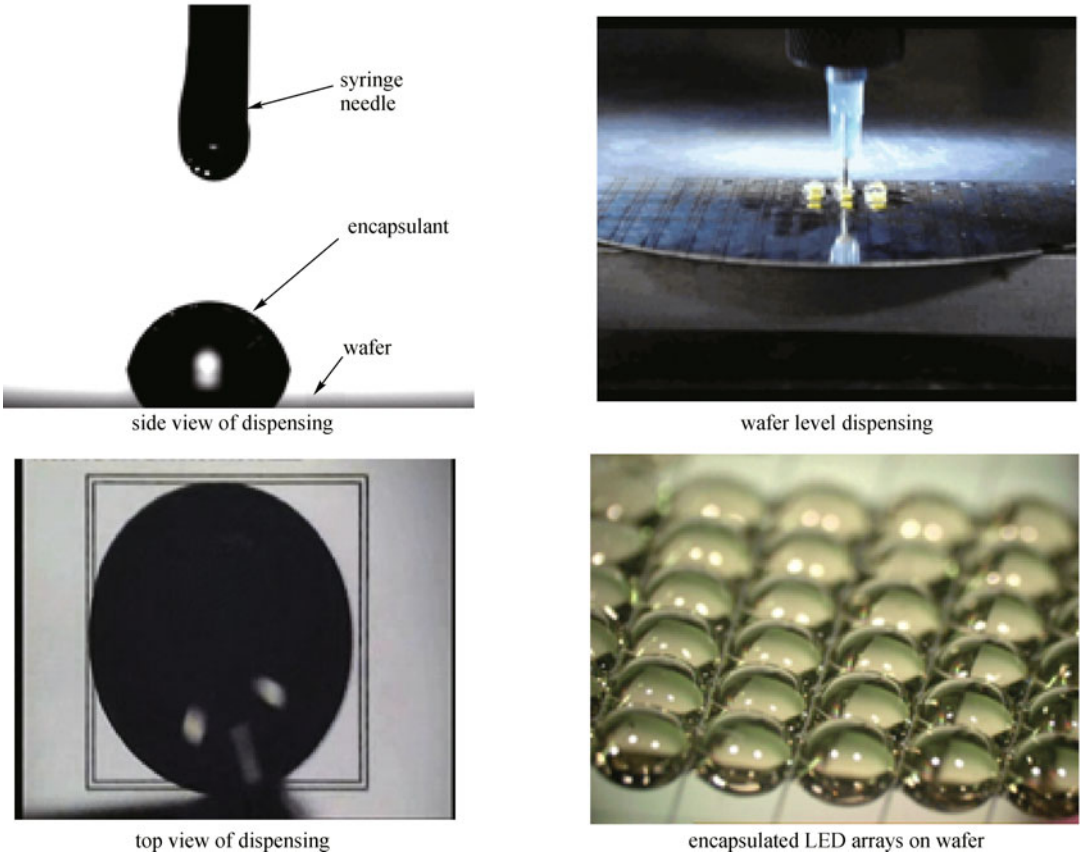


Fig. 4 Wafer level dispensing for LED encapsulation [5]

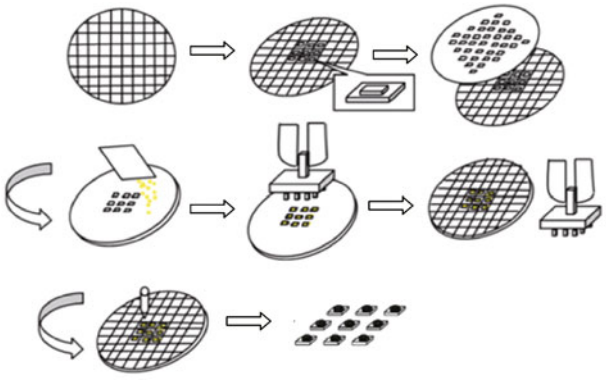
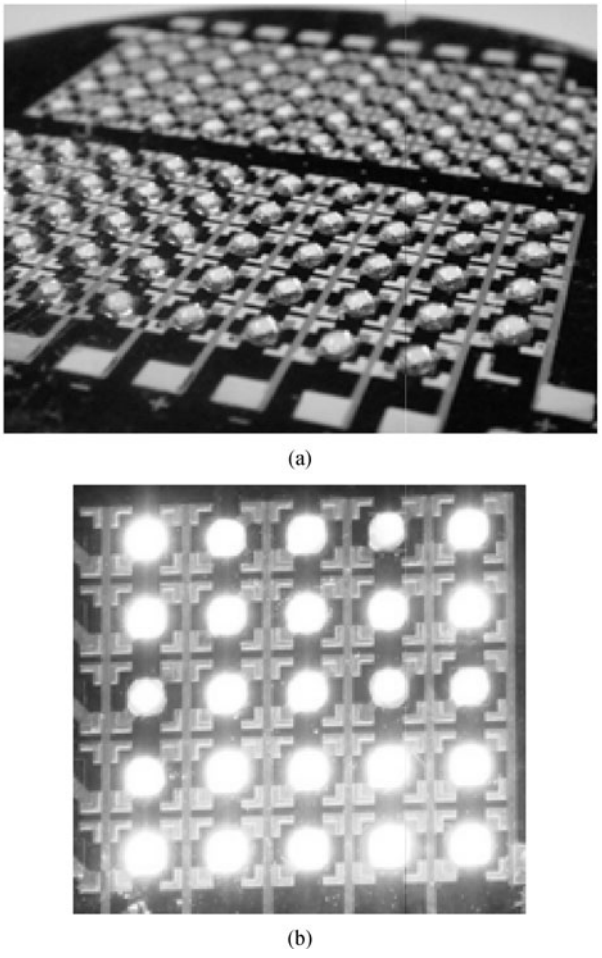


Fig. 5 LED WLP process flow with integrated phosphor printing for color tuning and moldless dispensing for encapsulation [6]



(a)

(b)

Fig. 6 LED arrays fabricated with integrated WLP processes [6]. (a) LED arrays after WLP; (b) on-wafer illumination test

and device integration. But the preparation of silicon sub-mount wafers becomes much more complicated. At HKUST similar effort was made along the same line.

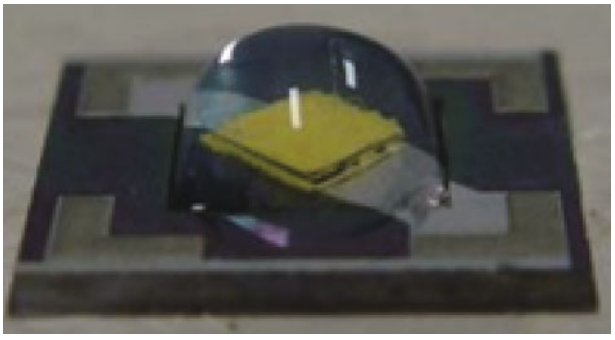


Fig. 7 Singulated component of LED WLP [6]

Cavities and TSVs are engineered into a silicon sub-mount wafer to suit LED flip chips [7]. The schematic diagram of process flow for sub-mount preparation is illustrated in Fig. 11. The fabricated sub-mount is presented in Fig. 12. Afterwards, LED flip chips are mounted in the cavities and phosphor powders are printed on the top as shown in Fig. 13. The completed prototype is presented in Fig. 14 with the LED lit up to prove the function of interconnection. It is believed this version of LED WLP should be the thinnest among all peers.

3 Proposal for full LED WLP

Although the aforementioned development involves certain wafer level processes, they still require dicing the LED wafer in advance and then mount LED chips on a silicon sub-mount wafer. In a way, this may be called "semi-WLP". For "true or full WLP", it should not require LED wafer dicing in advance. The LED wafer may be sandwiched between a silicon sub-mount wafer and a glass wafer by wafer bonding. After completing all targeted wafer level processes, the "sandwich wafers" will be diced to get individual packaged LED components, as illustrated in Fig. 15, which are ready for the next level assembly and applications. Such a kind of LED WLP may substantially reduce the manufacturing cost and increase the production throughput.

The basic concept and procedure of full LED WLP are adopted from IC WLP and MEMS packaging, and hence, the proposed wafer level processes should be implementable. This WLP structure will involve the following key enabling technologies, most of which have been implemented in IC WLP and MEMS fabrication:

1) Wafer lapping and polishing
2) Wafer etching and via forming
3) Wafer sputtering/plating/patterning
4) Wafer printing and coating
5) Wafer bonding

In particular, those processes associated with silicon wafers are considered quite sophisticated in the industry.

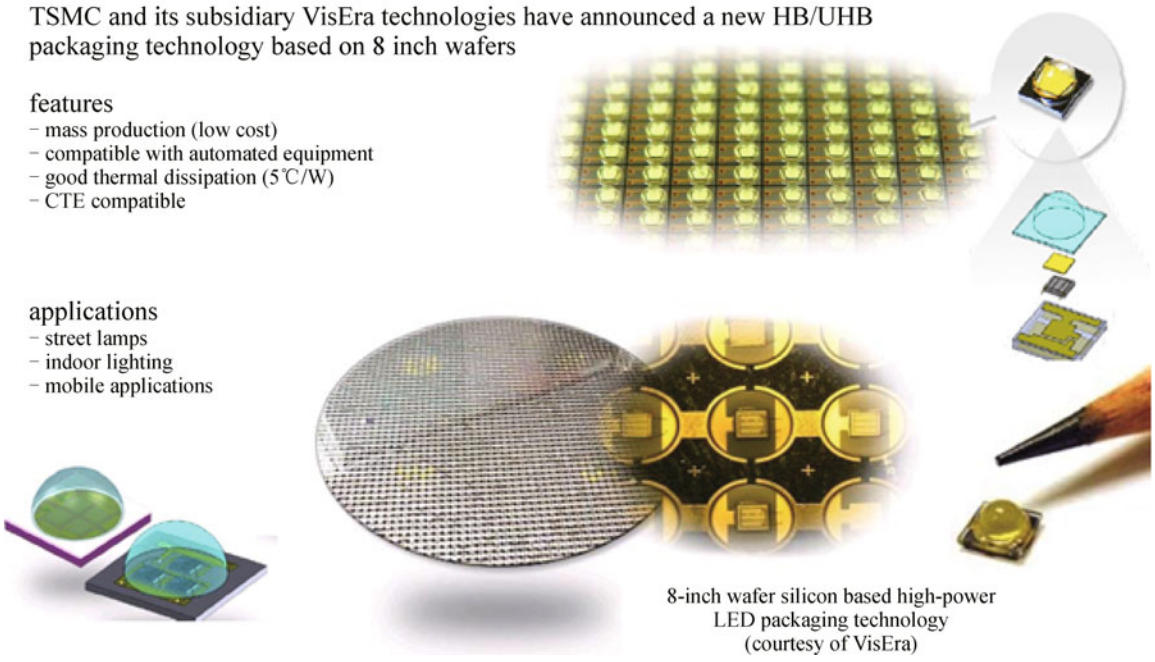


Fig. 8 Current industrial practice of LED WLP (http://www.tsmc.com/english/lighting/index.htm)

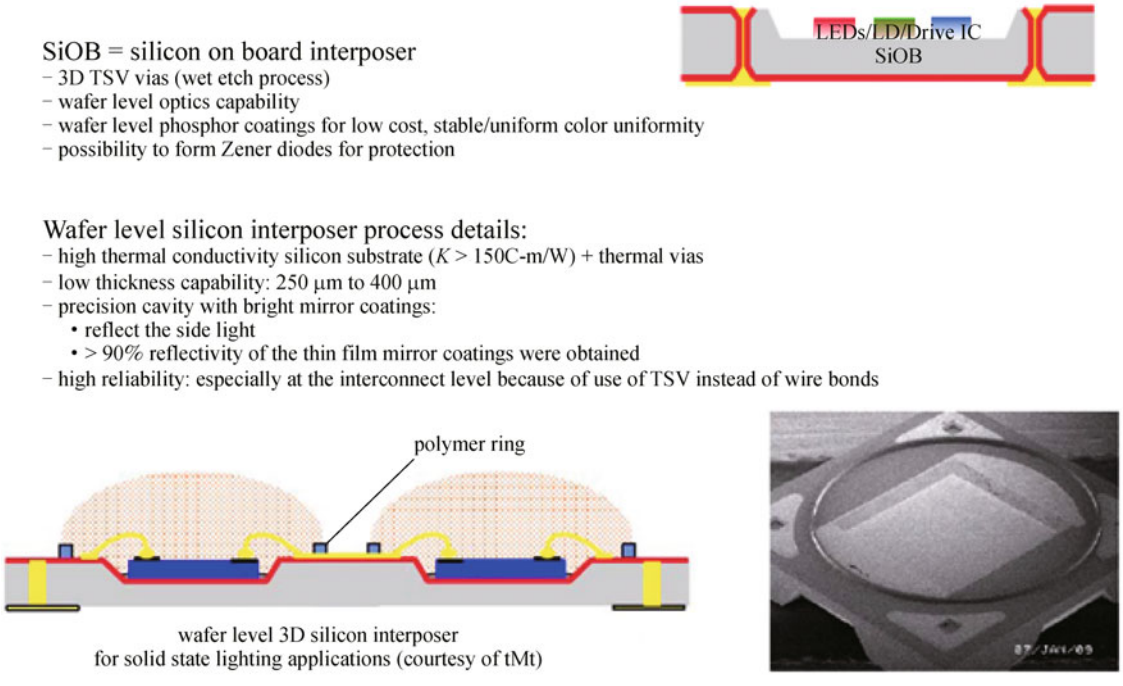


Fig. 9 LED WLP on a silicon sub-mount with cavities by tMt (http://www.tmt-mems.com/solutions.html)

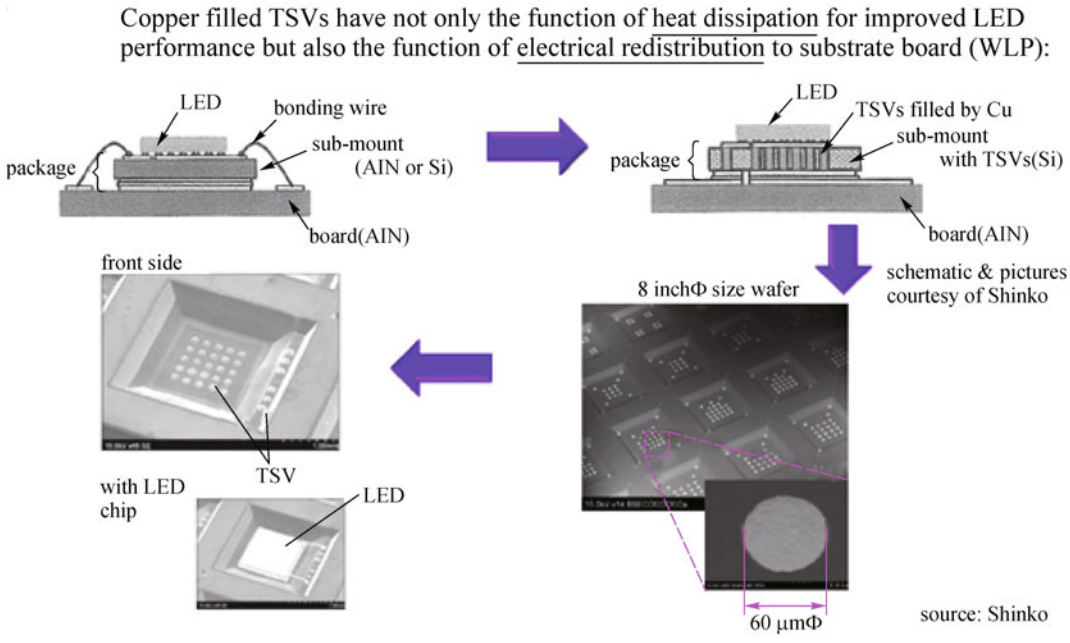


Fig. 10 LED WLP on a silicon sub-mount with cavities by Shinko (http://www.shinko.co.jp/english/corporate/outline.html)

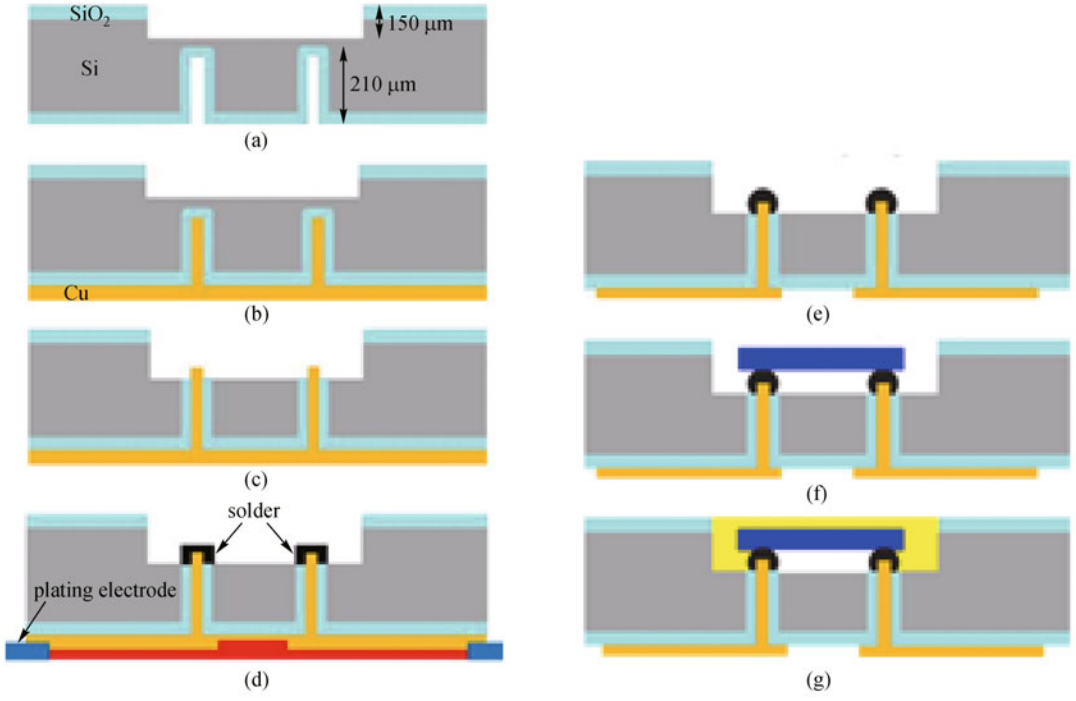


Fig. 11 Schematic diagram of process flow for a silicon sub-mount with cavities and TSVs [7]: (a) via and cavity etching; (b) via filling; (c) KOH and BOE etching to expose copper pillars; (d) solder plating; (e) reflow and RDL patterning; (f) LED chip mounting; (g) phosphor printing

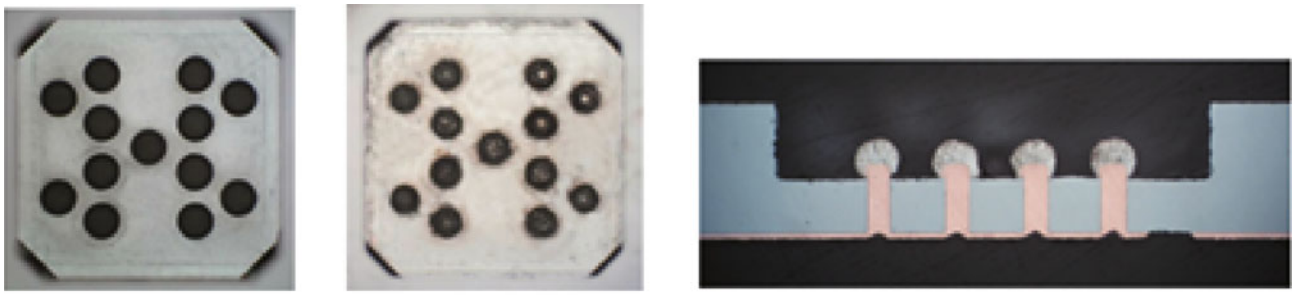


Fig. 12 Prototype of a silicon sub-mount with cavities and TSVs suitable for LED flip chip mounting [7]: placed solder (a) on copper pillars before reflow; (b) after reflow, and (c) cross-section of substrate

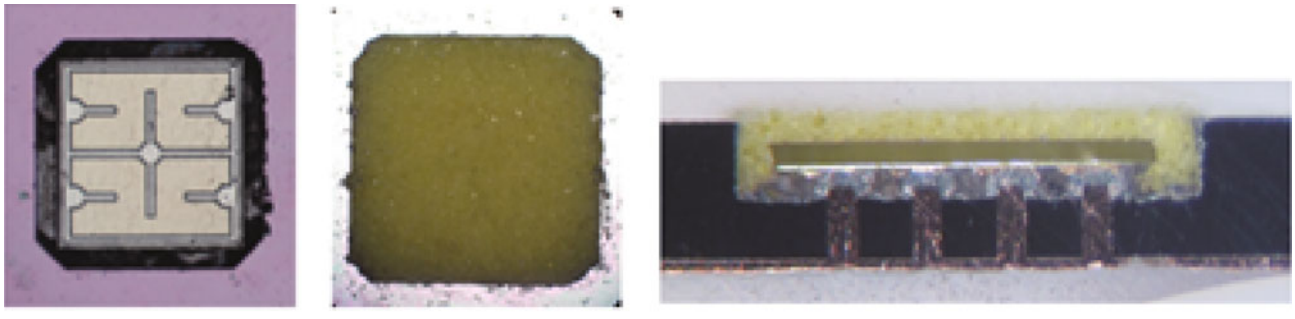


Fig. 13 Prototype of LED WLP with LED flip chips mounted on a silicon sub-mount with cavities and TSVs, and printed with yellow phosphor [7]: LED chip (a) mounted in cavity; (b) covered by phosphor powder; (c) cross-section of package

Fig. 14 Illumination of LED WLP prototype with LED flip chips mounted on silicon sub-mount with cavities and TSVs [7]: LED package (a) without phosphor printing; (b) with phosphor printing

However, although the technology basics are the same, efforts are still needed to fine tune the processing parameters in order to fit the new packaging structure and materials for optimization.

4 Conclusions

Some state-of-the-art LED WLP technologies are introduced in this review paper. The key enabling processes include sub-mount wafer preparation, interconnect fabrication, phosphor deposition, and wafer level encapsulation. In addition, the integration of enabling technologies for industrial practices on LED WLP are illustrated. At the end, a full LED WLP structure is proposed. It should be noted that high throughput and low cost manufacturing should be the main emphases for WLP.

Reference [8] reported that a yield as high as 95% could be achieved for the LED WLP process. This is a very impressive result for an emerging technology. It is believed that more LED manufacturing companies will evolve into the WLP arena. Further breakthrough in cost reduction, throughput elevation, and yield improvement are expected in the near future.

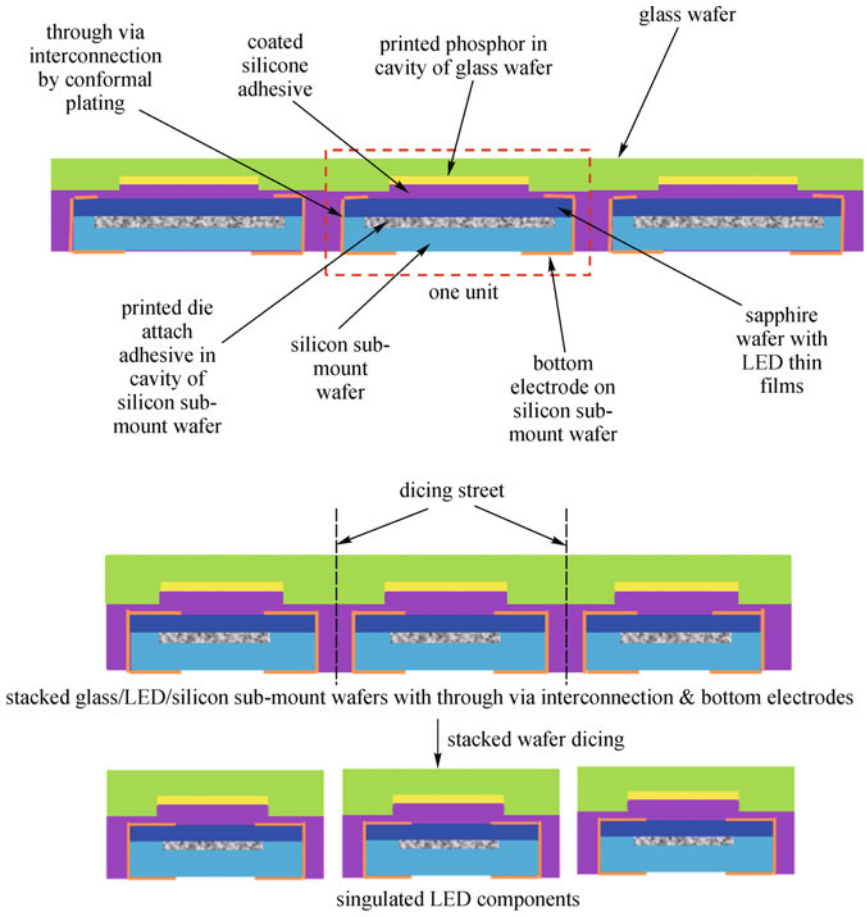


Fig. 15 Proposal for full LED WLP

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