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RESEARCH ARTICLE

High-speed optical binary data pattern recognition for network security applications

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Abstract All-optical high-speed binary data pattern recognition is one of the key technologies in network security applications. A serial pattern recognition scheme is presented, which can detect and locate a specified random target pattern within an input data sequence at high bit-rate. The logic operation principle is presented using logic equations. The logic AND/XNOR gates and a re-circulating loop at 10.65–42.6 Gbit/s are successfully demonstrated using three semiconductor optical amplifier (SOA) based gates. The experiments have successfully demonstrated the random pattern recognition up to 256-bits at 42.6 Gbit/s.

Keywords semiconductor optical amplifiers (SOAs), all-optical logic, XOR gates, high-speed optical signal procession

1 Introduction

Pattern recognition is important for optical fiber network applications, such as optical header processing and address recognition, especially in optical packet switching (OPS) networks. It is currently realized by opto-electronics via repetitive optical/electronic/optical (O/E/O) conversions, which relies on very high-speed electronic devices in the case of high bit-rate data transmission, and could be complex and costly to de-multiplex and use parallel processing by high-speed electronics. On the contrary, a simple all-optical approach is to process N bits in parallel, however it would require of N parallel high-speed gates [1], which is limited by the numbers of optical gates that could be integrated, since only hundreds of optical components can be currently integrated.

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To avoid those limitations, an alternative approach is serial processing technique, where the high-speed data can be re-circulated in a loop and permit logic operations between adjacent bits of the data [2]. The latter approach could reduce dramatically the number of optical gates and make this approach more practical. Moreover, the approach is independent of target pattern length, however in expense of increased latency. This approach could find applications such as IP address or port number recognition for OPS networks, or other data security applications. For instance, it is the task of the optical firewall being developed by the European FP6 project WISDOM[1)], where the pattern recognition in the optical layer was developed for the initial screening of incoming packets. In Ref. [3], the all-optical pattern recognition system was first proposed and demonstrated.

In this paper, we will present the overall logic operation principle and detailed experimental results of the pattern recognition system. The detailed theoretical equations are presented in Section 2. The performances of the key logic elements based on semiconductor optical amplifiers (SOAs) in the pattern recognition system will be illustrated in Section 3, where both an exclusive NOR gate (XNOR) and an AND gate in a loop will be demonstrated separately at 42.6 Gbit/s using SOAs in Mach-Zehnder interferometers (MZI). In Section 4, we will demonstrate the detailed experimental results of the complete all-optical pattern recognition system at 10.6, 21.3 and 42.6 Gbit/s, while the locations of the target pattern were correctly indicated. The discussion and conclusions will be presented in Section 5.

2 Operation logic

The pattern recognition system consists of an XNOR gate and a re-circulating loop of AND gate, as shown in Fig. 1 [3]. To find a N-bit target pattern $\{b_1, b_2,\ldots,b_N\}$ in an n-bit

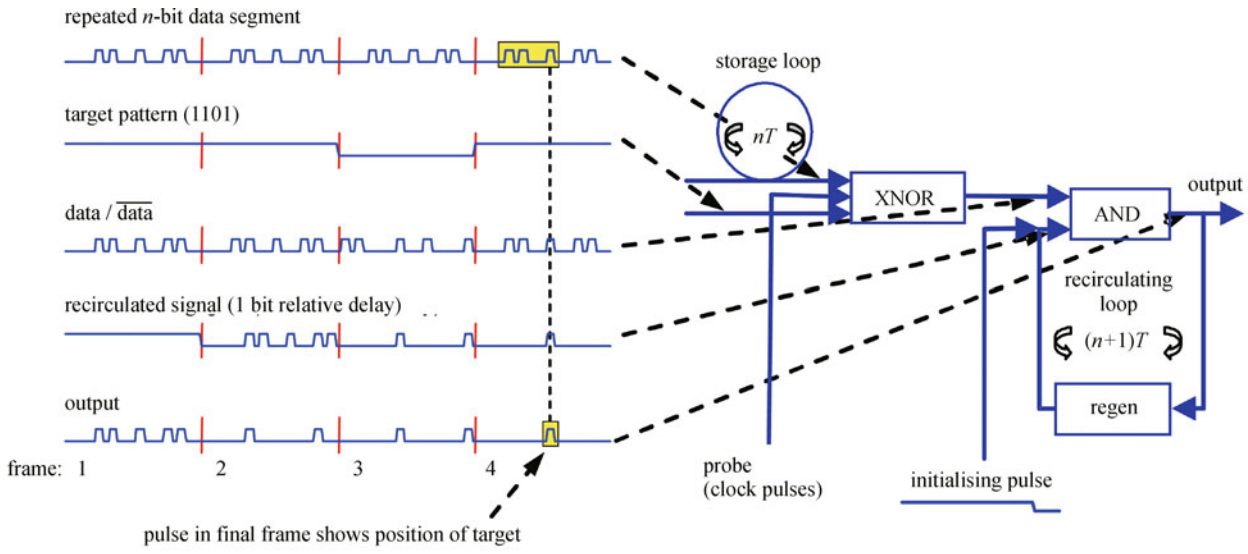

Fig. 1 Schematic of pattern recognition system

data segment $\{a_1, a_2,\ldots,a_n\}$, the data segment is repeated N times, and the target pattern is generated with a bit period of nT, where T is the bit period of the data.

The first optical gate (as shown in Fig. 1) acts as an exclusive NOR (XNOR) gate if the lengths of the MZI arms are adjusted to give constructive interference at the output. It will transmit if identical inputs are presented at A and B, because the phase-changes induced in the two SOAs will be equal and so the signals in each arm will still add constructively at the output. However, if an input having the appropriate power level is presented to just one of the inputs A or B, a π-radian phase shift will be induced in that arm and the interferometer will block the transmission. An initializing pulse is applied at AND gate input, named as the input C. The operation of the gate may be represented by the following Boolean logic expression:

$$Y = C \bullet (A == B), \tag{1}$$

where $A == B$ takes the value 1 (true), when A and B are equal or 0 (false) otherwise. It represents the exclusive NOR operation. The dot following the C indicates AND operation.

Since the initializing pulse C is presented during the first pass (numbered 0) of the n-bit sequence, thus for all the bits $C_{0,k} = 1$. The output of the first pass is therefore given by

$$Y_{0,k} = (A_k == B_0). \tag{2}$$

Note that $X_{m,k}$ denotes the kth bit of parameter X on the mth pass. k and m take integral values from 0,1,…,$n-1$ and 0,1, …,$N-1$ respectively. However, in the case of A, which is the same on every pass, the redundant m subscript is omitted for simplicity; and in the case of B, which remains constant during each pass, the k subscript is similarly omitted.

Hence, an output pulse occurs whenever a bit in the n-bit sequence matches the first bit of the target. The top part of Table 1 shows the output in response to an example sequence and a target pattern whose first bit is 1.

On the next pass of the n-bit sequence (pass number 1), the previous output is fed back to C with a 1-bit delay relative to the sequence at A. Thus C is given by

$$C_{1,k} = Y_{0,k-1},$$

so,

$$C_{1,k} = (A_{k-1} == B_0). \tag{3}$$

The output of pass 1 is obtained by substituting Eq. (3) into Eq. (1):

$$Y_{1,k} = C_{1,k} \bullet (A_k == B_1),$$

so,

$$Y_{1,k} = (A_{k-1} == B_0) \bullet (A_k == B_1). \tag{4}$$

After this pass, an output pulse occurs whenever a successive pair of bits in the n-bit sequence match bits 1 and 2 of the target ("10" in the example in Table 1).

Similarly, on subsequent passes the previous output is fed back to C with a 1-bit delay and transmitted by the gate when $A = B$. After N circulations, the output is given by

$$\begin{aligned} Y_{N-1,k} =& (A_{k-N+1} == B_0) \bullet (A_{k-N+2} == B_1) \\ & \cdots \bullet (A_{k-1} == B_{N-2}) \bullet (A_k == B_{N-1}). \end{aligned} \tag{5}$$

That is, an output pulse occurs when N bits in the repeated sequence applied to A match the target pattern applied to B.

As an example, the logic evolution of the output signal Y for a random sequence A and a target B (1011) is illustrated

Table 1 Evolution of output signal Y, for an example sequence A, and target B (1011)

		k	0	1	2	3	4	5	6	7
m	B_m	A_k	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**0**
0	**1**	$A == B$	0	1	0	1	1	1	0	0
		$C_{0,k}$	1	1	1	1	1	1	1	1
		$Y_{0,k}$	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**0**
1	**0**	$A == B$	1	0	1	0	0	0	1	1
		$C_{1,k}$	0	0	1	0	1	1	1	0
		$Y_{1,k}$	**0**	**0**	**1**	**0**	**0**	**0**	**1**	**0**
2	**1**	$A == B$	0	1	0	1	1	1	0	0
		$C_{2,k}$	0	0	0	1	0	0	0	1
		$Y_{2,k}$	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
3	**1**	$A == B$	0	1	0	1	1	1	0	0
		$C_{3,k}$	0	0	0	0	1	0	0	0
		$Y_{3,k}$	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**

in Table 1, while the corresponding waveforms are plotted in Fig. 2. The pulse indicates not only the presence of the pattern, but also its position in the sequence. A true bit in the final frame, therefore, indicates an occurrence of the complete target pattern in the data. The indicated position is important, for instance, it can tell where the pattern appears, either at the position of the input/output IP address or the port address in IP address structure. Due to the nature of serial procession, the system can search for targets of any length with the same number of gates, but at the expense of an increase in the latency to a minimum of nNT.

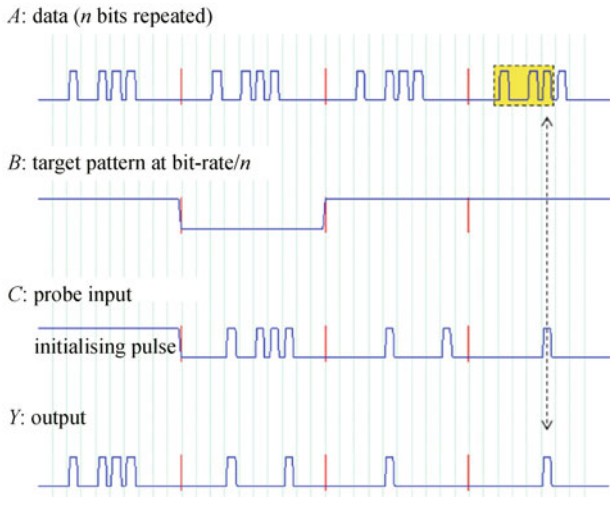

Fig. 2 Waveform evolution for the data in Table 1

3 Experimental demonstration of the key logic elements

The two key parts of the pattern recognition system, the XNOR gate and the re-circulating loop, were demonstrated separately, both at 42.6 Gbit/s [4].

3.1 XNOR gate

In Fig. 3(a), the XNOR gate was based on a push-pull 42.6 Gbit/s XOR gate using a MZI incorporating two SOAs [5]. It is a monolithic SOA array mounted on a passive silica-on-silicon planar lightwave circuit (PIC) from CIP Co. in UK [6]. Because the target pattern is a relatively slow signal, it was not necessary to use the push-pull configuration for this input. Moreover, it was possible to enter this target signal in the counter-propagating direction which allows greater flexibility in choice of operating wavelengths. The outputs of the XNOR gate were monitored by a 70 GHz sampling oscilloscope. In Fig. 3(b), the output waveforms show the original data and its inverse by setting the target high (1 level) and low (0 level) at 1 Hz. The average clock power was 0 dBm at 42.6 GHz, 3 ps pulses at 1552 nm. The target continuous-wave (CW) average power was 6 dBm at 1540 nm, and the 256-bit, 42.6 Gbit/s repeated data inputs (as push/pull pump) were 3 ps pulses at 1547 nm, with average powers of 2/−1 dBm. The applied currents of two SOAs were 300 mA. The contrast ratio of the inverted and non-inverted output signal was over 12 dB.

3.2 Re-circulating loop

The re-circulating loop was constructed by a twin MZI-SOA device consisting of 4-SOAs [6], which form two sets of MZI, as shown in Fig. 4(a). The whole fiber loop length was about 33.6 m (168 ns). Repeated 42.6 Gbit/s data patterns composed of 3 ps pulses (at 1547 nm, with a mean power of −6 dBm) were connected to the probe input of the AND gate. An initializing pulse (−3 dBm peak power)

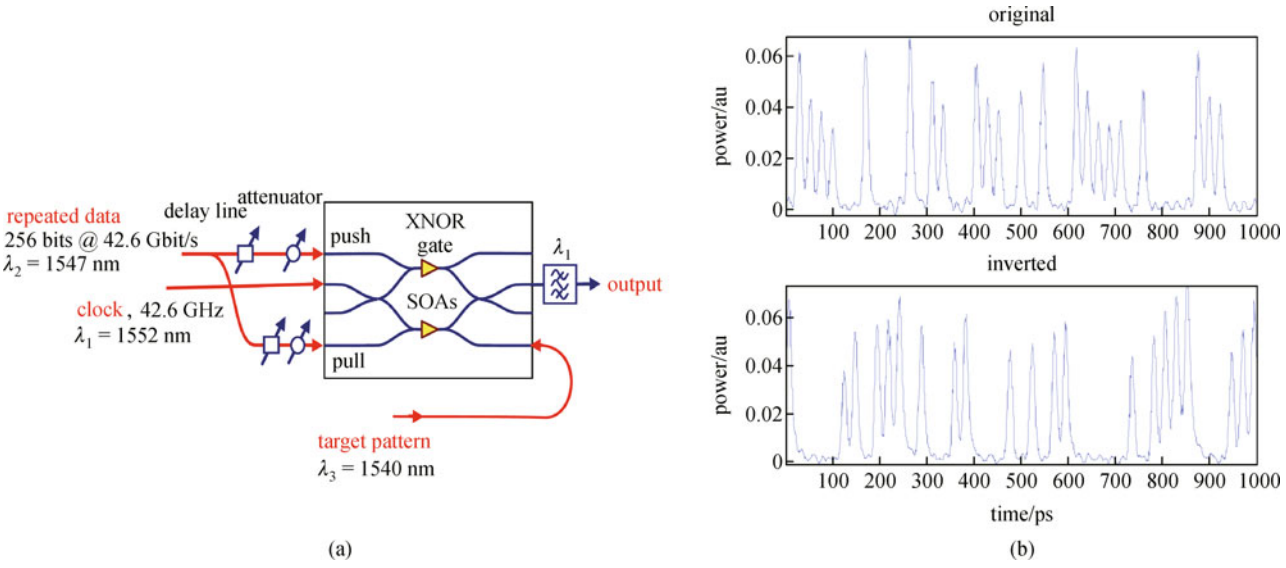

Fig. 3 Experimental setup (a) and output (b) of 42.6 Gbit/s XNOR gate for target pattern = 1 (upper frame, original) and pattern = 0 (lower frame, inverted)

allowed the data to enter the loop on one in every eight frames and an appropriately timed reset (5 dBm peak power) interrupted the CW probe to the regenerator to block any signal still circulating in the loop. The delay between the initializing pulse and the reset pulse was 168 ns. To verify the loop performance, the frames at the output port was monitored by a 70 GHz oscilloscope. During subsequent frames, the re-circulating signal reached the push and pull inputs of the AND gate and switched the data as described in Section 2. The target pattern, initial pulse and probe with reset were obtained by modulating a CW laser. The modulators were driven by a programmable pattern generator.

The output results in Fig. 4(b) show the pulse sequence evolution with respect to the number of circulations. Because the input repeated data to the loop were non-invented for all frames, it can be regarded as a special example of a target pattern 1111 1111. In Fig. 4(b), the circulation No. 7 indicates the occurrences of the specified target pattern 1111 1111, as described in Section 2. The locations of each pulse in the circulation No. 7 show the position of the last bit of the target pattern in the original data. However since the target pattern 1111 1111 is not a general one, in the next section, we will show more recent experimental results of the pattern recognition for general long patterns.

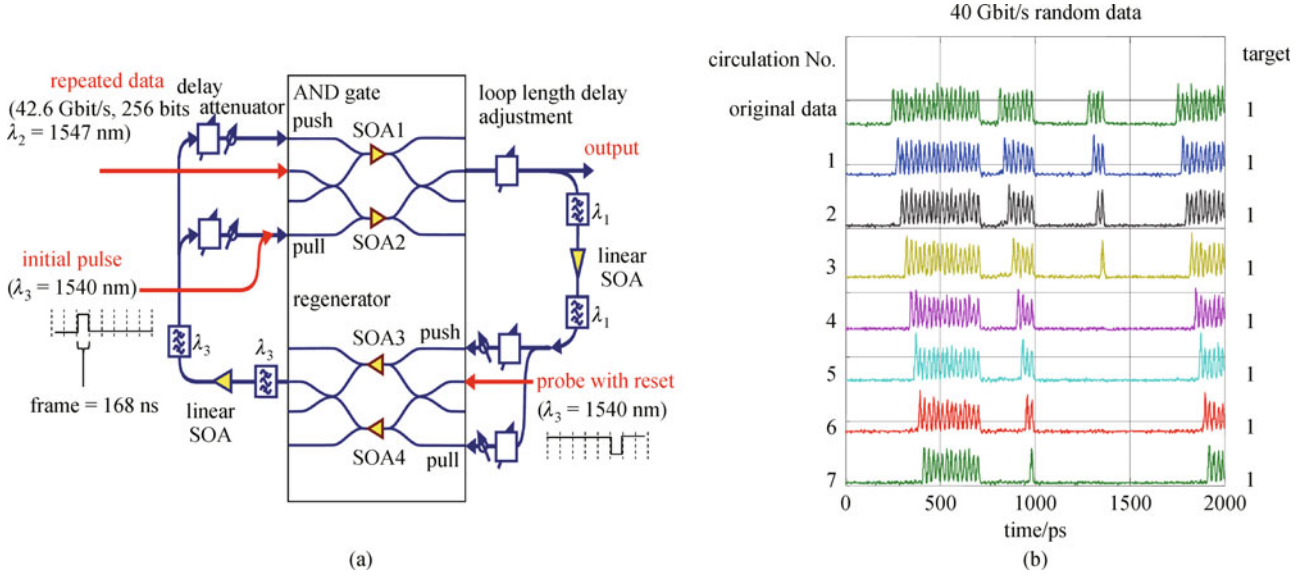

Fig. 4 Setup (a) and output (b) of the re-circulating loop at 42.6 Gbit/s. The waveforms show the evolution of the input data sequence (the original data are on top trace)

4 Experimental results of pattern recognition

The complete experimental setup of the pattern recognition scheme is basically the combination of the XNOR gate and the re-circulating loop, as described in Section 2 [7,8]. The setup is constructed with three CIP hybrid-integrated MZI gates [5], as shown in Fig. 5. The input repeated data were 64-bit at 10.65 Gbit/s, 128-bit at 21.3 Gbit/s or 256-bit at 42.6 Gbit/s. The clock signal was 2 ps pulses at 10.65, 21.3 and 42.6 GHz. The 10.65 GHz clock was the RF frequency from a 20 GHz synthesizer, which drove an external cavity semiconductor laser to provide the optical clock and the optical source before modulator.

4.1 Results of 10.65 and 21.3 Gbit/s

The output waveforms monitored on a 70 GHz oscilloscope are plotted in Figs. 6(a) and 6(b) for an 8-bit target at 10.65 and 21.3 Gbit/s. Figure 6 shows that the occurrences of the target pattern were identified from the input data sequence (only part of the repeated original data are shown

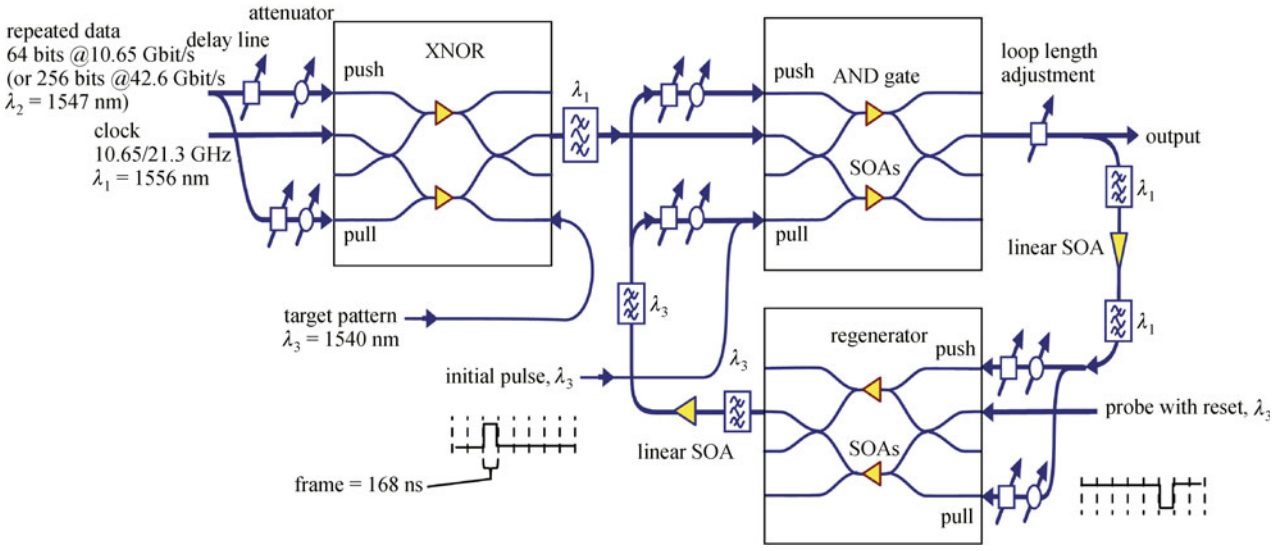

Fig. 5 Experimental setup of the complete pattern recognition system at 10.65–2.6 Gbit/s

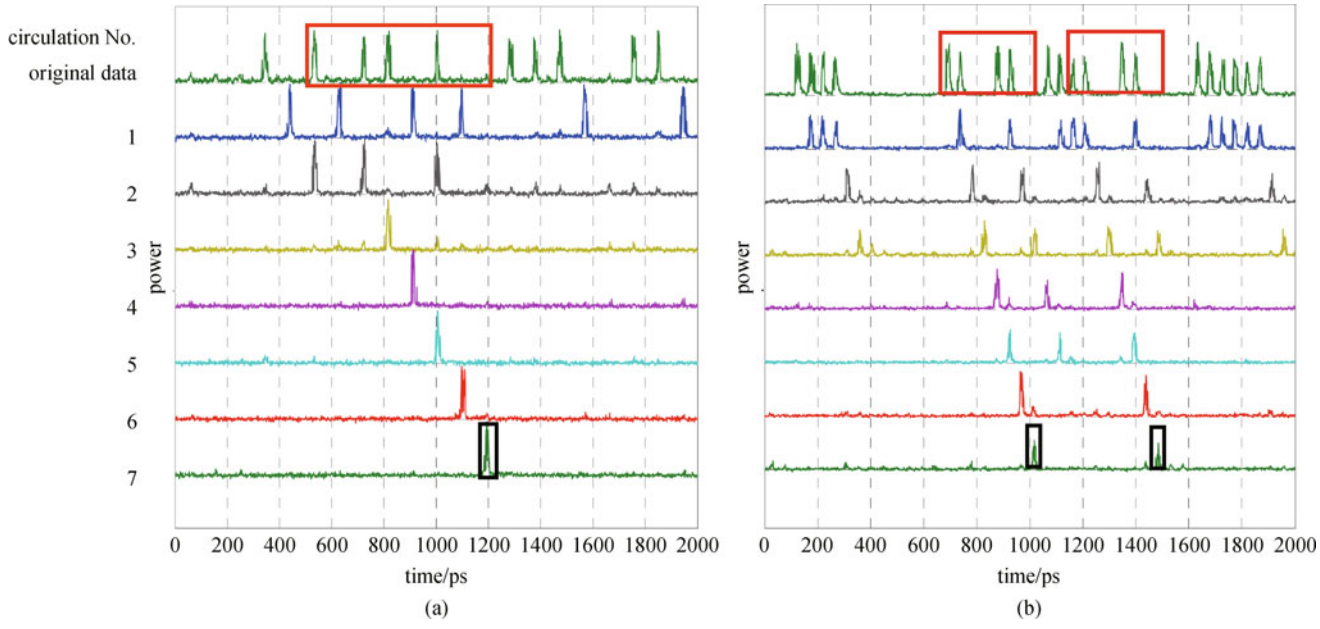

Fig. 6 (a) Recognition of an 8-bit target at 10.65 Gbit/s: 1011 0100; (b) recognition of an 8-bit target at 21.3 Gbit/s: 1100 1100. The target patterns are marked by boxes in the original data. The waveforms show the evolution of the input data sequence. Each pulse in circulation No. 7 (Marked in a box) indicates the occurrence and location of the last bit of target pattern

Table 2 Average input powers of XNOR gate, AND gate and regenerator at 10.65, 21.3 and 42.6 Gbit/s

XNOR gate	dBm at 10 Gbit/s	dBm at 20 Gbit/s	dBm at 40 Gbit/s
clock, 10/20 GHz	~13.3	2.0	6.5
push/pull	~3.4/none	1.6/−2.3	3.0
target CW	~4.0	0.8	7.2
AND gate			
data	~12.5	~7.0	~8
push/pull	~15.0	~11.4/−21.6	~6/−12
initialising pulse	~9.5	~9.5	
regenerator			
reset pulse	9.5	9.5	12
push/pull	1.0	~2.4/−15	3/−5

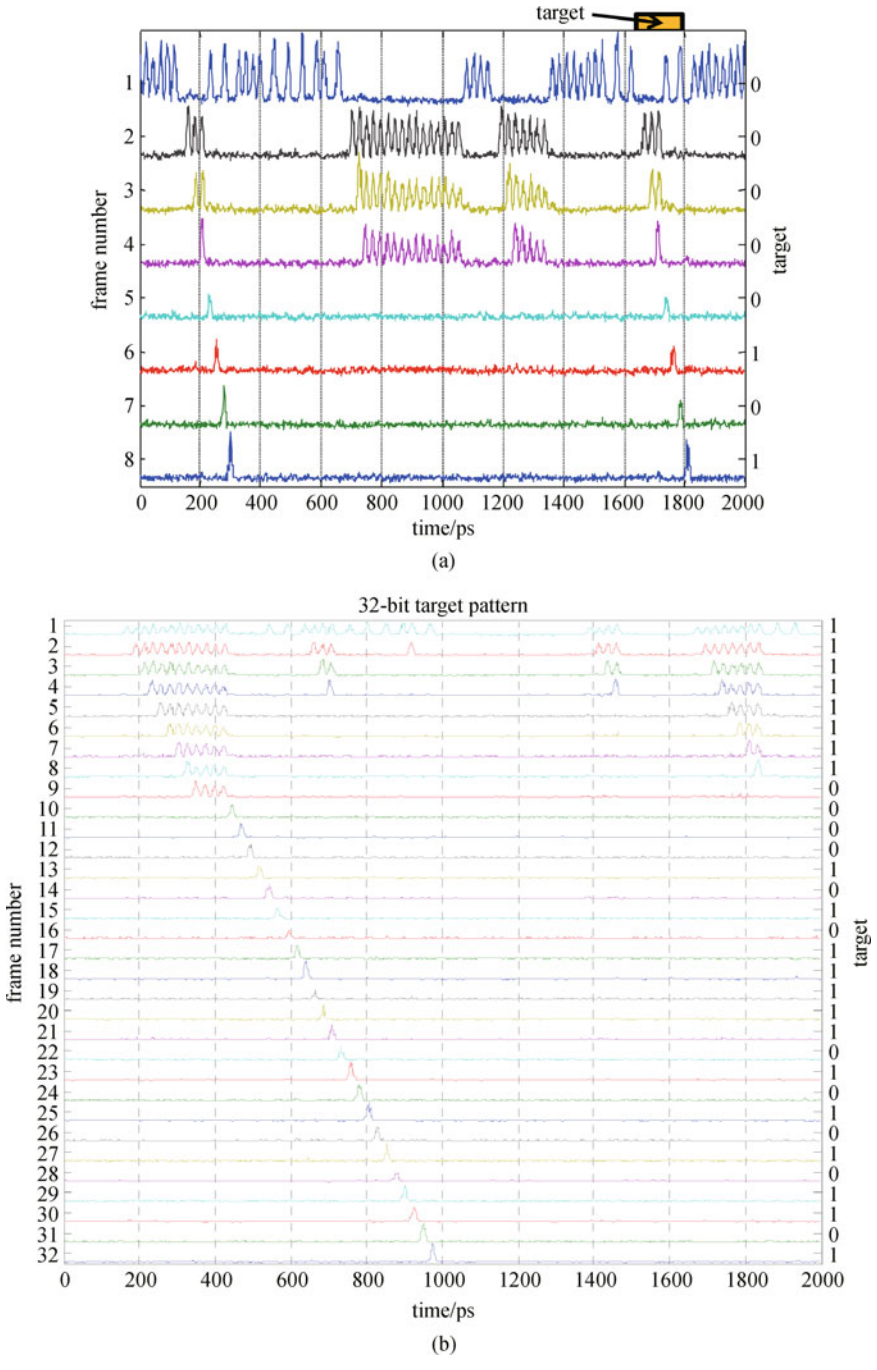

Fig. 7 Pattern recognition at 42.6 Gbit/s. (a) 8-bit target: 0000 0101; (b) 32-bit target: 1111 1111 0000 1010 1111 1010 1010 1101

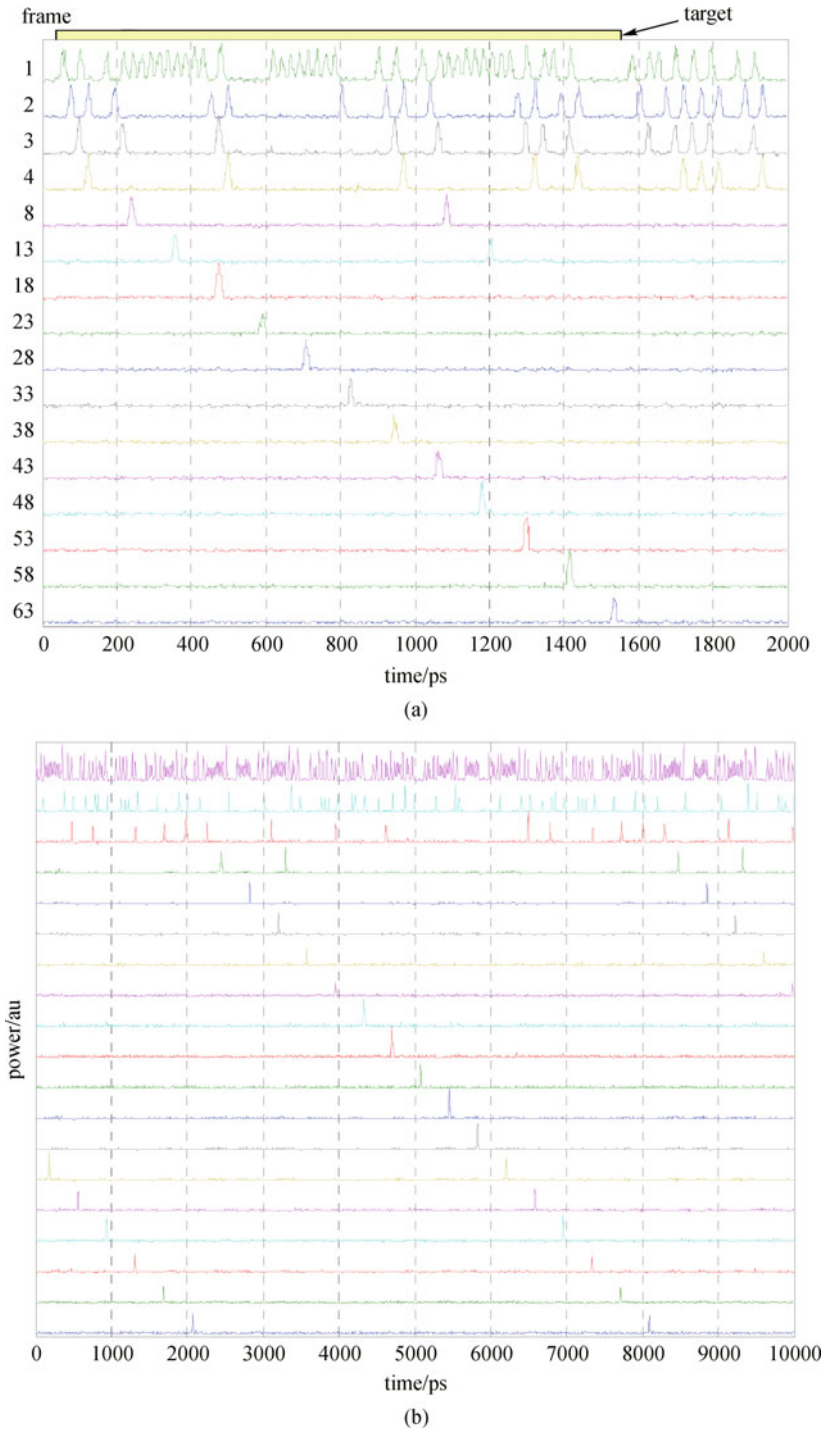

Fig. 8 Pattern recognition at 42.6 Gbit/s for target of (a) 64-bit and (b) 256-bit

in Fig. 6). Moreover, the pulse locations in the last frame (circulation No. 7) demonstrated the last bit of the corresponding target pattern. The applied currents of SOAs were 300 mA for XNOR gate, 400 mA for linear SOAs, AND gate and regenerator. Both linear SOAs have a linear gain of 23 dB. The average input powers to three logic gates are listed in Table 2. The loop fiber length was about 33.6 m, corresponding a traveling time of 168 ns.

4.2 Results of 42.6 Gbit/s

The 42.6 Gbit/s system was tested with a range of targets, varying in length from 8 to 256 bits as shown in Figs. 7 and 8. The output in each successive frame shows matches in the data to the sequence of target bits so far presented (Fig. 7). If the target is found in the data, a pulse appears in the final frame aligned with the last bit of the target. The

contrast of the output pulses was > 10dB and no deterioration was observed even after 256 frames (Fig. 8), showing that the limit to target length will be acceptable latency, not the quality of the logic signals. Latency could be substantially decreased by further integration, which would allow the length of the re-circulating loop to be reduced to fit the data segment being searched.

5 Discussion and conclusions

Both of the principle and the corresponding experiment results are presented, which show that this scheme would be useful in optical layer security check applications. For example, to search for the 16-bit IP destination address within a 16-bit data sequence at high line-rate, the required processing time will be a period of 32 bytes. If the following packet length is longer than 32 bytes (shortest IP datagram of length 40 bytes), there would be sufficient time to finish the search of the 16-bit target before the arrival of the next packet. The system does not require bit synchronization since the target signal is slow; however the loop length has to be adjusted to match the bit period. This scheme could also find many applications in high-speed optical code/word check apart from telecommunication systems. In addition, this approach could be cascaded in parallel by dividing a target pattern between multiple integrated recognition systems, in order to shorten the overall processing time.

In conclusion, we have demonstrated an all-optical pattern recognition system that can search and locate a random up to 256-bit target pattern in a data sequence at 10.65–42.6 Gbit/s. The system requires only three SOA-MZI gates for any reconfigurable length of target, which will be suitable for recognition and synchronization tasks in packet-based optical transmission systems. The two key elements of the system: XNOR gate and recirculation loop were demonstrated at 42.6 Gbit/s. The approach allows checking for any length of the target pattern, and could find various applications in high speed network security check and optical header recognition.

The operation data-rate of the optical firewall system is mainly limited by the speed of the SOA-MZI gates. Higher speed SOAs will lead to the higher data-rate operation. Further work on higher bit-rate operation and recognition of longer target pattern length is under way.

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