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RESEARCH ARTICLE

Analysis of TiO_2 for microelectronic applications: effect of deposition methods on their electrical properties

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Abstract Metal oxide semiconductor (MOS) device down-scaling is a powerful driving force for the evolution of microelectronics. The downsizing rate of metal oxide semiconductor field effect transistors (MOSFETs) is really marvelous. Silicon dioxide (SiO_2) has served as a perfect gate dielectric for the last four decades. Due to physical limitations, leakage current, high interface trap charge it now needs to be replaced with higher permittivity dielectric material. Keeping the motivation for the search of high-*k* materials, extensive studies have been carried out on several metal oxides, such as ZrO_2, Ta_2O_5, TiO_2, Al_2O_3 and HfO_2 for the replacement of SiO_2. The high dielectric constant (*k*) of titanium dioxide (TiO_2) will open multi-faceted prospects for the use of this material in microelectronic devices. In this paper, a comparative study of various deposition methods for fabrication of thin TiO_2 films has been presented. This work uses a combination of simulation results, experimental data and critical analysis of published data. Further, an experiment using sol-gel method has been carried out to deposit thin films of TiO_2. It has been characterized and compared with the earlier reported fabrication methods. The X-ray diffraction analyses and Raman spectra indicate the presence of anatase TiO_2 phase in the film. The dielectric constant as calculated using capacitance-voltage (*C*-*V*) analysis was found to be 23. The refractive index of the film was 2.43. The TiO_2 films studied for microelectronic applications and present acceptable properties such as low leakage current density of 1.0×10^{-5} A/cm at 1 V and band gap of 3.6 eV. The leakage current has been found to be dominant by the Schottky emission at lower electric field, while Flower-Nordheim (F-N) tunneling occurs at higher biasing voltages.

Keywords titanium dioxide (TiO_2), high-*k* material, sol-gel, thin films, atomic force microscopy (AFM), capacitance-voltage (*C*-*V*) analysis

1 Introduction

During the last few years, it has been observed that a transparent oxide semiconductor having optical band gap wider than 3 eV can be applied in microelectronic applications [1], i.e., UV photodiodes, transparent transistor, transparent integrated circuits, transparent electrodes, optical radiation photo detectors, wave length selective devices and solar cells, etc. The titanium dioxide (TiO_2) is the one which meets not only this requirement but also the outstanding properties, non toxicity and chemical stability in hostile environment which makes its study interesting [2]. It exists in amorphous form and crystallizes in three distinct crystallographic structures: two tetragonal phases, anatase ($a = b = 3.785$ Å, $c = 9.514$ Å) and rutile ($a = b = 4.587$ Å, $c = 2.953$ Å) shown in Fig. 1, and a third orthorhombic phase, brookite ($a = 5.456$ Å, $b = 9.182$ Å, $c = 5.143$ Å).

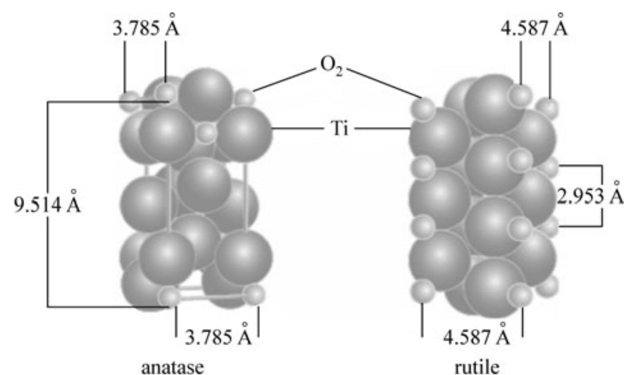

Fig. 1 Unit lattice crystalline structure

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Band gap of TiO_2 is determined by the crystal modification and in the case of thin films the reported values are 3.5 eV for amorphous films, 3.2 eV for crystalline films in the anatase phase and 3.0 eV for crystalline films in the rutile phase. As TiO_2 thin films can be applied in gate oxide in metal oxide semiconductor field effect transistors (MOSFETs) [3], it is the most promising material in photo catalytic application due to its strong oxidizing powder and high photo stability [4]. It has a high refractive index [5], high dielectric constant [6] and transparent to visible light [7]. TiO_2 films have successfully been used for photodecomposition of water and for environmental purification [8]. TiO_2 has also successfully been used as gas sensor and antireflection coating [9], as UV light emitting devices, sensors, laser diodes and other high speed electronic devices. It can be used for photo electrochemical solar cells and is also a promising material for quantum dot sensitized solar cells optical brightener in wall colors, ingredient in sun cream and bone implants photo catalysis, electro chromic devices and photovoltaic cells because of its biocompatibility [10], thermal stability, strong oxidized stability, non-toxicity and long term photo-stability. TiO_2 based gate insulators are seriously being considered for the applications of the next generation MOSFETs.

In every logic circuit, the key element is the metal oxide semiconductor (MOS) transistor, which basically constitutes an electrical switch [11]. The ever present development of the transistor manifests itself in two ways. Firstly, it has become smaller, and secondly, the number of transistors interconnected on state-of-the-art chips will be in excess of 10 billion [12]. The MOS transistor scaling beyond the present 32 nm design makes it difficult to grow high quality ultra thin oxides. Even though it is necessary to scale down the gate oxide thickness, there are two major limiting factors to overcome. First is the reliability, as the gate oxide thickness decreases, the breakdown voltage also decreases because of the increased electric field at the same gate bias; second, is leakage current especially, when the thickness of SiO_2 reaches its direct tunneling limit below 7 nm. Therefore, reducing the electric field can be reduced by increasing the physical thickness of the gate oxide or decreasing the power supply voltage. Several conduction mechanisms [5,13] of leakage current occur across SiO_2 MOS devices, i.e., Fowler–Nordheim (F-N) tunneling, space charge limited current (SCLC) mechanism, Schottky emission (SE) and Poole-Frenkel (PF) conduction, etc. But, whatever the mechanism, the electric filed was a common and basic parameter, which determines the amount of leakage current. Therefore, the challenge is to increase the physical thickness of gate dielectric, in order to reduce the tunneling current while maintaining an equivalent oxide thickness (EOT). So to keep the trend of scaling down of complementary metal oxide semiconductors (CMOS) transistors, require the replacement of conventional SiO_2 layer with higher dielectric constant (k) material for gate dielectric [14].

Many sophisticated fabrication techniques, namely, vacuum evaporation [15], molecular beam epitaxial [16], laser-assisted vacuum evaporation [17], chemical vapor deposition [18], various sputtering methods, reactive direct current (DC) or radio frequency (RF) magnetron sputtering [19], ion beam techniques [20], are used for fabrication of thin films. Although these techniques have merits of their own of having a control over the growth and for obtaining pure material but all these methods require complexity in process and of course costly equipments [21,22]. The present study aims to investigate the sol-gel process to deposit nano crystalline TiO_2 thin films on silicon substrate with very simple experimental setup. This may also be suitable for mass production. In this paper, various electrical characteristics of samples deposited by various methods have been compared with author's deposited samples by sol-gel methods.

2 Fabrication of ultra thin high-*k* films

Various thin film deposition techniques such as thermal/electron beam evaporation, pulsed laser deposition, DC/RF sputtering chemical vapor deposition and ion beam deposition have been widely used for the deposition of TiO_2 thin films. But every method has its merits and demerits in terms of quality of the deposited films as well as applications.

Chowdhury et al. [23] deposited thin film of titanium of thickness 15–20 nm using dc magnetron sputtering system on n-type Si substrate at room temperature. The growth of uniform TiO_2 films was reported using thermal oxidation of e-beam evaporated Ti films in O_2 ambient [23]. It has been shown that it was possible to achieve the leakage current density of 1×10^{-8} A/cm^2 for the films annealed at 550°C for 30 min. The flat band was estimated to be −0.6 V. The oxide charge density Q_i, is estimated to be of the order of 2.35×10^{12}cm^{-2}. The metal and semiconductor work function potential difference was found to be 0.35 V. At low temperature, F-N tunneling of electron was observed to be dominating while SCLC current mechanism was found to dominant at higher voltages. The TiO_2 films used in this study were deposited by Hitchman et al. [24] low pressure chemical vapor deposition (CVD) at various temperatures from 257°C to 400°C. Anatase peaks appear at 144, 197, 397, 515 and 637 cm^{-1} and rutile peaks were found at 448 and 612 cm^{-1}. Rutile has a larger value of peaks than anatase, while refractive indices were found 2.57 for anatase and 2.74 for rutile. In case of solar cell devices, it was reported that increasing film thickness may increase the resistance of the film because of the polycrystalline structure, and this will lead to a slight decrease in the photocurrent. These parameters are best suitable for the potential application in Solar cell and

photodiodes. Kaliwoh et al. [25] reported the deposition of TiO_2 films on crystalline silicon by plasma impulse chemical vapor deposition (PICVD). The thickness of grown films was 20 to 510 nm with refractive indices of 2.20 to 2.54 at temperature between 50°C and 350°C. The deposition rate reported by this method was 50 nm/min at 350°C. Device fabricated may have potential application in solar cell, insulating memory devices, and fiber optical sensors. Babelon et al. [27] discussed the effect of growth parameters on different characteristics of TiO_2 thin films grown on 100 Si had been studied. The grain size increases from 30 nm at 450°C to 50 nm at 550°C. Binding energy at peak was reported approximately 500 eV and band gap around 5.7 eV. However, the channel mobility was found to be very low, probably due to the presence of large interface states. Electrical properties of ultrathin TiO_2 films deposited at 150°C on strained-Si heterolayers by microwave plasma enhanced chemical vapor deposition (PECVD) had been investigated by Chakraborty et al. [27]. The extracted values of interface charge (D_{it}) were 1.19×10^{12} and 3.36×10^{11} $eV^{-1}\cdot cm^{-2}$ for as-deposited and annealed samples, and the field oxide charge densities are 5.07×10^{12} and 4.01×10^{12} cm^{-2}, respectively. Two main conduction mechanisms were invoked to explain the current transport in TiO_2 thin films, i.e., SE and F-N tunneling [23,28,29]. The SE is a process occurring across the interface between a semiconductor (or metal) and an insulating film as a result of barrier lowering due to applied field. The leakage current is found to be dominated by the SE at a low electric field (<1 MV/cm) for both as-deposited and annealed samples, whereas PF effect appears only for the deposited samples at moderate electric field (>1 MV/cm) [26,28,29].

Dalapati et al. [30] provides another possible synthesis route for forming $Si_{1-y}C_y$ layer. Samples of rapid thermal were annealed in QUPLAS reactor under flowing nitrogen at 1046°C for 30 s. In order to study the electrical characteristics of the TiO_2 films deposited on strained $Si_{1-y}C_y$ layers, MIS structures were fabricated with Al gate (area: $1.96\times10^{-3}cm^{-2}$). A separation of 5.6 eV between two peaks of Ti 2P confirms the formation of TiO_2. Inversion capacitance of the MIS capacitors is found to increase with the increase in carbon concentration due to an increase of donor like centers in the $Si_{1-y}C_y$ layers. The value of D_{it} was found to be 1.5×10^{12} cm^2/eV for the continuum model. The current-voltage characteristics of the MIS capacitors were measured and observed that the current density (J) at 1 V is 10^{-5} A/cm^2 increases sharply with bias and then almost saturates. The leakage current has been found to be dominated by the SE at a low electric field, whereas PF emission takes over at higher electric field. So may be used for the next generation metal oxide semiconductor field effect transistors [30]. Zhang and Han [31] discussed the TiO_2 anatase thin films of 1000 nm were deposited by dielectric barrier discharge enhanced chemical vapor deposition (DBD-CVD) method at 400°C for glass substrate under working pressures from 200 Pa to atmospheric pressure. The film surface is closely covered by small Particles with size about 20–50 nm but the TiO_2 film deposited at 2000 Pa with size about 100–200 nm. Depending on discharge conditions, different kinds of discharges can be generated, like glow-like discharge, corona- like discharge, or filamentary streamers. The glow-like discharge could produce more homogeneous transient plasma and it normally appears at lower pressure. Obviously it cannot be useful for microelectronics application but suitable for display devices and photo detectors. Ivan et al. [32] presented nanocrystalline Tatiana thin films deposited at ambient temperature by DC magnetron sputtering, the triangular columnar grains of the order of 70–100 nm were obtained at 400°C with pressure of 32 m Torr. The anatase and rutile films of thickness of the order of 500 nm were reported. The refractive index of the films deposited at different O_2 partial pressure was between 1.8 and 2.25 in the dispersion free region. The optical band gap values to lie between 3.3 and 3.5 eV. The band gap values for anatase TiO_2 is 3.20 eV and up to 3.70 eV have been reported for the amorphous phase. The results presented that the refractive index and crystallite size decrease with an increase in the percentage of oxygen in the sputtering environment. The band gap increase with decrease in crystallite size, which is frequently deemed to indicate the onset of quantum confinement effects, light-emitting diode (LED), etc. These may be quite expensive when large-scale production is needed. It is one of the most promising gas-sensing materials due to its high temperature stability, harsh environment tolerance and catalytic properties. Bendavid et al. [33] deposited thin films of titanium dioxide on conducting (100) silicon wafers by filtered arc deposition. The refractive index values of the amorphous, anatase and rutile films were found to be 2.56, 2.62 and 2.72 at wavelength of 550 nm, respectively. The morphology of TiO_2 on silicon substrates changes from anatase to amorphous and then to rutile phase without auxiliary heating and, by using an appropriate substrate bias. The author reported that the densities of TiO_2 films had a significant effect on the optical and mechanical properties. The effect of surface morphology of the electrodeposited TiO_2 was studied by changing the precursor concentrations of the electrochemical bath. It can be a promising as a preparation method for industrial applications. Ohsaka et al. [34] obtained the TiO_2 layers of anatase phase, well-adhered, homogenous, with good secularity and colored by interference of reflected light. Their thickness was in the range of 100 ± 500 nm. Microwave heating required short times, low temperatures and is relatively inexpensive. TiO_2 films on conducting glass were used in new types of solar cells. However, all above methods have high costs, and the preparation of films in a large area is technically difficult. Recently, wet processes, such as sol-gel and electrochemical deposition, have emerged as an

alternative route for the preparation of the crystalline TiO_2 thin films.

3 Sol-gel method

In our work, we have opted for sol-gel spin coating method and have tried to make a comparison of various fabrication methods and their characteristics required for the application of microelectronics.

3.1 Experimental detail

TiO_2 thin films were deposited using sol-gel spin coating technique. Titanium isoproxide was used as the Titania precursor. The sol was prepared with absolute ethanol and acetic acid in the molar ratio of 1:0.9:0.1. The role of acetic acid acted as catalyst. The sol was prepared as shown in Fig. 2 and stirred for 30 min using magnetic-stirrer at 90°C. Then substrate was placed on spinner and drops of the above mentioned solution were placed on surface of RCA cleaned P(100) substrate. The substrate was then allowed to spin for 2 min with spinning rate of 3000 r/min. Then wafer was baked for 20 min at 90°C. The film was then sintered in a temperature controlled resistance furnace under dynamic air at 550°C and 850°C in nitrogen ambient.

The TiO_2 film thickness and optical characteristics were determined by ellipsometry. Scanning electron micrograph (SEM) were obtained using JEOL-1200 EX model. The accelerating voltage was kept at 5 kV. X-Ray diffraction (XRD) Philips model (PW 1729) was used for XRD analyses. The target was consists of copper metal, where as nickel metal is used as β-filter. The accelerating voltage was kept at 30 kV. The tube current was kept 15 mA. For electrical measurements of the structure Al/TiO_2/Si MOS capacitor, current voltage and capacitance voltage were taken by Keithley 2400 source meter and Agilent model (4284 A) LCR analyzer respectively in a probe station. Lab view program was used to interface LCR meter with computer for plotting data.

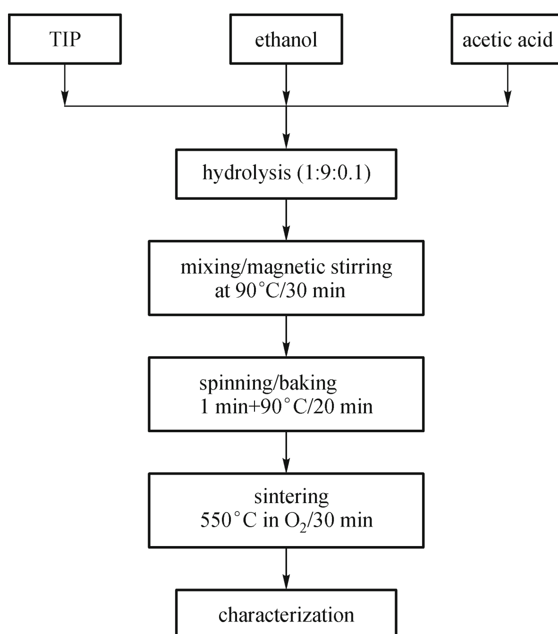
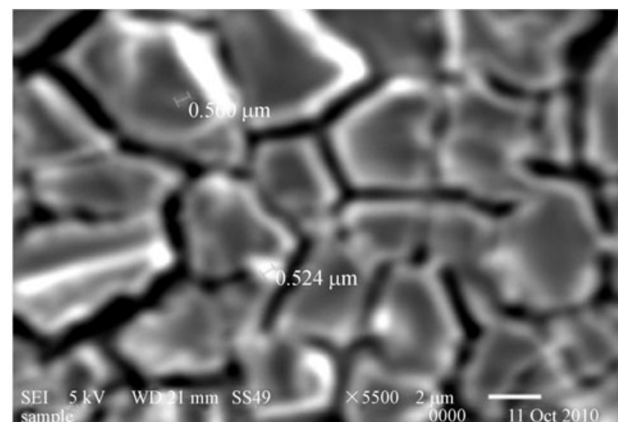


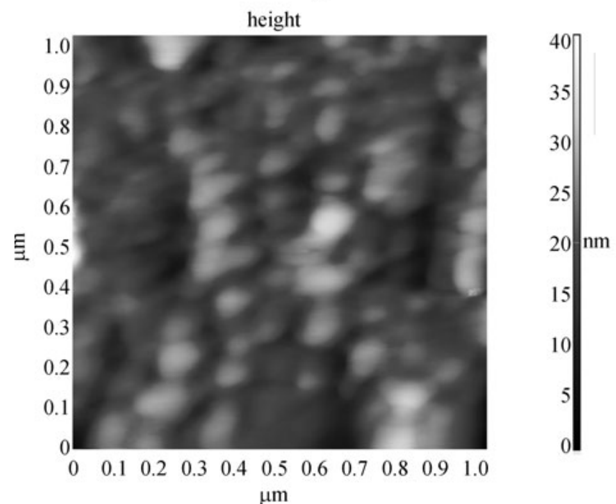
Fig. 2 Experimental setup for chemical process

3.2 Experimental results

Measurements of samples were carried out at room temperature by SEM (Fig. 3(a)) and atomic forcemicroscopy (AFM) (Fig. 3(b)). The surface morphology was obtained using AFM and field emission scanning electron microscopy (FESEM) as shown in Fig. 3, the porous nature with better crystallinity is clearly visible. The AFM topography of the as deposited TiO_2 films and annealed at 550°C revealed that surface is smooth and compact over whole substrate. The AFM images were subjected to



(a)



(b)

Fig. 3 SEM and AFM images of thin TiO_2 films annealed at 550ºC. (a) FESEM image; (b) AFM image

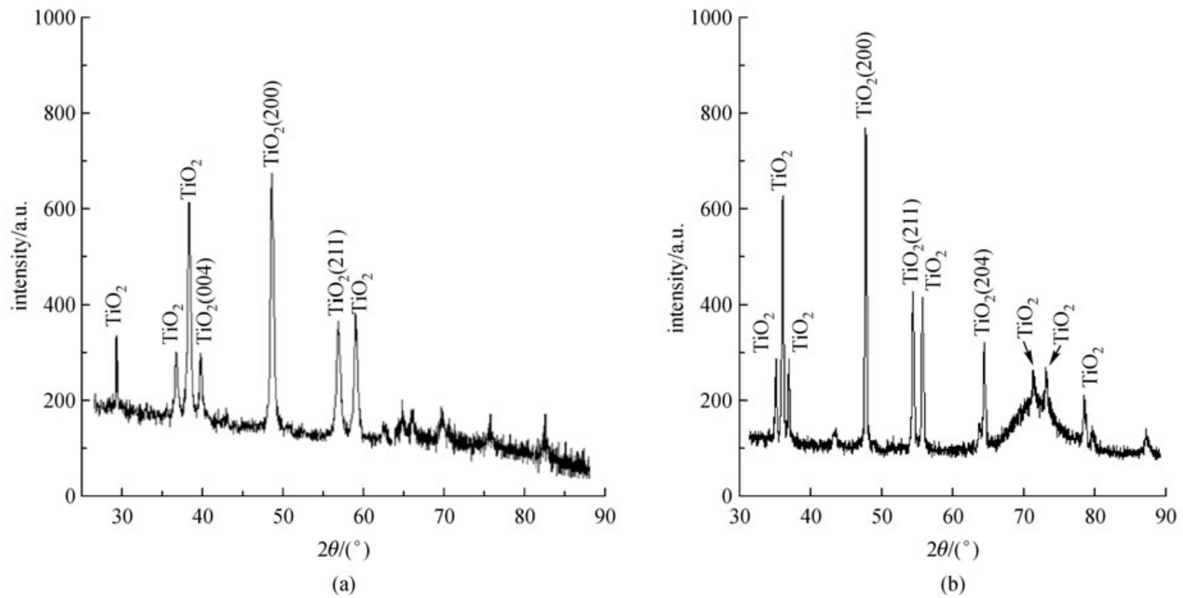


Fig. 4 XRD spectra: (a) TiO_2 film deposited on silicon wafer annealed at 550°C; (b) titanium oxide film annealed at 850°C

flattering process. Then according to quantitative analysis measured value of average roughness (R_a), root mean square (RMS) value, and coefficients of kurtosis (R_{ku}) were 0.33, 0.42, and 0.72 nm respectively at 550°C. These results were in well agreement with the literature.

Figure 4 shows the XRD pattern of the thin TiO_2 films annealed at 550°C in Fig. 4(a) and 850°C in Fig. 4(b) respectively. The amorphous nature of thin TiO_2 films was confirmed by XRD analysis. The horizontal axis represents the angle 2θ (in degrees) and the vertical axis represents the intensity of the diffracted X-Ray beam from the sample in arbitrary units. The grain size was calculated by the Scherer's formula $D = 0.89\lambda/(\beta_{1/2}\cos\theta)$, where λ is X-ray wavelength, $\beta_{1/2}$ is full width at half maximum (FWHM) of diffractions line and θ is diffraction angle, and confirmed by SEM. The XRD exhibit different crystalline phase of TiO_2 thin film and the calculated grain size of $TiO_2(004)$, $TiO_2(200)$ and $TiO_2(211)$ were 23, 37 and 54 nm respectively. Figure 4(b) shows the XRD pattern of TiO_2 film deposited at Si wafer and annealed 850°C in nitrogen ambient. The calculated grain size of $TiO_2(004)$, $TiO_2(200)$, $TiO_2(211)$ was 71, 69, and 63 nm respectively after annealing at 850ºC.

The Raman spectrum of TiO_2 nanocrystalline film anealed at 550°C is shown in Fig. 5. The spectrum is typical of anatase TiO_2 phase and also support the results of XRD analysis. The three Raman peaks at 144, 192 and 634 cm^{-1} are aggined to the E_g mode of anantase phase, which supports the result of literature [34]. The peak at 390 cm^{-1} was obtained correponding to B_{1g} mode and 519 cm^{-1} for the A_{1g} and B_{1g} modes. So TiO_2 have six Raman active modes $A_{1g}+ 2B_{1g}+ 3E_g$. The Raman spectra shows well defined peak and the absence of overlapping

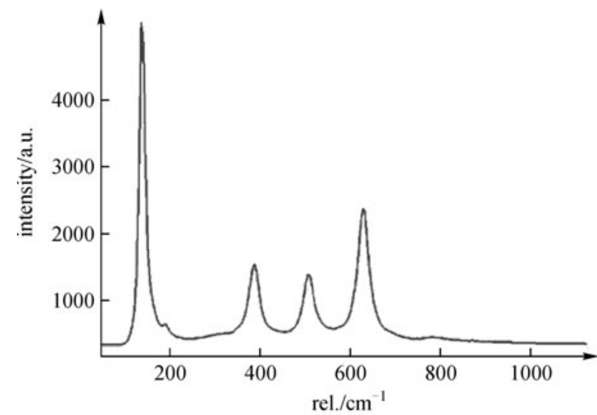


Fig. 5 Raman spectrum of TiO_2 thin film annealed at 550°C

peaks confirms the well crystallinity of thin films with low number of imprefection sites.

The variation of the capacitance (C) with gate voltage (V_G) ranging from -4.0 V to $+4.0$ V with frequency 100 kHz was obtained using Keithley 590 capacitance-voltage (C-V) analyzer for TiO_2 layer as shown in Fig. 6. The oxide capacitance (C_{ox}) is the high frequency capacitance when the device is biased for strong accumulation and found to be 54 pF. The dielectric constant of TiO_2 (high-k) 29 was observed by calculation from the knowledge of the capacitance (C_{ox}), film thickness (d), the free space charge permittivity (ϵ_0) and the area of the capacitor (A) using the relation $K= Cd/(\epsilon_0 A)$. Thickness was measured by using stylus profiler and found to be 52 nm for TiO_2 thin film.

By comparing the characteristics of the capacitor with

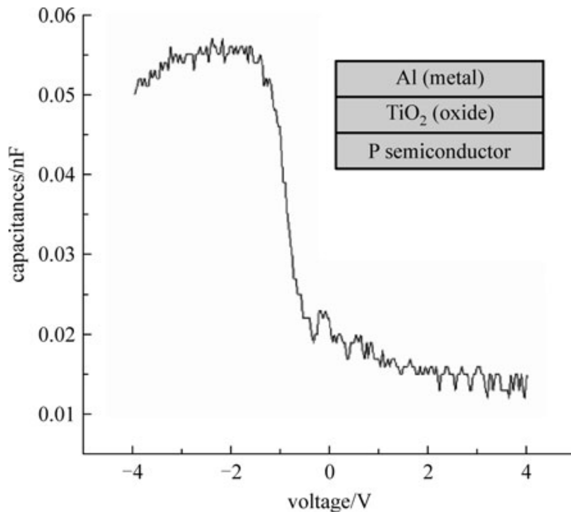


Fig. 6 *C-V* characteristics of Si/TiO_2/Al structure

ideal stimulated *C-V* curves, the flat band voltage of the capacitor was calculated 1.02 V using the relation $K = C_{ox}d/(\epsilon_0 A)$ where C_{ox} (54 pF) is taken from *C-V* graph from Fig. 6. Extrinsic Debye length calculated using the formula $\lambda = [\epsilon_S KT/(q^2 N_X)]^{1/2}$ and is found to be 184.92 Å. The gate area was calculated $1\times10^{-5}\,cm^{-2}$ using the expression πr^2 with r = 0.72 mm. Flat band capacitance (C_{FB}) can be calculated using the relation

$$C_{FB} = \frac{C_{ox}\epsilon_S A/(1\times10^{-4})(\lambda)}{(1\times10^{-12})(C_{ox}) + (\epsilon_S A)(1\times10^{-4})(\lambda)}, \quad (1)$$

was found to be 51 pF. Where C_{ox} is the oxide capacitance, ϵ_S is the permittivity of substrate material, λ is the extrinsic Debye length, A is the gate area. W_{MS} (metal semiconductor work function difference) it is found to be (−1.025 V) using the relation $W_{MS} = W_M - (W_S - \Phi_B + 0.5E_G)$. D_{it} was found to be $1.02\times10^{11}\,cm^{-2}\cdot eV^{-1}$, using the relation $1\times10^{12}\,C_{it}/(Aq)$ where here C_{it} is the interface state capacitance and A is electrode area. The effective oxide charge (Q_{EFF}) represents the sum of the oxide fixed charge (Q_F), the mobile charge (Q_M), and the oxide trapped charge (Q_{OT}). The calculation of Q_{EEF} is based on the assumption that the charge is located in a sheet at the silicon to TiO_2 interface. Its value is found to be $12.9\times10^{-8}\,C\cdot cm^{-2}$ using the relation $Q_{EEF} = C_{ox}(V_{FB} - W_{MS})$. And the effective oxide charge concentration (N_{EFF}) is computed using the equation $N_{EFF} = Q_{EFF}q^{-1}$, and is found to be 8.06×10^{11} unit/cm^3. *I-V* characteristics of TiO_2 thin films have been studied with Al/TiO_2/Si MOS capacitor structure. The input voltage is swept from 0 to ±6 V and the gate leakage current is determined. The current-voltage characteristics were shown in Fig. 7. Gate voltage is considered positive when top electrode (Al) is more positively biased then ohmic contact of MOS structure. The electrical properties of TiO_2 films as the gate bias were also investigated. It can be noted that the as

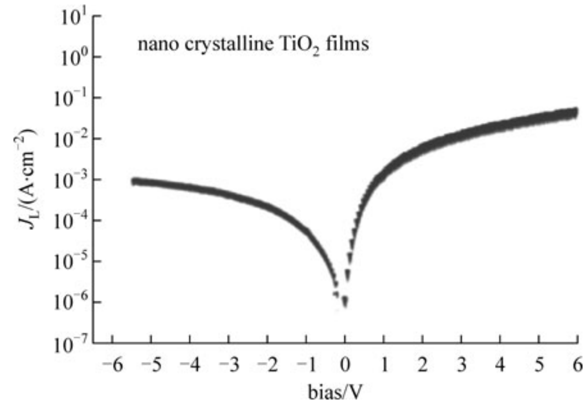


Fig. 7 Current voltage characteristics of MOS capacitor with TiO_2 film with Al top electrode

deposited film showed a relatively low leakage current (J_L) of about 10^{-6} A/cm^2 at zero bias and 5.32×10^{-5} A/cm^2 at a gate bias of + 1 V.

For higher gate voltages two prominent leakage current mechanisms were invoked namely SE and FN tunneling which were similar to reported values elsewhere [26,28,29]. The *I-V* relationship for the SE emission can be expressed as

$$J = A_{th}T^2\left[\exp\left(-\frac{qW_{MS}}{k_B T}\right)\right]\exp\left[\frac{q}{k_B T}\left(\frac{qV_B}{4\pi\varepsilon_r\varepsilon_0 d_{ox}}\right)^{\frac{1}{2}}\right], \quad (2)$$

where A_{th}, W_{MS}, ε_r, ε_0 and d_{ox} were the Richardson-Dushmann constant, metal work function, relative dielectric constant, vacuum permittivity and oxide thickness, respectively. Figure 8 shows the current (I) versus $V^{\frac{1}{2}}$ plot in semi-log scale of the observed data in the voltage range of 0.2 to 0.7 V. It is clear that the current was linear with

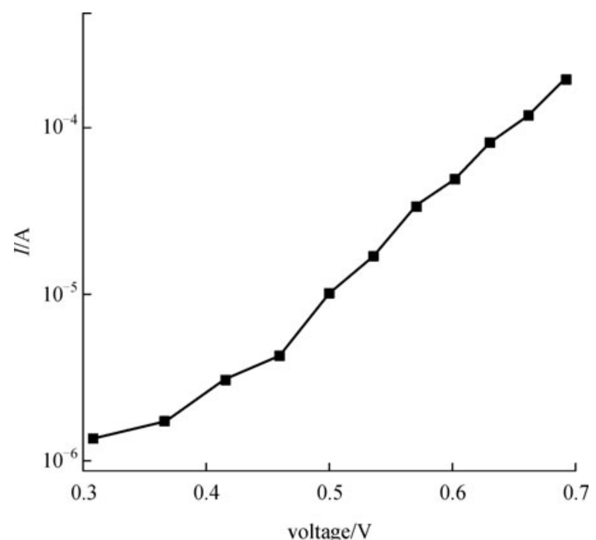


Fig. 8 SE plot of measured *I-V* data

applied electric field confirms the SE process at lower biases < 1 MV/cm. The conduction mechanism at lower biases region is dominant by thermally excited carriers known as hopping mechanism which can confirmed by Fig. 8. As the bias is increased, the current increases exponentially confirm the SE behavior. It can be observed that hopping conduction mechanism is dominant below gate voltage < 1 V while further increasing the gate bias, the conduction was invoked by F-N relationship as shown in Fig. 8. F-N tunneling can be expressed as

$$J_{\mathrm{FN}} = A_{\mathrm{FN}} V^2 \exp\left(-\frac{B_{\mathrm{FN}}}{V_{\mathrm{B}}}\right), \tag{3}$$

$$B_{\mathrm{FN}} = \frac{8\pi\sqrt{2m-m_0}\left(qW_{\mathrm{MS}}^{3/2}\right)d_{\mathrm{ox}}}{3qh}, \tag{4}$$

where A_{FN} and B_{FN} are constants.

The F-N plot of MOS capacitor is shown in Fig. 9 with conduction band offset value of 0.87 eV while theoretically it should be 1.02 eV. In case of Al top electrode, Ti ions in the TiO_2 film is reduced due to oxidation of Al. Thus aluminum oxide film continuous to grow a heterogeneous mixture of the aluminum created on top of the TiO_2 and results to change in conduction offset value. The device reliability was confirmed by the time dependent dielectric breakdown analysis (TDDB). The analysis was performed for 20 min on the MOS capacitor and constant leakage current was observed for whole operation. The increase in temperature affects the crystal size and leakage current significantly. The increase in grain size of as deposited thin TiO_2 film with respect to temperature reduces the boundary area, and so reduces the scattering electron on the surface and increase in carrier concentration, which take participate in current flow. Hence increase the conductivity with temperature. This effect on lattice structure can be confirmed with XRD analysis in Fig. 3 and also by DSC-TGA graph as shown in Fig. 10.

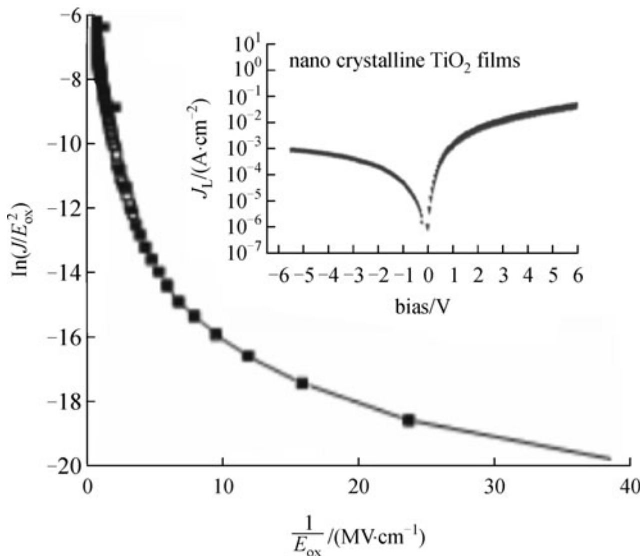


Fig. 9 F-N tunneling for TiO_2 gives conduction band offset 0.83 eV. Upper inset shows the current-voltage plot in the range from 0 to ±6 V. E_{ox} denotes electric field in the oxide layer

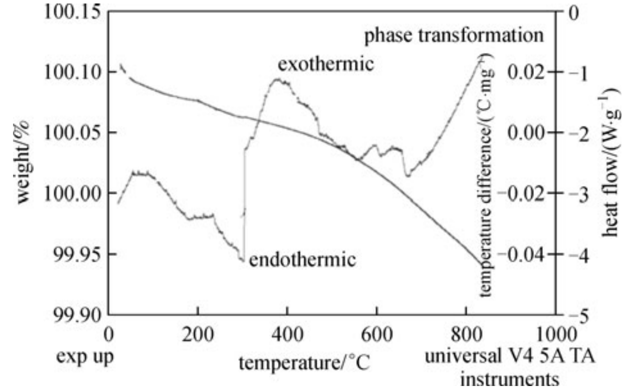


Fig. 10 DSC-TGA analysis of TiO_2 thin films

The crystalline temperature (T_{c}) was 310°C. This transition from amorphous solid to crystalline solid is an exothermic process, and results in a peak in the DSC signal as shown in Fig. 10. Thermal characterization was performed on DSC/TGA instrument with heating rate of 5°C/min in N_2 atmosphere. From the TGA curve, in the temperature range from 100°C to 400°C, a considerable weight loss of 17% is observed which is imputing the loss of water and transformation of Ti-peroxide to TiO_2. DSC shows endothermic at 250°C and exothermic peaks at around 450°C and 800°C. The endothermic peak around 10°C due to loss of water and other solvents, peak at 450°C is due to partially change of anatase to rutile phase, while another peak at 800°C completely transformation of rutile phase.

4 Electrical characteristics of various deposition methods

Table 1 shows measured and calculated data about TiO_2, electrical characteristics by considering T = 300 K, standard physical constant (q, K, ϵ_0), and electrode area 1×10^{-5} cm^2. Table 2 summarizes the major electrical and technological characteristics for various deposition methods.

We now have much better understanding on leakage current and method option for high-k gate insulator. The effect of the parameters for film production to the mechanisms of film growth is understood to some extent. There has much more research to be performed in order to clarify the relationship between microscopic aspects (interfaces, structure, and bonding) and macroscopic features and properties (crystalline, texture, etc.). The understanding of such connections is essential for

Table 1 Various characteristics of nanocrystalline TiO_2 ultra thin film grown by sol-gel

dielectric constant	band gap /eV	formation temperature /°C	silicide formation	thermal stability /°C	interface trap density /($eV^{-1}\cdot cm^{-2}$)	oxide trap density /cm^{-2}	breakdown field /($MV\cdot cm^{-1}$)	capacitance (C_{ox}) /($F\cdot cm^{-2}$)	flat band voltage (V_{fb})/V	threshold voltage (V_t)/V	bulk potential (Φ_f)	low leakage current density wrt SiO_2 /($A\cdot cm^{-2}$)
22–40	3.6	400	NA	550	1.1×10^{12}	8.9×10^{12}	<4	5.85×10^{-8}	0.37	1.2	0.35	10^1–10^2

Table 2 Comparison of main features of existing deposition methods versus our sample

electric field /($MV\cdot cm^{-1}$)		thermal (12 nm)	e-beam (15 nm)	sputtering (13.6 nm)	PECVD (15 nm)	sol-gel spin (52 nm)
leakage current	0	0		3.16×10^{-6}		
	0.5	3.16×10^{-8}	1.00×10^{-6}	1.25×10^{-5}	3.98×10^{-7}	1.00×10^{-4}
	1	3.16×10^{-7}	1.00×10^{-6}	1.58×10^{-5}	6.30×10^{-5}	1.00×10^{-3}
	1.5	3.98×10^{-6}	3.16×10^{-5}	1.99×10^{-4}	7.94×10^{-5}	1.26×10^{-3}
	2	6.30×10^{-6}	3.98×10^{-4}	5.01×10^{-3}	1.00×10^{-4}	1.58×10^{-3}
	2.5	1.58×10^{-5}	6.30×10^{-4}	6.30×10^{-3}	1.25×10^{-4}	1.58×10^{-3}
	3	5.01×10^{-5}	1.00	7.94×10^{-3}	1.58×10^{-4}	1.58×10^{-3}
	3.5			1.00	1.99×10^{-4}	1.99×10^{-3}
refractive index		2.2–2.5	2.1	2.53–2.72	2.12–2.56	2.33
optical dielectric constant		4.84–6.25	4.41	6.4009	4.4944	5.428
band gap/eV		3.2–3.5	2.69	3.0	3.25	3.4
heat treatment/°C		550–750	600	700–1000	300–450	400–550
dielectric constant		15–40	23	15–25	20–35	26–80
merits/application		can be used as gate dielectric material	best photocataystics material, junction based devices	microelectronic materials, enhance mobility MOSFET	solar cell, insulating memory devices, fiber optical sensors	next generation high-*k* dielectric material for MOS, chip
drawbacks		higher leakage current density	5 nm roughness in surface, leakage current	mass fabrication is expensive	mass fabrication is expensive	higher silicon/dielectric interface density

Notes: Data from Refs. [18, 20, 24, 28, 35–38] and some other sources, slightly different values of those parameters were report time to time

establishing defined and reproducible processes. The leakage current depends upon the deposition method as shown in Table 2.

5 Discussion

In the present study, it was found that TiO_2 is a possible candidate among the gate insulators because its anatase type has a high dielectric constant of approximately 27 and good thermal stability on Si. Conduction band offset of 1.2 eV with silicon can act as better gate dielectric with high gate capacitance with less leakage current in sub-micron regimes of CMOS ultra large scale integration. The band gap of material was reported 3.6 eV. The acceptance for most modern CMOS fabrication facilities, TiO_2 has extensively been investigated as a possible SiO_2 replacement [39] for the fabrication of new generation of dynamic random access memories (DRAMS) and micro-electromechanical systems. A smaller grain size increases the surface area to volume ratio that leads to an enhancement of surface processes, as photo catalytic activity and humidity adsorption capacity [38]. TiO_2 have too low conduction band offset and can react with the silicon substrate. In addition, TiO_2 is found to have a low crystallization temperature of about 400°C which is below most of the processing temperatures in the present CMOS technology. The grains of the titanium dioxide film were of the order of nanometers. It was also observed that grain size improved with increased annealing temperature. The further improvements in deposition process are required to make thin films suitable for MOS devices.

6 Conclusions

Main aspects for film deposition methods are economy and ecology, to make the technique an increasing demand of future. In the past ten years, various methods have been employed to coat TiO_2 thin films on supporting substrates for substantial applications, like water and air purification, self-cleaning, fabrication of various semiconductor devices

in microelectronics industries etc. among which, the sol-gel process has been long utilized to prepare Anatase TiO_2 films. However, it still remains a problem for a large scale production in the long run. The commercially more established process of CVD seems to be mostly suitable for large-scale industrial production of TiO_2 thin films. Solid phase epitaxial method also has potential but cathode electro deposition seems promising as a preparation method for mass production and industrial applications. The sol-gel method is simple, inexpensive, non-vacuum, and low temperature technique for deposition of films. TiO_2 by thermal oxidation is considered as one of the potential methods because the current density was observed three orders of less magnitude than other methods. Generally, high crystalline nature of TiO_2 is desired for its applications in CMOS devices and as an electrode of a photovoltaic device. When oxide thickness is in nanometer scale, even small non-uniformity either in chemical composition or even at surface fluctuation leads to increase leakage current by 10 fold. It has been reported that EOT of 3.6–13 nm is achieved with TiO_2 as gate dielectric and also reduced leakage current by two orders of magnitude is achieved.

In this study, we successfully deposited thin TiO_2 films by sol-gel method and compared with other traditional methods. It has been observed that the dielectric constant is 26 and grain size which is found to be tens of nm in case of silicon wafer in air at 550ºC and grain sizes increases with 850ºC in nitrogen ambient. The X-Ray diffraction studies show that the nature of deposited film was amorphous. The high value of leakage current and interface trap density requires more research. Further improvements can be done in deposition process and annealing process in order to bring the interface trap charge density and leakage current value at minimum level. So these parameters enhance the acceptability of TiO_2 for the fabrication of quantum dot solar cell and for ultra thin gate electrodes. This may make the thin TiO_2 films suitable for futuristic CMOS devices.

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