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RESEARCH ARTICLE

Charge trapping memory devices employing multi-layered Ge/Si nanocrystals for storage fabricated with ALD and PLD methods

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Abstract The Ge/Si nanocrystals on ultra thin high-*k* tunnel oxide Al_2O_3 were fabricated to form the charge trapping memory prototype with asymmetric tunnel barriers through combining the advanced atomic layer deposition (ALD) and pulse laser deposition (PLD) techniques. Charge storage characteristics in such memory structure have been investigated using capacitance-voltage (*C-V*) and capacitance-time (*C-t*) measurements. The results prove that both the two-layered and three-layered memory structures behave relatively qualified for the multi-level cell storage. The results also demonstrate that compared to electrons, holes reach a longer retention time even with an ultra thin tunnel oxide owing to the high band offset at the valence band between Ge and Si.

Keywords high-*k* tunnel oxide, equivalent oxide thickness (EOT), charge trapping memory (CTM) prototype, atomic layer deposition (ALD) technique, multi-level cell (MLC) storage

1 Introduction

Nanocrystals (NCs) based memory [1,2] is considered a promising candidate for the conventional poly-Si film floating gate memory owing to its low voltage programming/erasing characteristic, enhanced retention and endurance. Both theoretically and experimentally, the stacked hetero-structure proves to be a most hopeful way to overcome the trade-off between long retention time and high programming/erasing (P/E) speed [3,4]. High-*k* materials, such as HfO_2, ZrO_2, Al_2O_3, could maintain larger physical thickness while having the same equivalent oxide thickness (EOT) with SiO_2. Thus, it is favored and gradually imported into complementary metal oxide semiconductor (CMOS) process and charge trapping memory (CTM) products as either tunnel dielectric or control dielectric [5,6]. As the memory scales down, high density flash, using the multi-level cell (MLC) storage such as multi-bit or multi-layer [7,8], comes up, reducing the cost per bit at the same time.

2 Experiment

In a fabrication process, a 4 nm ultra thin tunnel oxide, Al_2O_3, was grown on p-type Si wafer with atomic layer deposition (ALD) method. Then mono-/bi-/tri-layered $(4\,nm\text{-}Si/2\,nm\text{-}Ge/2\,nm\text{-}HfAlO)_n$ ($n = 1,2,3$) film was deposited on the tunnel oxide in the pulse laser deposition (PLD) chamber with their co-target at 400°C in 6E-4Pa ambient. Afterwards, a 20 nm thick control oxide, HfAlO ($HfO_2:Al_2O_3 = 1:1$), was *in-situ* deposited also in the PLD chamber. Later the samples were annealed using rapid thermal annealing (RTA) at 750°C for 90 s, 800°C for 45 s/60 s/90 s in N_2 atmosphere, to form nanocrystals. Finally, the CTM prototype was accomplished with the thermal evaporation for Al electrodes. Figure 1 gives the final schematic structure of the CTM prototype based on bi-layered Ge/Si NCs.

The surface morphology of the three samples was observed by tunnelling electron microscopy (TEM). The behavior of charge storage of the CTM prototype was characterized using high frequency capacitance-voltage (*C-V*) and capacitance-time (*C-t*) measurements at 1 MHz with Agilent 4284A.

3 Results and discussion

Figure 1 gives the schematic diagram of bi-layered Ge/Si NCs based CTM prototype devices. The other two, the mono-layered and tri-layered ones, are similar.

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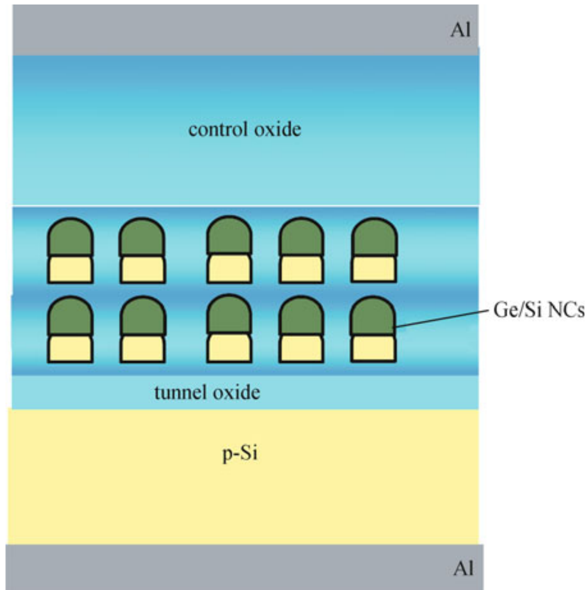


Fig. 1 Schematic diagram of bi-layered Si/Ge NCs based CTM

Figure 2 shows the TEM image of the bi-layered Ge/Si NCs based CTM sample. The density and diameter of NCs are about 2×10^{10} cm^{-2} and 5 m, respectively.

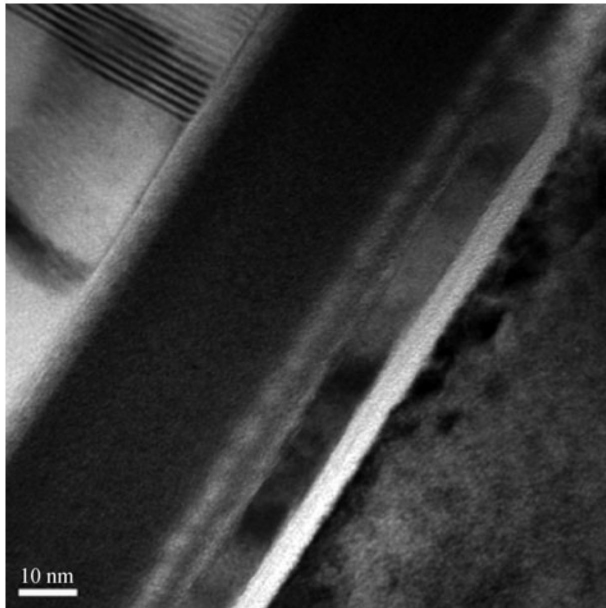


Fig. 2 TEM image of bi-layered Si/Ge NCs based CTM

The *C-V* hysteresis loops of the bi-layered Si/Ge NCs based CTM are shown in Fig. 3. A counter-clockwise hysteresis is clearly observed. It indicates that the hysteresis is induced by the holes in accumulation range and electrons in inversion range tunneled from the substrate rather than by the traps in the gate oxide. The

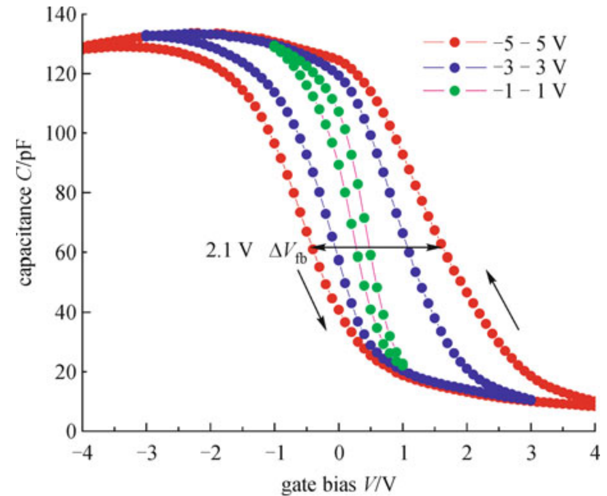
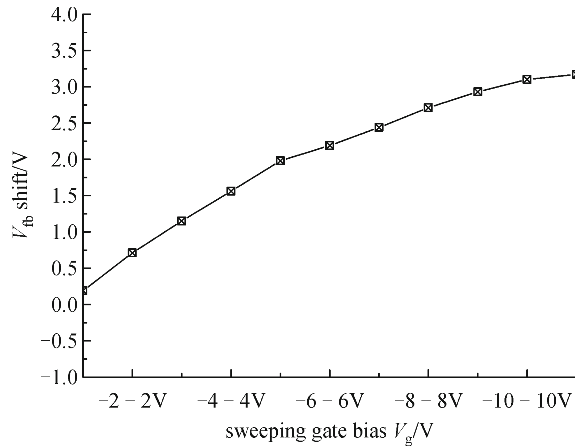


Fig. 3 *C-V* hysteresis loops of bi-layered Si/Ge NCs based CTM

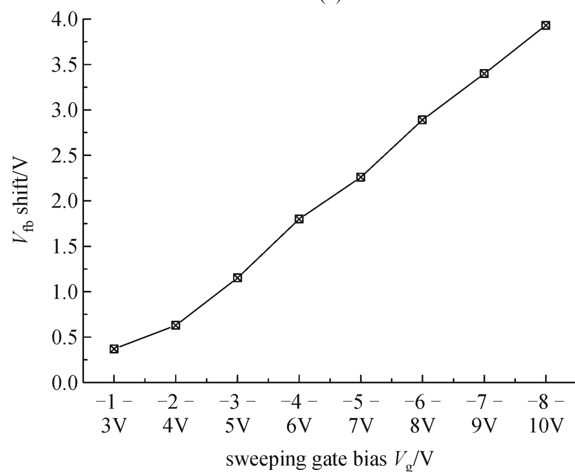
window of the flat-band voltage V_{fb} shift is only 0.3 V when sweeping between −1 and 1 V, and it rises to about 2.1 V under the sweeping voltage range between −5 and 5 V. It could also be seen that a gate bias as low as 3 V could yield about 1.0 V V_{fb} shift, the limit for one-bit read/write. This virtually makes it eligible for low-voltage, low-consumption memory devices.

The fact that hysteresis window is dependent on the range of sweeping voltages are shown more clearly in Figs. 4(a) and 4(b). Figure 4(b) also reveals the information that applied to −8–10 V gate bias voltages, it could yield as large as a 4.0 V V_{fb} shift, indicating the possibility of a two-bit operation (4 states, each distinguished by 1 V).

The retention characteristics of the charge storage were surveyed with the constant voltage method at the flat-band voltage. As shown in Fig. 5, *C-t* curve of bi-layered Si/Ge NCs based CTM, the leakage of holes is only about 18% in 10^4 s after the stressing of −7 V for 1 s and it gradually remains at this level. It is also noted that the injected holes have a considerable longer retention time than that of the electrons. This could be explained by the band offset between hetero-structures. As displayed in Fig. 6, the high band offset between Ge and Si at the valence band is about 0.51 eV, greatly larger than the thermal activation energy (0.026 eV~kT). As a result, the injected holes should store mainly in the side of Ge, which suggests a promising way for the realization of long time retention. On the other hand, it could be seen from Fig. 5 that most of the injected electrons charged at 7 V for 1 s leak out after 10^4 s, since the electron affinity of Si (4.05 eV) is 0.05 eV larger than that of Ge, and the injected electrons mainly store in the side of Si NCs and will easily tunnel back to the substrate subsequently. Details about the charge leakage processes and mechanism during retention are clearly explained in Ref. [4]. The conclusion could be drawn that



(a)



(b)

Fig. 4 (a) V_{fb} shift versus V_g of bi-layered Si/Ge NCs based CTM; (b) V_{fb} shift versus V_g of tri-layered Si/Ge NCs based CTM

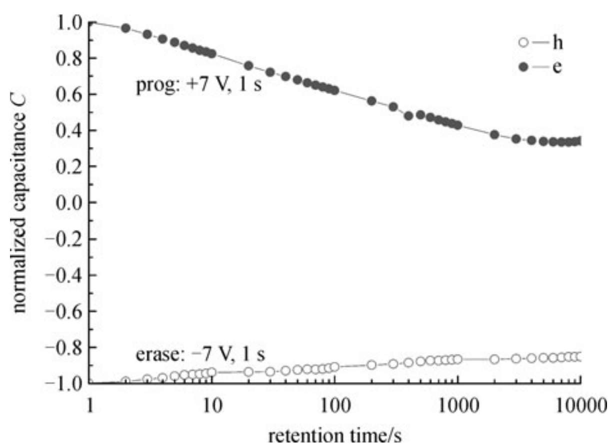


Fig. 5 *C*-*t* curve of bi-layered Si/Ge NCs based CTM

this asymmetric barriers hetero-structure could improve the CTM's programming/erasing performance while keeping a long retention time.

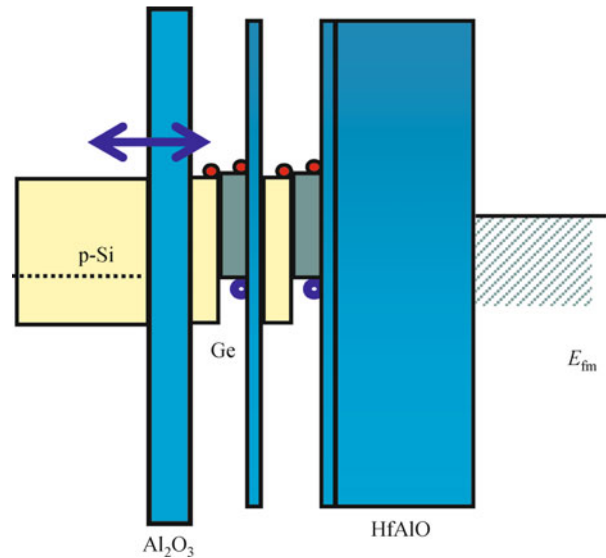


Fig. 6 Energy band diagram of bi-layered Si/Ge NCs based CTM

4 Conclusion

In summary, the multi-layered Ge/Si NCs based CTM devices have been fabricated, combining the advanced ALD and PLD techniques. High-*k* materials, Al_2O_3, HfAlO (HfO_2:Al_2O_3= 1:1) are imported as ultra thin tunnel oxide and control oxide separately. Charge storage characteristics of such CTM prototypes have been investigated with *C*-*V* and *C*-*t* measurements. The present results reveal that the holes reach a longer retention time even with an ultra thin tunnel oxide, owing to the larger valence band offset between Ge and Si. As a result, the CTM devices with optimized band gap could be expected to solve the contradiction between high-speed programming and long time retention, and the performance of memory devices would be substantially improved. Besides, multi-layered structures give a promising possibility for two-bit operation and the MLC storage.

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