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RESEARCH ARTICLE

A novel architecture of optical code label generation and recognition for optical packet switching

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Abstract A novel architecture of optical code (OC) label generation and recognition for optical packet switching (OPS) by using super structured fiber Bragg grating (SSFBG) is proposed. The OC label is generated and recognized by a label generator and recognizer, respectively. The label generator is composed of N encoders in parallel, and it can generate $2N$ kinds of serial optical code labels (SOCLs) for indicating $2N$ network routing information. The label recognizer can decode SOCLs by N decoders in parallel and provides label information to the switching control unit so that clock information is not required during the decoding process. In the switch nodes, handling of the high-speed information payload stream and the recognition of the OC label are performed in the optical domain, while processing of the routing information remains in the electrical domain. This approach could be a promising solution for an OPS network with high capacity, good quality of service (QoS), multi-service function and high security. In this experiment, we demonstrate 40 Gbps 256 label optical packet switching that employs clockless SOCL processing.

Keywords optical code (OC) label, serial optical code label (SOCL), label switching, encoder/decoder, optical packet switching (OPS)

1 Introduction

The need for greater transmission capacity through optical fibers has been met so far by the wide scale development of wavelength division multiplexing (WDM) [1]. A direction of IP into the optical layer will eventually simplify the protocol architecture to minimize the transfer delay in the core network [2]. Still, to manage and access this bandwidth the next growth challenge will most likely emerge at the switching node [3]. The eventual goal is to reduce the amount of complex electronics and the cost by migrating to the all-optical network where data is switched and routed transparently in the optical domain [4]. An optical packet switching network can have high performance and fast switching with fine granularity for future networks [5]. Photonic packet header processing for routing and switching will be needed to increase throughput and reduce latency [6]. However, the processing capability of electronic routers will eventually end up with bottlenecks due to the explosion of IP traffic [7]. Therefore, it will be imperative to explore a solution for resolving problems due to the electronic router's bottleneck [8]. Optical label switching is an effective way to realize ultrahigh speed switching because its label processing is handled optically. There are several implementations of the optical label that have been demonstrated, where sub-carrier multiplexing (SCM) [9], differential phase shift keying (DPSK) [10], and amplitude shift keying (ASK) [11] are among the technologies that have been employed. In order to detect these labels at core nodes, they usually need precise clock information for synchronization in the specially designed burst mode receiver [12]. However, a burst mode receiver requires a special design, and it is always more complex and expensive than the conventional receiver [13].

The correlation-based technique of optical code (OC) label recognition has advantages compared to the above techniques, such as not requiring clock extraction to read label information and also offering low latency [14]. This technique has already been implemented by using super structured fiber Bragg gratings (SSFBGs) or a planer lightwave circuit (PLC) [15,16]. Especially, the SSFBGs label recognizer has advantages in having a smaller size, low loss, polarization independency and a greater number of labels compared with the PLC type [17]. However, one OC label assigns only one address [18,19]. This means, for

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example, that in the case of ten thousand addresses, the OC based photonic router would require ten thousand separate correlation devices, which is not intended for practice in the future [20,21].

In this paper, to overcome the above problems, we propose a novel architecture of the OC label generator/recognizer by using SSFBG. It could increase the number of labels exponentially. In previous experiments, we demonstrated 8-bit 256 OC labels generation and recognition, and achieved the result that 40 G 256 label optical packet switching employing a clockless serial optical code label (SOCL) proceeded successfully.

The remainder of this paper is organized follows: in Sect. 2, we state the principle of optical coding based on SSFBG and present the architectures of the OC label generator and recognizer. In Sect. 3, we demonstrate the OC label switching through the experimental setup and results. In Sect. 4, we discussed the results of the experiment. Finally, concluding remarks are given in Sect. 5.

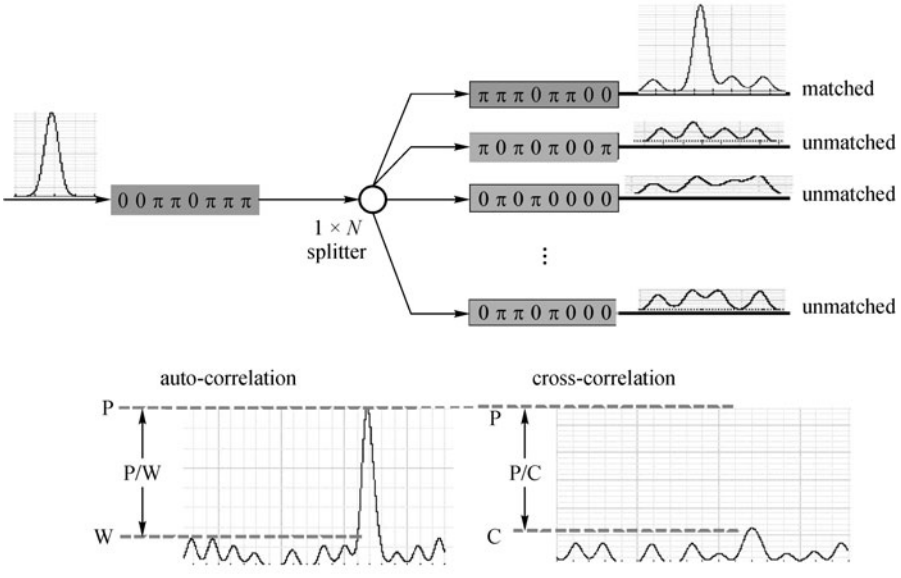
2 OC processing

The OC label can catch the information on switching which is mapped onto an OC, a sequence of time-spread optical pulses, so called chip pulses, as shown in Fig. 1. The auto-correlation emerges only where the codes match, while all the other correlations show cross-correlation outputs. The chip itself is a short pulse, and the time duration of a sequence has to be within a bit time duration. The number of OCs increases as the code length increases. The two desired properties of the code as the OC-label are: a) the peak to sidelobe ratio P/W of the auto-correlation is large; b) the auto-correlation to the cross-correlation ratio P/C is large.

The Gold code can be preferably used as the bipolar OC label. The number of codes is as much as the code length, but selection must be carefully made to satisfy the above two requirements. For example, in the case of 256-chip long Gold there are about eight codes in the class with the highest P/W and P/C.

2.1 Architecture of label generator

Figure 2 shows the architecture of the OC label generator and the process of OC label generation. The OC label generator is mainly composed of the label distributor, N encoders, a short pulse generator and an optical switch gate (OSG) array which contains N optical switch gates. All encoders are controlled by the corresponding optical switch gate in order to choose which encoder is performed. The number of encoders decides the total number of OC labels; one OC of an encoder denotes a bit 1, if an OSG is



256-chip Gold code (max 513 codes)	P/C	50					60	70		
	P/W	50	60	70	80	90	100	110	120	130
	number of codes	513	420	302	211	137	68	32	16	8

Fig. 1 Schematic of optical encoding and decoding process

closed, that let the corresponding encoder be non-coding, and the corresponding bit is 0. For example, if N encoders in parallel can generate $2N$ OC labels and the label distributor decides to allot a label (suppose $N=8$, 10101000) to a payload, it configures the optical switch array as: OSG 1, OSG 3 and OSG 5 are opened, the others are closed. The process of OC label generation is: the label distributor allots an OC label to an incoming data packet according to a protocol (for example, mapping onto IP or multiple protocol label switching (MPLS)) first; subsequently, the label distributor controls the optical switch array to choose encoders and the staruping short pulse generator that generates an ultrashort optical pulse (the pulse width is about 50 ps); by passing through the $1\times N$ optical splitter, N reproductions of the ultrashort optical pulse are encoded by corresponding encoders, and OC pulses are dispersed in the time domain due to the fiber delay line (FDL) and optical coupler. Finally, an SOCL is generated and affiliates the SOCL as a packet header to a payload that contains information for routing and switching.

2.2 Architecture of label recognizer

Figure 3 shows the architecture of the OC label recognizer and the process of OC label decoding. OC label recognition is performed by the optical correlation between an incoming OC label and the OC label entries in parallel. It is based upon optical correlation in the time domain.

In the label recognizer, the incoming SOCL consists of N kinds of different OCs divided into N signals by the $1\times N$ optical splitter, and is correlated by each OC decoder 1 to N, which corresponds to the OC encoder 1 to N, respectively. If the OC matches with a decoder, the output has a high peak, then a decision circuit can detect the peak and send out a bit 1 to the field programmable gate array (FPGA). Finally, an SOCL is decoded to N bit digital data, that is, 2^N kinds of OC labels can be distinguished and easily handled by simple logic gate devices. Note that no clock information is used during the decoding process.

3 Experiment of OC label switching

3.1 SOCL generation and recognition

To realize our proposed label processing scheme, the OC label generator and recognizer is the key component because its characteristic decides the total number of labels. We employed and fabricated eight pairs of SSFBGs as an OC label generator/recognizer, as shown in Fig. 4.

To generate the OC label, a 50 ps width optical pulse with a center wavelength of 1550 nm is shown in Fig. 4(a). The optical pulse was converted into the OC label by SSFBGs (256-chip, 40 Gchip/s, binary phase shift keying Gold codes). The center reflection wavelength of the SSFBGs was set at 1550 nm. To generate an OC label (10101010), we used encoders 1, 3, 5, and 7 to encode the optical pulse that indicated bit 1 at the OC label generator, and for the others that were not used, that indicated bit 0. Four OCs were set at different delays by the FDL and were combined into an SOCL, which is shown in Fig. 4(b). In the OC label recognizer, the inputting label signal was divided into eight label signals, and each optical label was optically correlated with the SSFBGs of the decoders. Decoders 1, 3, 5, and 7 detected the auto-correlation peak, while other decoders detected a cross-correlation waveform without a high peak, as shown in Fig. 4(c). The high optical peak was converted to bit 1 by the optical/electronic (O/E) converter, or else converted it to bit 0. The decoded SOCL, which has 8-bit parallel digital signals (10101010), is shown in Fig. 4(d).

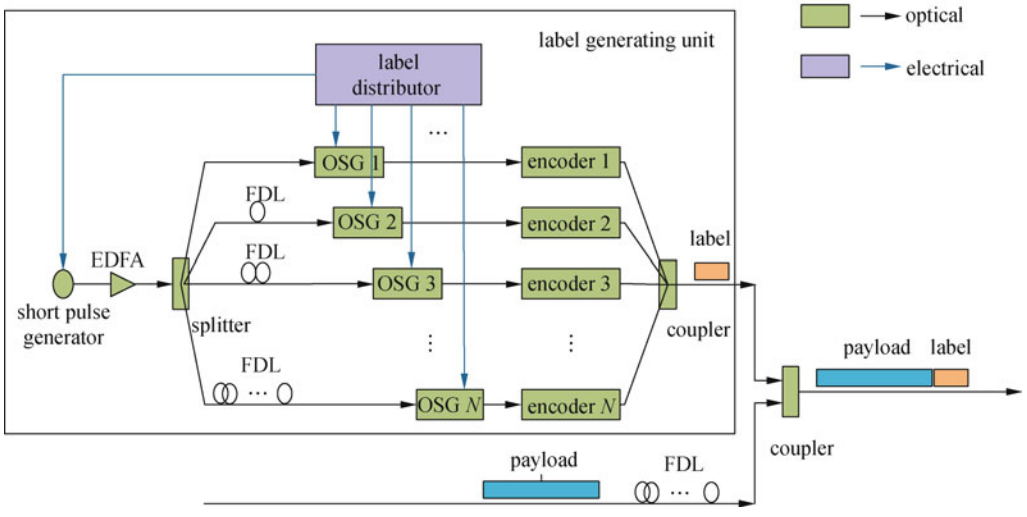


Fig. 2 Architecture of OC label generator and its encoding process (EDFA: erbium-doped fiber amplifier)

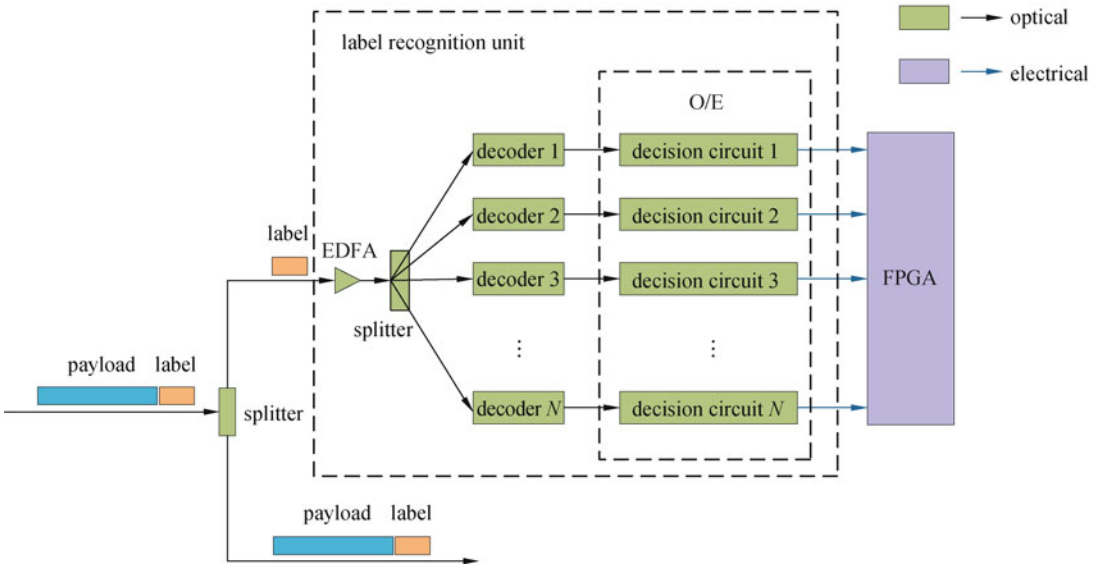


Fig. 3 Architecture of label recognizer and its decoding process (O/E: optical/electronic)

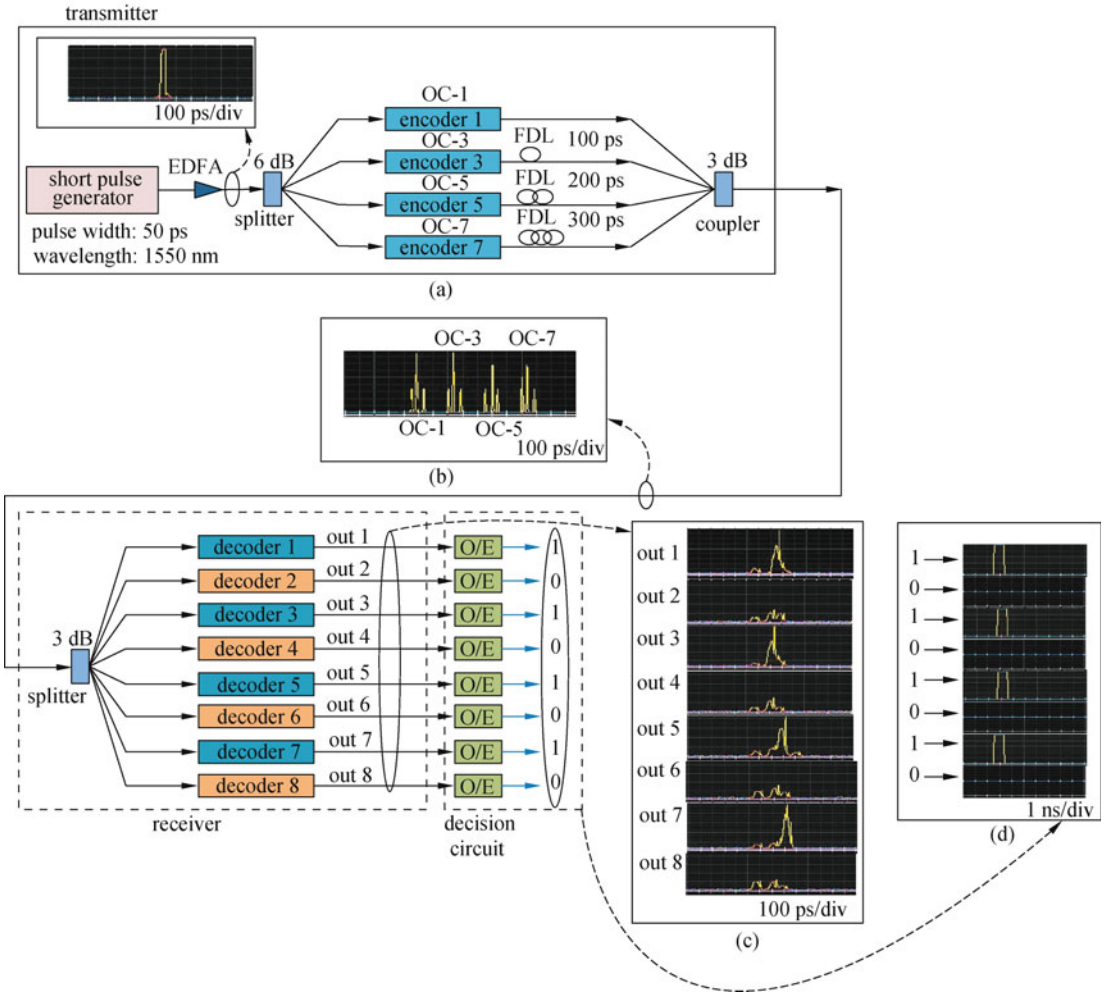


Fig. 4 Illustration of experimental setup and results. (a) Inputting ultrashort pulse; (b) SOCL encoding waveform; (c) SOCL decoding waveform; (d) outputting 8-bit parallel digital data

3.2 Packet switching based on SOCL

To demonstrate our optical packet switching based on SOCL, we made a principal experiment, described in Fig. 5. It consisted of a transmitter and the optical packet switching node. The experimental setup and results are illustrated in it.

The transmitter outputs of the optical packet consist of a payload and an SOCL. The generator generates a 50 ps width optical pulse at 1550 nm, as shown in Fig. 5(a).

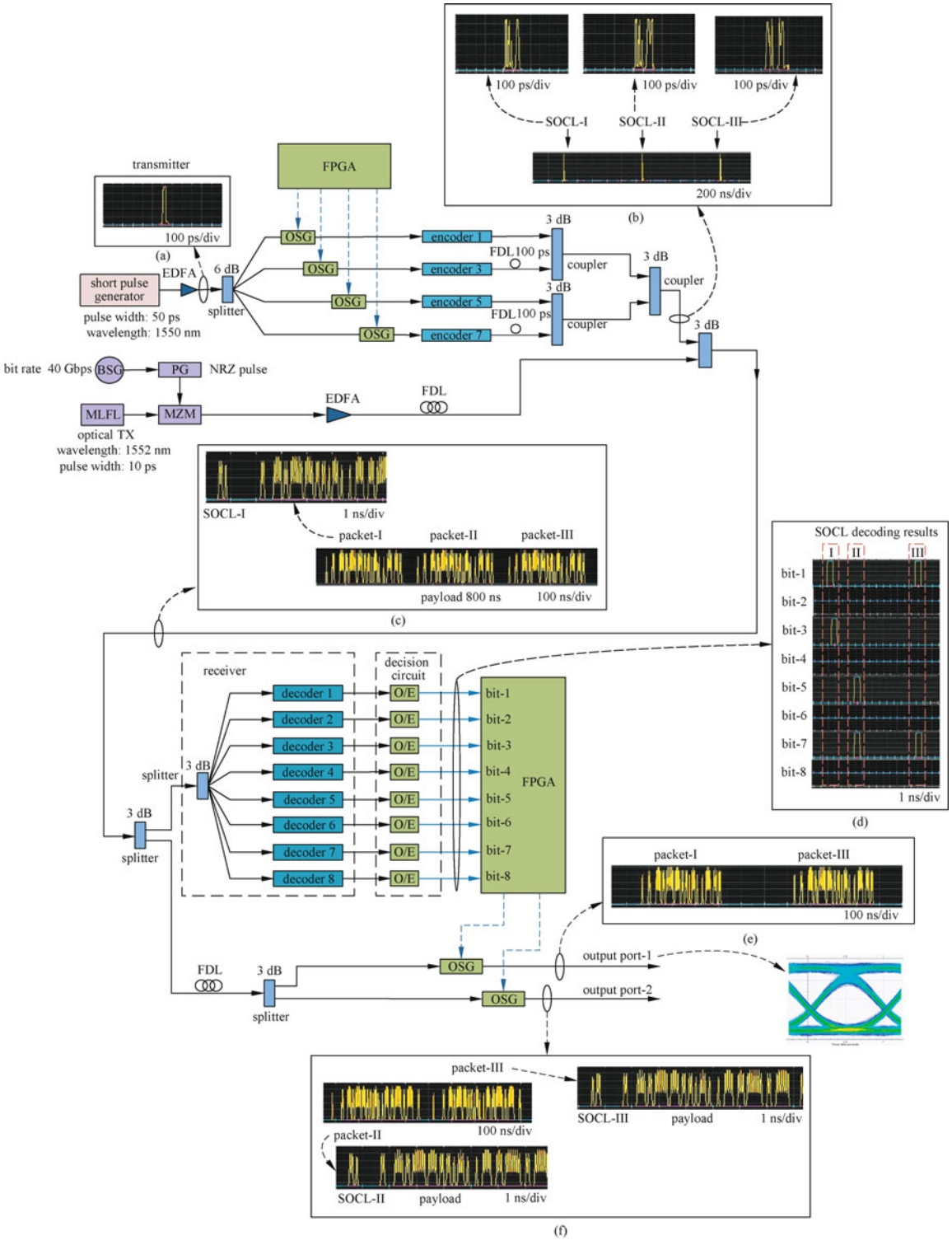


Fig. 5 Experimental setup and results. (a) Inputting ultrashort pulse; (b) SOCL encoding results; (c) inputting packets with SOCL; (d) SOCL decoding results; (e) packets switched from output port-1; (f) packets switched from output port-2

FPGA controlled four OSGs and let them open or close; to choose encoders, the pulse was converted into appointed encoders and OC labels were generated. Three kinds of 8-bit SOCL, SOCL-I (10100000) and SOCL-II (00001010) indicated unique packets, and SOCL-III (10000010) indicated multicasting.

The generation process of the payload was as follows: a 40 Gbps pseudo-random bit sequence from a bit sequence generator (BSG) entered into a pulse generator (PG) that generated a non-return-to-zero (NRZ) pulse sequence and which was modulated by mode locked fiber laser (MLFL) and Mach-Zehnder modulator (MZM), to generate the 40 Gbps payload with 10 ps pulse width. Each SOCL and payload were sets of different generating times that were controlled by FPGA: at the start, SOCL-I and packet-I were generated at the same time; 1 μs later, SOCL-II and packet-II were generated; after 2 μs, SOCL-III and packet-III were generated, and is shown in Fig. 5(b). Then we attached the optical label forward to the corresponding payload, as shown in Fig. 5(c).

In the optical packet switching node, the incoming packet was divided into two signals (one was given into eight decoders in parallel to decode, and the other was used as an optical packet for switching). The OC label recognizer decoded SOCL, that is, 8-bit parallel digital data, and inputted it to FPGA; we relate the SOCL-I to output port-1, SOCL-II to output port-2, and SOCL-III to output port-1,2. According to the 8-bit information shown in Fig. 5(d), the FPGA outputs the driving voltage that can open or close OSGs that send packet-I to output port-1, packet-II to output 2 and packet-III to output port-1,2, as is shown in Figs. 5(e) and 5(f). It is shown that the payloads were switched according to the SOCL information.

In this experimental system, the speed of label generation and recognition affects the efficiency of packet switching and transmitting. The speed of label generation is primarily decided by the reaction time of OSGs. In our experiment, the $LiNbO_3$-optical switch gate is used, whose reaction time is approximately within 10 ns so that we need about 3 m FDL for delaying incoming payloads by10 ns. In the label recognizer, the time of O/E conversion and the speed of FPGA constrain the processing of routing information and decide the length of FDL for buffering optical packets in the core node. In the experiment on optical packet switching bases on SOCL, the time of O/E conversion is about 1 ns. The dominant frequency of FPGA is up to 700 MHz; the time for processing routing information is about 20 ns, combined with the time of configuring optical switch gates, thus employing 10 m FDL for buffering optical packets which wait to be switched in the core node.

In this architecture, the high-speed payload stream is performed in an all-optical domain, and the routing information is processed in an electrical domain which enables the provision of ultra-high speed transmission for payloads and flexible and accurate performance for routing information.

4 Discussion

Although the 40 Gbps optical packet switching with the 256-OC label is demonstrated in the experiment successfully, there are still several issues that must be considered to enhance the performance of the label switching strategy, including bit error rate (BER) of label recognition, length of FDL, and the routing scheduler.

The BER of label recognition is an important issue in OC label switching because the routing information can be recovered from the OC label and it directly regulates packet switching. In the O/E decision circuit, the decision threshold for the auto-correlation pulse and cross-correlation pulse is a key matter. We adopted 256-chip long Gold SSFBG to encode the optical pulse and generated eight optical encode pulses, which generated 256 OC labels. In decoding of eight optical pulses, the P/W was up to 130 and P/C was up to 70, that is, maximum, so that the decision threshold could be set easily. We suppose that the number of OC labels for OPS be increased to increase the number of SSFBG's chips, which then ensures that the P/W and P/C be as maximal as possible. In addition, the time of O/E conversion is a key parameter, which in part decides the length of FDL. In our experiment, the time of O/E conversion is 1 ns, needing about 0.3 m of FDL.

It is well known that FDLs are massive and bulky, and 1 m of FDL introduces 3 ns of delay. In the OC label generator/recognizer, there are a great many FDLs for buffering optical packets. In order to reduce the FDL length, we must shorten the time for configuring optical switch gates. Among all, using a high-speed processor and simplifying the scheduler of routing may be effective approaches. On the other hand, an optical amplifier is needed to compensate for power loss, so we can adopt erbium-doped fiber amplifiers (EDFAs) to achieve power compensation while realizing the function of time delay.

5 Conclusion

We proposed the architecture for an OC label generator/recognizer and demonstrated clockless SOCL switching using eight pairs SSFBGs which can increase the number of packet addresses up to 256. The OC label is composed of a number of OCs which are encoded by encoders, so the number of OC labels is decided by the number of encoders; that is, N encoders can generate $2N$ OC labels, and the requirement of an OPS network address suffices. The 40 Gbps payload was accurately switched according to the SOCL information. The approach of OC label swapping can effectually provide many functions which contain broadcast, multicast, TE, quality of service (QoS), and

encryption for all optical packet switchings. In addition, no clock synchronization is required in packet switching. All these results and advantages confirm the practical feasibility of asynchronous ultrahigh speed optical packet switching.

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