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RESEARCH ARTICLE

Design and fabrication of waveguide-based chip-to-chip optical interconnection network on printed circuit boards

Zhihua YU[1,2], Fengguang LUO (✉)[1], Xu DI[1], Qing TAO[1], Weilin ZHOU[1], Bin LI[1], Liangjia ZONG[1], Guangjun WANG[2]

1 Wuhan National Laboratory for Optoelectronics, College of Optoelectronic Science and Engineering, Huazhong University of Science and Technology, Wuhan 430074, China
2 Experimental Teaching Center of Information Technology, China University of Geosciences, Wuhan 430074, China

Abstract A waveguide-based chip-to-chip optical interconnection network on printed circuit board (PCB) was designed and fabricated, and experiments confirmed that the data rate in each channel could reach above 3.125 Gbit/s and the bit error rate (BER) could be up to 1.27×10^{-18}, which would be a good solution to solve the communication bottlenecks between high-speed very large scale integration chips. Besides, the whole design and fabrication of optical interconnection network on printed circuit board has the advantages of high reliable, low cost and ease of manufacture.

Keywords optical interconnect, printed circuit board (PCB), optical waveguide (WG), bit error rate (BER)

1 Introduction

Recently, memory bandwidth and capacity requirements in distributed memory multiprocessor systems are being accelerated by multicore configurations, but the interconnection networks between processors have not been the performances of individual processors and multiprocessor computing systems. Attenuation, crosstalk and reflections in electrical signal lines become increasingly severe problems as bus and backplane speeds increase. However, the success of optical interconnects already emerged at the chip-to-chip level gives a good example for replacing electrical interconnects. According to IBM's Terabus project [1–3], a complete technology set is developed for a terabit per second optical bus for chip-to-chip interconnects on printed circuit board (PCB). The data rate per line will be up to 20 Gbit/s with 48 parallel channels, leading to an aggregate bit rate approaching 1 Tbit/s.

In this paper, we propose a waveguide-based chip-to-chip optical interconnection network on PCB and experiments confirmed that the data rate in each channel could reach above 3.125 Gbit/s and the bit error rate (BER) could be up to 1.27×10^{-18}, which would be a good solution to solve the communication bottlenecks of high-speed interchip interconnects.

2 Waveguide-based chip-to-chip optical interconnects

The architecture of interchip optical interconnects on PCB [4] includes a vertical-cavity surface-emitting laser (VCSEL) array, a PIN photodiode array, and a polymeric channel waveguide array functioning as a physical layer of optical interconnects (as shown in Fig. 1). The VCSEL is placed close to an MT-coupler with a 45° end face so that light beams from VCSEL array can be emitted into the 45° end face directly and reflected by 90°, then coupled into the waveguide layer. VCSEL and photodetector (PD) array along with their driver integrated-chip are bonded with VLSI chip by ball-grid array (BGA) technology. The VLSI chips with VCSEL and PD arrays are bonded upon PCB by surface-mount technology (SMT).

To fulfill the embedded structure, two major stumbling blocks need to be solved [5–7]. The fabrication of a low cost, high performance polymer optical waveguide layer represents the first. Next, the waveguide coupler with high coupling efficiency stands for the second. The research work presented herein will relieve the concerns for them, and is believed to be able to accelerate the deployment of the fully embedded optical interconnect architecture with further efforts.

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E-mail: fgluo@mail.hust.edu.cn

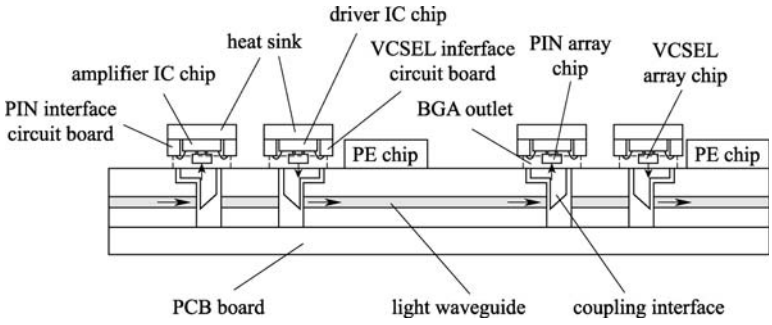

Fig. 1 Schematic diagram of waveguide-based chip-to-chip optical interconnect

3 Optical waveguide layer embedded in PCB

3.1 Fabrication of polymer optical waveguide

In order to fabricate optical waveguide layer embedded in PCB [8], SU-8 2000 photolithography is used to generate casting mould for the waveguide core layer. Electroplating is made on the surface of the SU-8 2000 photoresist mould to obtain a mechanical stability. Doctor blading technique is used to form large area formats. This method is well compatible with large area PCB production technologies. The polysiloxane materials are used to form waveguide cores and cladding layers. Waveguide cores are fabricated using doctor blading technique by filling the grooves in the SU-8 2000 photoresist mould by the core polymer material firstly. Then the core material is thermally cured under 70°C for 30 minutes. In order to fabricate sub-cladding layer and super-cladding layer of the polymer waveguide, the substrate and superstrate carriers must be made to control the thickness of the polymer waveguide cladding layers. FR4 material is used to prepare substrate carriers. The cladding polymer material is filled in the SU-8 2000 photoresist mould which the cured polymer cores still in it. After pressing the substrate carrier against the SU-8 mould and curing the polymer cladding layer comprising cores under 70°C for 30 minutes, the substrate cladding layer with polymer cores and carrier is demoulded from SU-8 2000 mould. The whole fabrication process is show in Fig. 2, and Fig. 3 gives the photograph of polymer optical waveguide array. The cross-sectional size of single waveguide is 60 μm×60 μm.

3.2 Waveguide couplers

Waveguide couplers play a key role for the realization of

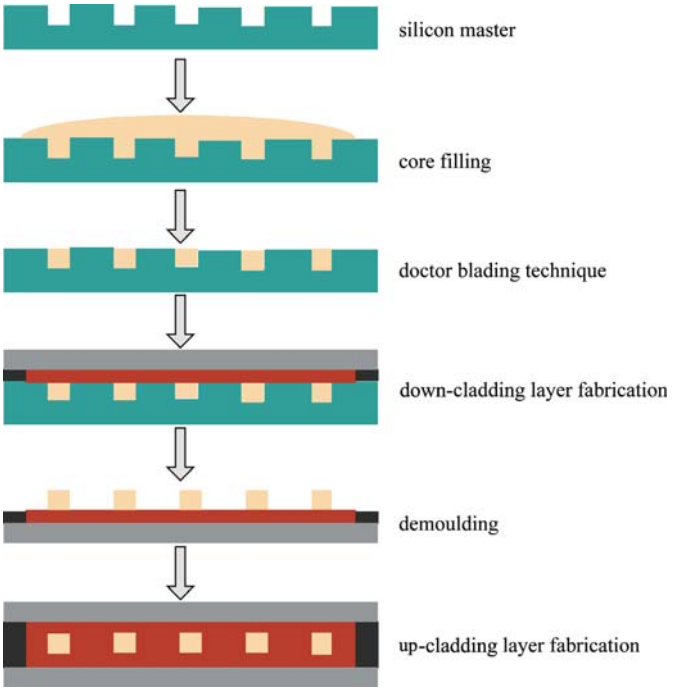

Fig. 2 Doctor blading process of polymer waveguide array

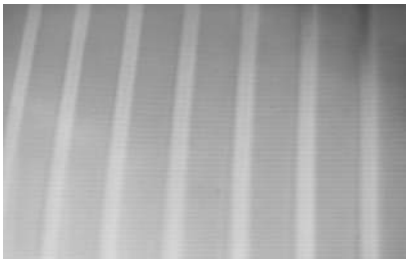

Fig. 3 Photograph of polymer waveguide array

three-dimensional fully embedded board-level optical interconnection owing to their coupling of optical signals into and out of in-plane waveguides. A waveguide grating [9] can serve as a surface normal coupler. However, the grating-based approach requires precise control of grating parameters for efficient coupling and usually has a low tolerance to wavelength variations. Therefore, the mechanically transferable (MT) coupler with 45° end face, which is based on a standard MT-PIN interface, would be a good choice (Fig. 4). At the corner of the coupler topside, there are alignment hole that mate with the mechanical alignment features on the PCB. The two MT holes to the left and right of the waveguide array provide the reference structure for the optical-electro or electro-optical element to be aligned.

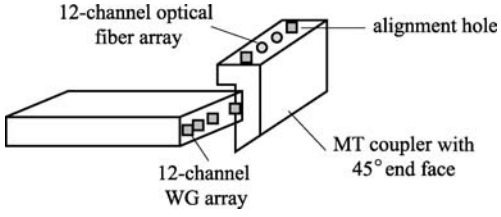

Fig. 4 Schematic diagram of MT coupler with 45° end face

3.3 Measurement of propagation losses

To observe the light propagation performance over the waveguide array and MT coupler with 45° end face, the sample tested with the configuration is shown in Fig. 5.

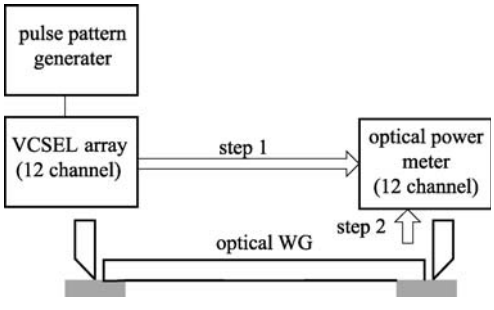

Fig. 5 Schematic diagram of measurement setup for propagation losses

Optical power meter was applied to measure the output optical power values of the VCSEL array (showed as step 1), then, by step 2 we could get the output power values of optical propagation through two MT couplers and waveguide (5-cm-length). By comparing the values of two steps, we extracted the total propagation losses of the 12 channels at 850 nm wavelength. Figure 6 gives the 12-channel optical losses via the whole propagation, from which we can see the average loss is about 2.5 dB.

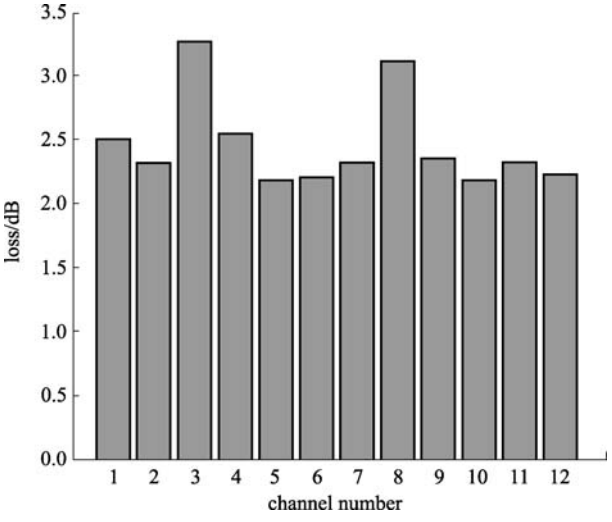

Fig. 6 Experimental results of measured propagation losses

4 Chip-to-chip optical interconnection network on PCB

Although there are many reports about all optical switch on PCB [10], which mainly adopts wavelength division multiplex (WDM) technology due to the development of long haul fiber systems, the methods are not very mature in chip-level optical interconnects. Here we have designed an optical interconnection network on PCB, using VSC3312 (Vitesse semiconductor company) as switch node. The VSC3312 has a total of 24 I/O channels and could get a low-lost, low-power asynchronous switch capable of data rates up to 6.5 Gbit/s, which would be enough to meet the current need of the rate of single central process unit (CPU) [11].

Figure 7(a) gives the schematic structure of 2×2 interconnects network for distributed-memory multiprocessor system. Each node includes a switch chip (VSC3312), optical-electronic convert module and electronic-optical convert module. VSC3312 allows flexible switch: multicast, loopback and snoop capability, so it would be a good choice of the switches in this reconfigurable mesh. The optical interconnects of switch chips are realized by VCSEL array, photodetector array and ultra-high bandwidth polymer waveguide embedded in PCB. The VCSEL converts the electrical signal from

switches into optical signal, which then propagates along the waveguide and is converted into electrical signal via a PD. The VCSELs and PDs works at 850 nm wavelength. The optical interconnect route is controlled by the control unit (CU) of C8051F310, which is a kind of single chip. Figure 7(b) is the photograph of the fabricated PCB with embedded optical waveguides, which provide sixteen I/O difference signal ports. Besides, we programmed a network router control software (see Fig. 8) with Visual Basic (VB), which could communicate with the CU, aimed for altering optical switch routers via the CU.

5 Experiments and results

Experimentally, we tested the channel performance of each node of the interconnection network up to 3.125 Gbit/s data stream (limited by the maximum rate of current signal generator in laboratory) by the interconnect control system (Fig. 8). A 3.125 Gbit/s data stream from a pseudo-random binary system (PRBS) was put into one of the sixteen I/O ports. After E/O conversion by the VCSEL, propagation of polymer waveguide and O/E conversion by the PD, the electrical output signal from the PD is then connected to a

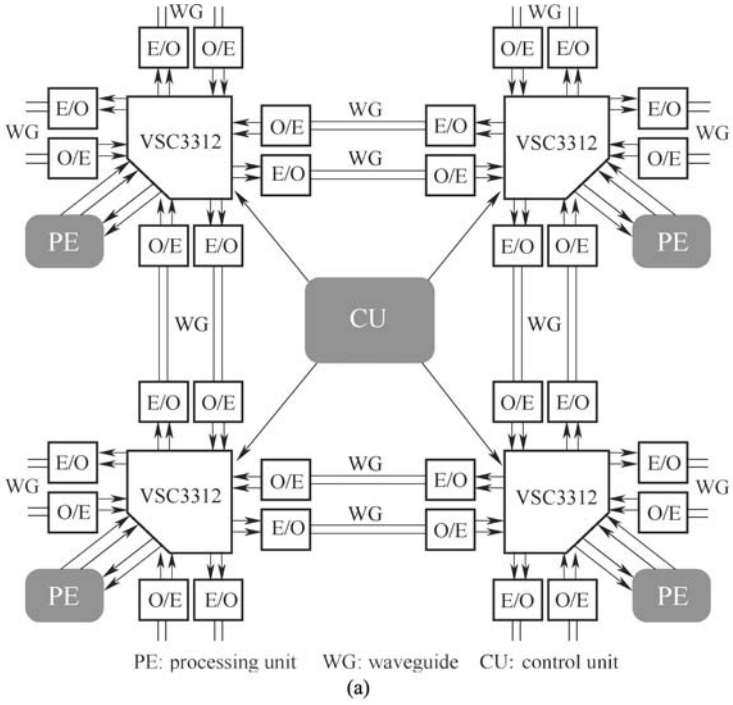

Fig. 7 2×2 mesh-based optical switch network. (a) Schematic structure of optical switch network; (b) photograph of PCB embedded with optical waveguide

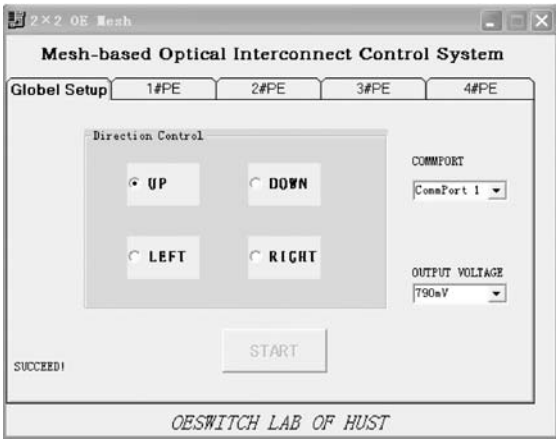

Fig. 8 Running interface of interconnection network control system

wide-band oscilloscope and a clear 3.125 Gbit/s eye pattern was observed, with Q-factor of 8.73 (Fig. 9). If we assume the presence of Gaussian distributed noises, the relation between BER and Q-factor can be expressed as

$$\mathrm{BER} = \frac{1}{2}\mathrm{erfc}\left(\frac{Q}{\sqrt{2}}\right).$$

The calculated BER is 1.27×10^{-18}.

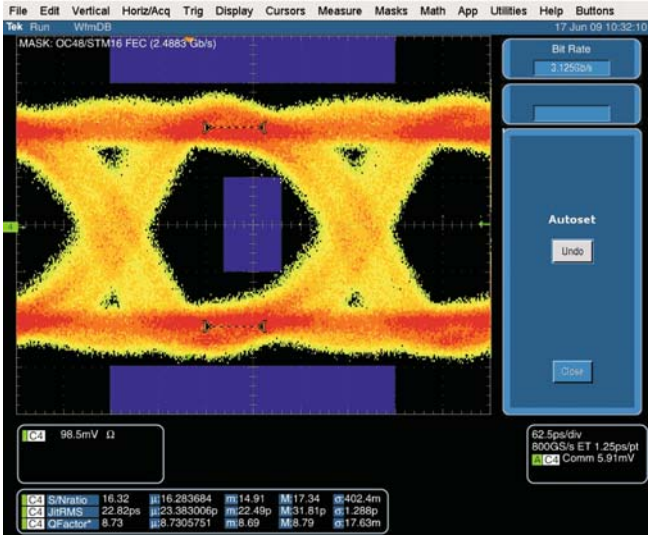

Fig. 9 Measured 3.125 Gbit/s eye diagram with Q-factor of 8.73

6 Conclusion

We successfully demonstrated a 3.125 Gbit/s optical propagation through a 2×2 optical interconnection network on PCB. And the inter-chip optical interconnects were realized by VCSELs, PDs and waveguides embedded in PCB. The data rate in each channel could reach above 3.125 Gbit/s and the BER could be up to 1.27×10^{-18}, which would be a good solution to solve the communication bottlenecks between high-speed VLSI chips.

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