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RESEARCH ARTICLE

Simple technique to fabricate microscale and nanoscale silicon waveguide devices

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Abstract Fabrication of microscale and nanoscale silicon waveguide devices requires patterning silicon, but until recently, exploitation of the technology has been restricted by the difficulty of forming ever-small features with minimum linewidth fluctuation. A technique was developed for fabricating such devices achieving vertical sidewall profile, smooth sidewall roughness of less than 10 nm, and fine features of 40 nm. Subsequently, silicon microring resonator and silicon-grating coupler were realized using this technique.

Keywords nanofabrication, silicon waveguide, roughness, microring resonator, grating coupler

1 Introduction

Silicon photonics have attracted considerable interests as a promising technology platform for low-cost solution to optical communications and interconnections [1,2]. Recently, rapid progress has been made in developing photonic building blocks in silicon, such as microring resonator, modulator, grating coupler, photonic crystals, and so on. Silicon has to be patterned in the fabrication process of these silicon waveguide devices, which, in contrast to the mature high performance techniques in wide use for relatively large scale patterning applications such as microelectromechanical system (MEMS) devices, requires smooth sidewall, vertical profile, and minimum linewidth fluctuation in nanometer dimensions. So there is a need for techniques to be developed for much smaller feature sizes as required by fabrication of the microscale and nanoscale silicon waveguide devices.

Recently, processes consisting of electron beam lithography (EBL) followed by wet and dry silicon etching have stimulated a significant amount of research [3–5]. In the work discussed here, a simple technique comprising EBL and an optimized chlorine-based inductively coupled plasma (ICP) etch process was developed, which meets the requirement of fabricating the microscale and nanoscale silicon waveguide devices with anisotropic profile and smooth sidewall morphology without any post etch process. The EBL process of the technique features the high resolution of negative tone e-beam resist hydrogen silsesquioxane (HSQ) down to decade nanometer dimensions and the great etch selectivity of silicon to HSQ under chlorine plasma. Subsequently, the optimized ICP etch process produces the silicon waveguide sidewalls with vertical profile and roughness of less than 10 nm. Lastly, realization of silicon microring resonator and silicon-grating coupler with fine features down to 40 nm are demonstrated.

2 Experiment

Silicon-on-insulator (SOI) wafers that consist of a 320-nm thick silicon top layer and a 1-μm thick buffer oxide insulator layer were used as substrates. First, negative tone e-beam resist HSQ was spin-coated on the substrates and baked under 100°C, 200°C, and 350°C, one minute each on hot plate. The exposure was done by a JEOL JBX-9300FS EBL system with 100 kV accelerating voltage. The exposure beam current was 2 nA, and doses were varied

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according to different pattern sizes and densities. Figure 1 shows the HSQ patterns in a dense structure consisting of lines and spacings with different widths after development, which demonstrates the high resolution of the e-beam resist. The insert picture of Fig. 1 is a cross-section view of the HSQ patterns in which the charge effect caused by the nonconductive e-beam resist is also displayed in the background.

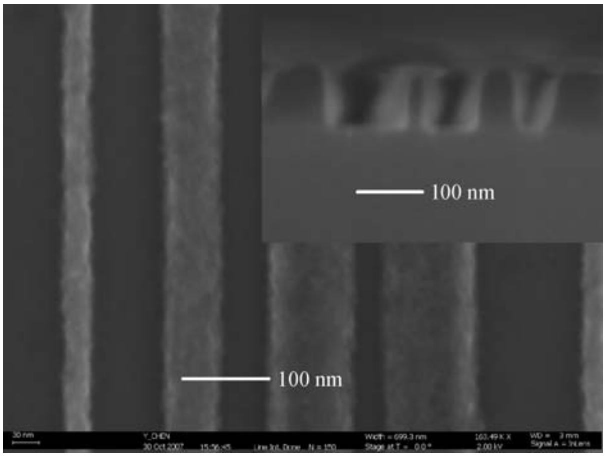

Fig. 1 Patterns of e-beam resist HSQ

The etch process for patterning silicon with micrometer and nanometer dimensions was developed using a Plasma-Therm ICP tool. Both ICP coil power and bias power, which separately control generation and direction of reactive ions, respectively, operate at radio frequency. Chlorine was the only gas used in the process, and backside helium maintained the sample temperature at 25°C. The optimized etch process was achieved with a chlorine flow rate of 50 sccm, the ICP coil power of 500 W, and the bias power of 30 W under a pressure of 5 mT. The etch rate is approximately 160 nm/min, and the resultant sidewall profile of an etched silicon waveguide is shown in Fig. 2. The insert picture in the top left corner of Fig. 2 is a top view of the edge of a silicon waveguide, indicating the less than 10-nm roughness, which demonstrates that nanometer linewidth fluctuation was achieved.

3 Results and discussion

Silicon microring resonator, leveraging off the mature SOI platform, has become a key building block for silicon photonic integrated circuits because of its versatility in function and capability of integration. It has been utilized in various applications including filtering, switching, modulation, wavelength conversion, and sensing [6–19]. The silicon microring resonator with diameter of 40 μm, 500 nm wide waveguides, and 160-nm gaps was fabricated with the technique, as shown in Fig. 3, where the insert picture demonstrates a very smooth sidewall.

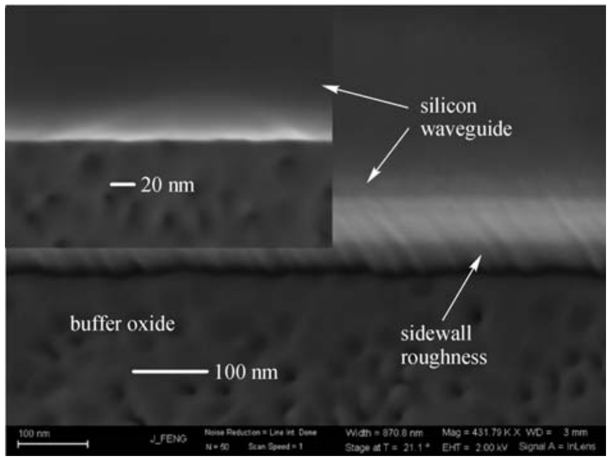

Fig. 2 Etched sidewall profile of silicon waveguide

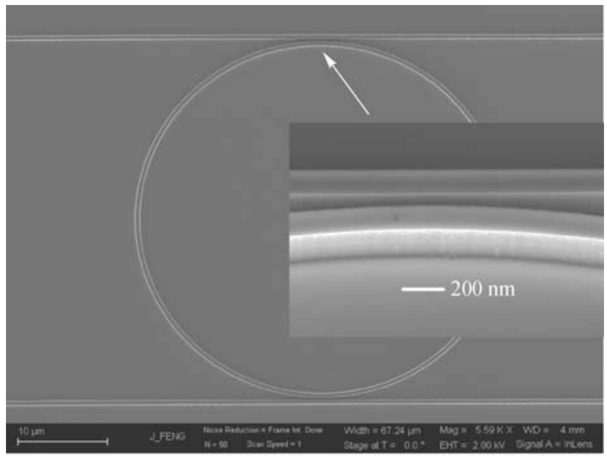

Fig. 3 Silicon microring resonator

Nanoscale silicon-grating coupler, compared with other coupling methods, is the most potential component for highly efficient compact silicon waveguide devices coupling and a fundamental device for nano-optoelectronic systems. However, few fabrication processes were reported to realize it because it requires minimum linewidth fluctuation in nanometer dimensions in a high pattern density. A nanoscale grating coupler was designed to have ridges and spacings with different widths in steep profile [20]. The structure fabricated using the above developed technique is shown in Fig. 4, indicating the smallest ridges and spacings of 40 nm in width.

It is worthy to notice that, normally, the developer for the e-beam resist HSQ in the EBL process is 2.5% tetramethyl ammonium hydroxide (TMAH), and in our process, a high-concentration developer of 25% TMAH was applied, which helps to increase the contrast of the e-beam resist while decreases its sensitivity, which is necessary for patterning nanoscale patterns in a high-density fashion, and the comparison was demonstrated in Fig. 5. The exposure dose map of the EBL process also needs to be

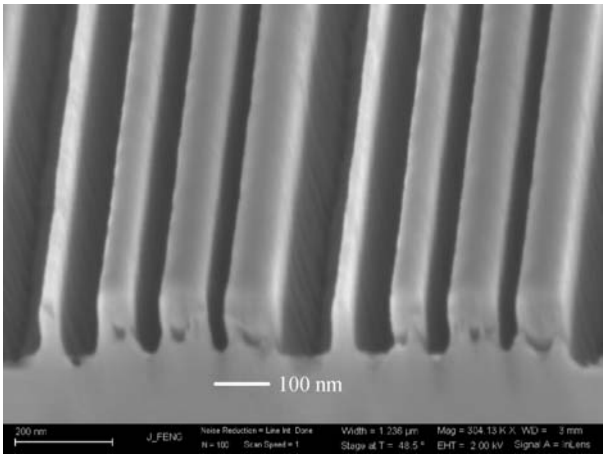

Fig. 4 Nanoscale silicon-grating coupler

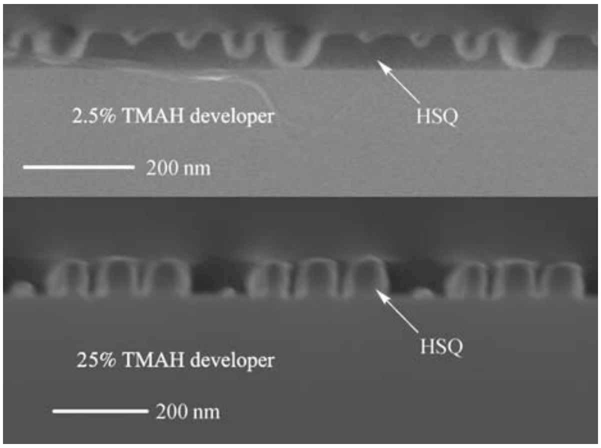

Fig. 5 Comparison results by two different developers

elaborately adjusted, in which different exposure doses are applied for different pattern widths to get equal heights of the resist and the desired sizes for the ridges and spacings. Figure 6 shows the dose map used to pattern the nanoscale silicon-grating coupler, where higher exposure doses are applied to smaller lines.

The striation roughness induced by ion bombardment during etching silicon is another issue to which much attention should be paid, as demonstrated in Fig. 7. It may cause severe scattering loss of the silicon waveguides. However, it can be greatly reduced by properly adjusting the ICP coil power and the bias power to balance the chemical absorption reaction and ion-assisted reaction [21].

4 Conclusion

A simple and effective technique has been developed to fulfill the requirements for patterning microscale and nanoscale silicon waveguide devices. Vertical sidewall

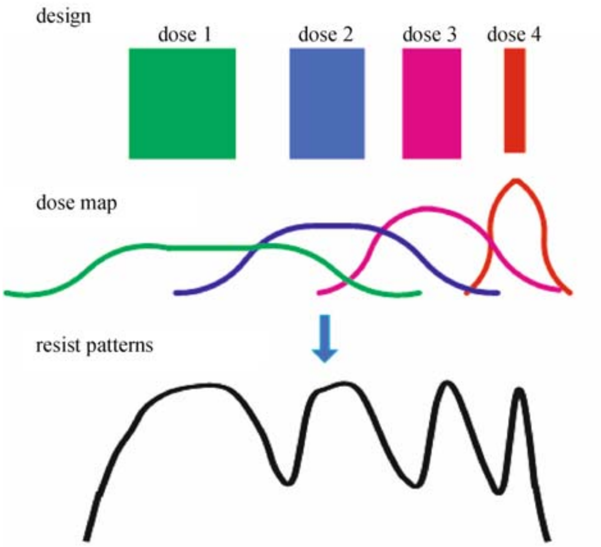

Fig. 6 Dose map for patterning silicon-grating coupler

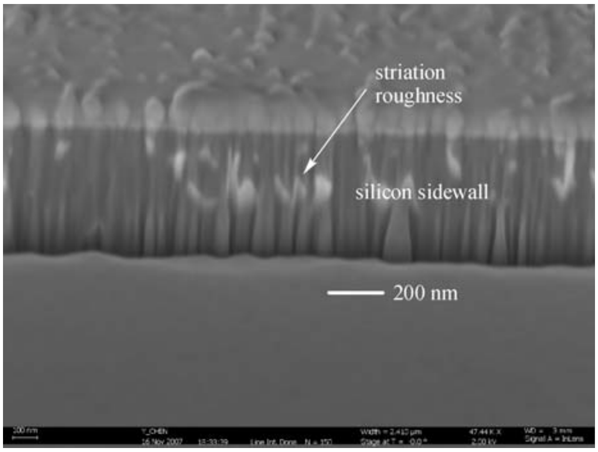

Fig. 7 Striation roughness

profile, smooth sidewall roughness of less than 10 nm and fine features of 40 nm were achieved using EBL and ICP reactive ion silicon etching without any post etch process. The process details for patterning ever-small features are discussed. Finally, the silicon microring resonator and the silicon-grating coupler were realized using the technique, which is compatible with the mature complementary metal oxide semiconductor (CMOS) technology and owns potential applications in microscale and nanoscale silicon photonics.

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