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RESEARCH ARTICLE

Monolithically integrated long wavelength photoreceiver OEIC based on InP/InGaAs HBT technology

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Abstract The epitaxial structure and growth, circuit design, fabrication process and characterization are described for the photoreceiver opto-electronic integrated circuit (OEIC) based on the InP/InGaAs HBT/PIN photodetector integration scheme. A 1.55 μm wavelength monolithically integrated photoreceiver OEIC is demonstrated with self-aligned InP/InGaAs heterojunction bipolar transistor (HBT) process. The InP/InGaAs HBT with a 2 μm × 8 μm emitter showed a DC gain of 40, a DC gain cutoff frequency of 45 GHz and a maximum frequency of oscillation of 54 GHz. The integrated InGaAs photodetector exhibited a responsivity of 0.45 A/W at $\lambda = 1.55$ μm, a dark current less than 10 nA at a bias of −5 V and a −3 dB bandwidth of 10.6 GHz. Clear and opening eye diagrams were obtained for an NRZ $2^{23}-1$ pseudorandom code at both 2.5 and 3.0 Gbit/s. The sensitivity for a bit error ratio of 10^{-9} at 2.5 Gbit/s is less than −15.2 dBm.

Keywords InP/InGaAs heterojunction bipolar transistor (HBT), PIN, photoreceiver, opto-electronic integrated circuit (OEIC)

1 Introduction

With the development of optical communication and optical interconnection towards large bandwidth and high volume, the monolithic integration photoreceiver of the PIN photodetector and the preamplifier using InP-based heterojunction bipolar transistors (HBTs) is becoming one of the focuses of optoelectronic integrated circuits. InP HBTs have great advantages in the frequency, integrating ratio, uniformity of threshold voltage, current driven capability, power dissipation and noise performance. Furthermore, the epitaxial structure and the fabrication process of the opto-electronic integrated circuit (OEIC) using the collector junction as PIN photodetector show good compatibility with InP HBT. All these push out a lot of related reports in recent years [1–4]. Up to now, the best result of the −3 dB bandwidth for integrated photoreceivers is beyond 50 GHz, and the related performance of both the sensitivity and the bandwidth for the monolithically integrated photoreceivers have been better than those for the hybrid integrated ones [1,2]. Series prototype products of InP-based HBT/PIN photoreceiver OEICs with 10 and 40 Gbit/s bit-rates have been developed by some companies such as Opto speed, Vehidium and Vitessi etc.

Research work about integrated photoreceiver OEICs with InP-based metal-semiconductor-metal (MSM) photodetector and high electron mobility transistors (HEMT) were reported in mainland China [5,6]; however, there are fewer reports in the development about HBT/PIN integrated photoreceiver OEICs. In this paper, the design and fabrication process in InP/InGaAs HBT and related HBT/PIN integrated photoreceiver OEICs in our group have been presented. Using the PIN photodetector integrated with InP/InGaAs HBT, a 1.55 μm wavelength HBT/PIN integrated photoreceiver OEIC was demonstrated with clearly opened eye diagrams under 2.5 and 3 Gbit/s transmitting rate.

2 Circuit design for photoreceiver OEIC

HBT/PIN photoreceiver OEIC consists of a p-i-n photodetector and an HBT preamplifier. The optical signal from the fiber is converted into a small current signal through the photodiode and then output as a voltage

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signal by the transimpedance preamplifier. Considering monolithic integration, the p-i-n photodetector is implemented with the base-collector junction. The circuit design starts with the selection of basic circuit topology. Using the measured DC parameters and microwave parameters of the test InP/InGaAs HBT and p-i-n photodetector, the small and large signal models of the devices to be used in the circuit simulations are characterized. The circuit topology is analyzed with advance design system (ADS) simulation tool, and the bias conditions of active devices and the value of the passive components are chosen to optimize the performance of the circuit. After the simulation is finished, the mask layout is designed according to the layout rules. Figure 1 is the schematic diagram of the HBT/PIN photoreceiver OEIC, which includes a p-i-n photodetector with a diameter of the light window of 60 μm and a three-stage InP/InGaAs HBT transimpedance amplifier with a feedback resistor $R_f = 800\ \Omega$; the emitter geometry of all the HBTs used in the design is 2 μm × 8 μm.

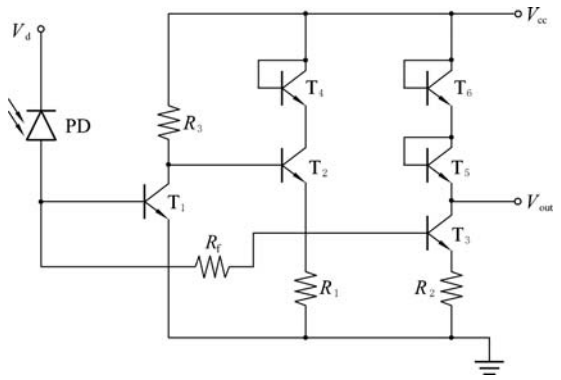

Fig. 1 Schematic of PIN/HBT photoreceiver OEIC

3 Epitaxy and fabrication process

The design of the epitaxial structure of the photoreceiver OEIC is generally based on that of InP/InGaAs HBT with the p^+-n^--n^+ InGaAs base-collector (BC) junction as p-i-n photodetector. The BC junction is optimized considering both the frequency performance of HBT and the responsivity of the p-i-n photodetector. Figure 2 is the profile structure of the photoreceiver OEIC. To improve the high-frequency performance of HBT, the collector region of light-doped InGaAs is expected to be thinner so that the transit time for the carrier through the depletion layer of BC junction decreases and the cutoff frequency, F_t, of the HBT increases. To improve the responsivity performance of the p-i-n photodetector, the collector region is expected to be thicker and the doping density to be lower so that much more absorption of optical signal at the wavelength of 1.55 and 1.31 μm is realized. As a tradeoff, the collector structure is determined as non-doped intrinsic InGaAs with a thickness of 700 nm; and other parameters of the epitaxial structure are almost the same as that of conventional InP/InGaAs HBT. Table 1 is the optimized epitaxial structure for the HBT/PIN photoreceiver OEIC on the semi-insulated InP substrate, as Fig. 2 indicates. The layer structure is grown by the V90 gas source molecular beam epitaxy (GS-MBE) system on the 2-inch Fe^+ doped semi-insulating (100) InP substrate. The dopant of the p-doped base is Be^+; and a 10-nm-thickness non-doped InGaAs is inserted in both side of the 55-nm-thickness p-type heavy doping InGaAs base region as space buffer layer to avoid the diffusion of Be^+.

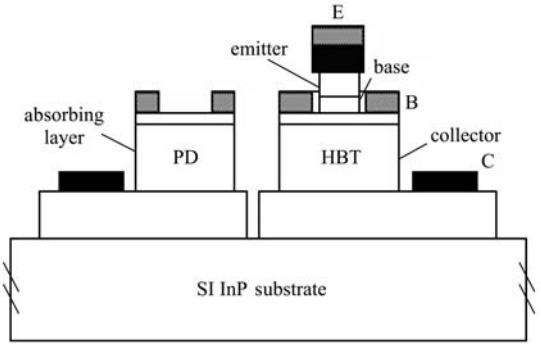

Fig. 2 Profile structure for PIN/HBT OEIC

Table 1 Epitaxial structure for PIN/HBT OEIC

layer	material	thickness/nm	doping	
			dopant	density/cm^{-3}
cap1	InGaAs	200	n^+–Si	2×10^{19}
cap2	InP	50	n^+–Si	1×10^{19}
emitter	Inp	100	n–Si	5×10^{17}
spacer	InGaAs	10	i	–
base	InGaAs	55	p^+–Be	3.5×10^{19}
spacer	InGaAs	10	i	–
collector	InGaAs	700	i	–
subcollector	InGaAs	400	n–Si	1×10^{19}

The fabricating process for HBT/PIN OEIC is almost the same as that for conventional self-aligned InP/InGaAs HBT [7]. As shown in Fig. 1, the process starts with the definition of emitter contact geometry and non-alloyed Ti/Pt/Au is deposited by electronic beam evaporation and lift-off to form the emitter contact. Then, the surface of InGaAs base is etched out with wet chemical etching solution of H_3PO_4:H_2O_2:H_2O and HCl:H_2O using the emitter contact as mask. Next, base contact is defined and Pt/Ti/Pt/Au is evaporated, lift-off and annealing to be self-aligned emitter ohmic contact. BC mesa is formed after the InGaAs sub-collector surface is etched out. The

following evaporation of Ti/Pt/Au forms the collector ohmic contact by lift-off. During the above process, the mesa and p^+, n^+ ohmic contacts of the photodetector are formed with the BC mesa and the base, collector contacts simultaneously. SiO_2 layer is used as the passivation for active devices, the isolation between interconnecting metals and the anti-reflecting film of the photodetector. The thin-film NiCr resistors with a sheet resistance of 50 Ω/□ are formed by the sputtering system. The via holes for the ohmic contacts of HBTs and the photodetector are opened by reactive ion etching (RIE) process and Au with a thickness of 2 μm is electro-plated and forms the interconnecting metal to end the process. Figure 3(a) is the self-aligned emitter structure of HBT; Fig. 3(b) is a SEM photograph of the integrated photodetector. Figure 4 is the photograph of the fabricated PIN/HBT photoreceiver OEIC, and the circular area in the left of the picture is the integrated p-i-n photodetector.

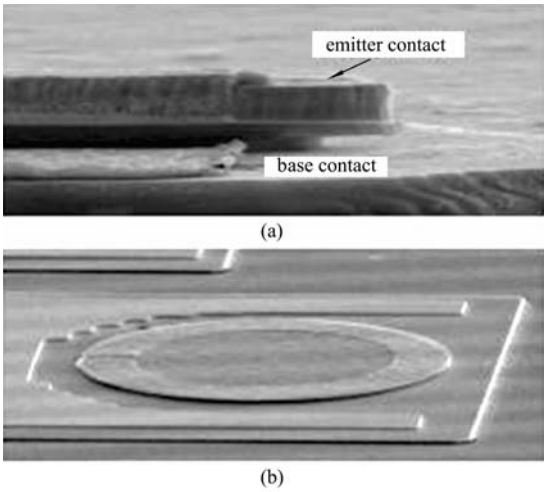

Fig. 3 SEM Photograph of device structure. (a) Self-aligned emitter structure of HBT; (b) integrated photodetector

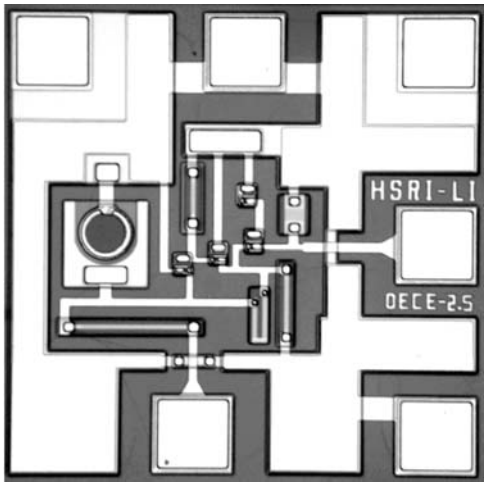

Fig. 4 Photograph of PIN/HBT photoreceiver OEIC

4 Characteristics of HBT, integrated photodetector and photoreceiver OEIC

4.1 InP/InGaAs HBT

DC and microwave parameters for InP/InGaAs HBTs with 2 μm × 8 μm emitter were characterized using Keithely 4200 semiconductor parameter analyzer and HP 8510C network analyzer. A DC current gain of about 40, a threshold voltage of 0.6 V and a breakdown voltage (V_{ceo}) of 3 V, and ideality factors of 1.12 and 1.43 for the collector and base current, respectively, were obtained from the measured *I–V* DC characteristic plot and the Gummel plot. DC current gain H21 and Mason's unilateral gain GU were calculated from the measured S parameters. Figure 5 shows the gains of HBT with the size of emitter of 2 μm × 8 μm versus the frequency under $I_c = 10$ mA and $V_{ce} = 1.5$ V. The DC gain cutoff frequency F_t and the maximum oscillation frequency F_{max} were extrapolated as 45 and 54 GHz.

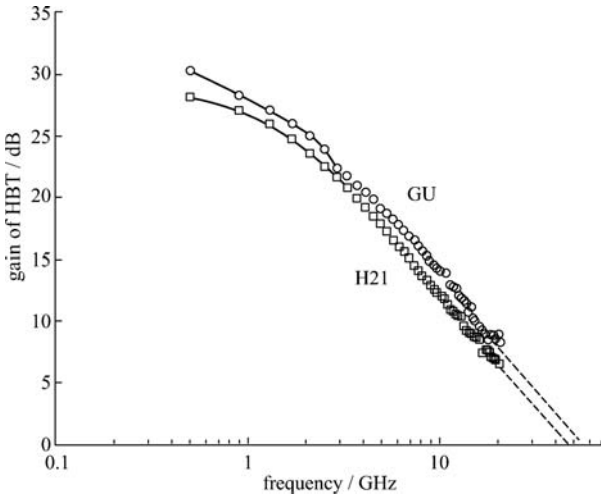

Fig. 5 Gain versus frequency of InP/InGaAs HBT

4.2 Integrated InGaAs p-i-n photodetector

Different from the discrete InGaAs photodetector, the thickness of the absorbing layer of the integrated InGaAs p-i-n photodetector, i.e., the collector of HBT, is only 700 nm for trade-off between the response speed and the responsivity of the photodetector and the high-frequency performance of the HBT. The responsivity of the integrated photodetector is usually lower for its InGaAs homojunction structure lack of p-type wide bandgap InP as the window layer. To improve the responsivity performance, the dielectric layer in the HBT process for passivation is optimized and SiO_2 with a thickness of 760 nm is employed to act as an anti-reflecting layer for the photodetector.

The responsivity and the dark current of the integrated InGaAs photodetector were measured on a wafer with a 1.55 μm wavelength laser diode, AI9402A optical power meter and a Keithley 6485 Picoammeter. The results show that the responsivity is 0.45 A/W, the dark current is lower than 10 nA at a bias voltage of −5 V. The small signal gain-frequency characteristics of the integrated photodetector at −3 V bias was characterized on a wafer with a light wave component analyzer. Figure 6 presents the small-signal gain-frequency characteristics of the integrated photodetector with a light window of 60 μm, which shows that the −3 dB bandwidth reaches 10.6 GHz.

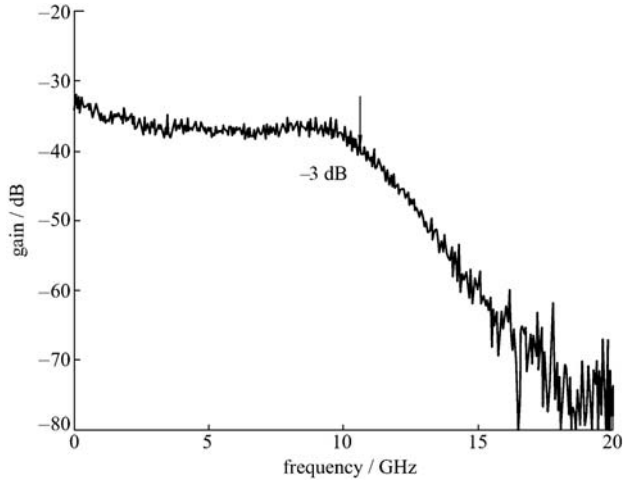

Fig. 6 Small-signal gain-frequency characteristics of integrated photodetector

4.3 HBT/PIN photoreceiver OEIC

The data transmission performance and the sensitivity of the HBT/PIN photoreceiver OEIC are measured by coupling an input tapered fiber to the OEIC mounted on a test carrier using a micro optical bench. The test system consists of Advantest 3186 pattern generator, Advantest 3286 Error Detector, Tektronix CAS8000ex Communication Signal Analyzer, a high-speed optical transmitter at the wavelength of 1550 nm and a variable optical attenuator. The measurement starts by adjusting the high-speed transmitter till the output eye diagram satisfies the demand of the standard OC-48/STM-4; and then the receiver OEIC is measured by observing the eye diagram and the BER performance. Figures 7(a) and 7(b) show the output eye diagram of the OEIC for a NRZ 2^{23}–1 pseudorandom code at both 2.5 Gb/s and 3.0 Gb/s, respectively. The eye diagrams at 2.5 and 3 Gb/s bit rates are open and clear enough to satisfy the demand of OC-48. The sensitivity measurement demonstrates that the sensitivity of HBT/PIN photoreceiver OEIC is less than −15.2 dBm at a bit error ratio of BER = 10^{-9}.

5 Conclusion

We have described the epitaxial structure and growth, circuit design, fabrication process and characterization of the integrated photoreceiver with InP/InGaAs HBT and p-i-n photodetector. The InP/InGaAs HBT with a 2 μm × 8 μm emitter contact showed a DC gain of 40, a DC gain cutoff frequency of 45 GHz and a maximum frequency of oscillation of 54 GHz. The integrated InGaAs photodetector exhibited a responsivity of 0.45 A/W at $\lambda = 1.55$ μm, a dark current less than 10 nA at a bias of −5 V. Clear and opening eye diagrams were obtained for an NRZ 2^{23}–1 pseudorandom code at both 2.5 and 3.0 Gb/s. The sensitivity for a bit error ratio of BER = 10^{-9} at 2.5 Gb/s is less than −15.2 dBm. This is the first report for monolithically integrated photoreceiver realized in the approach of HBT/PIN integration in mainland China.

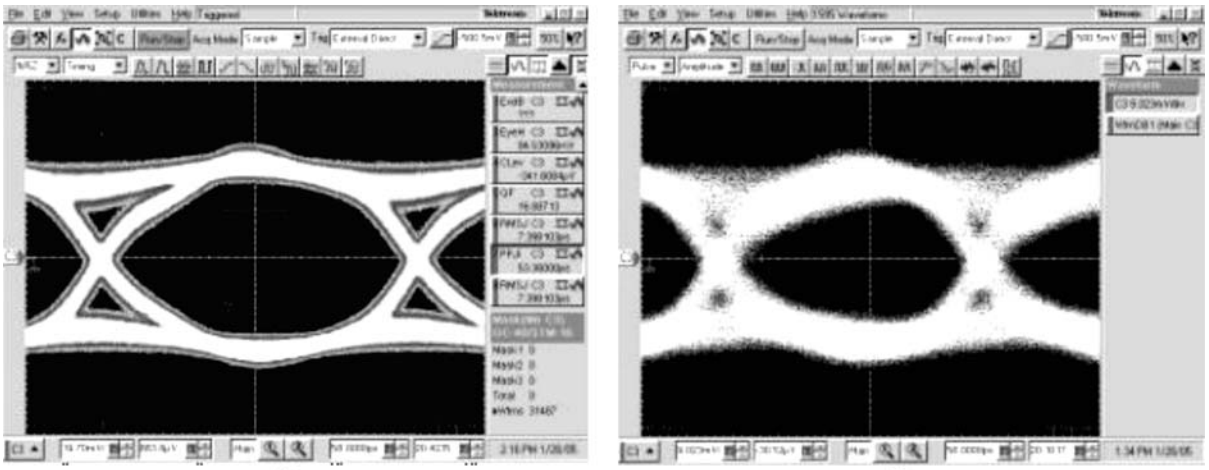

Fig. 7 Optical eye-pattern. (a) NRZ 2^{23}–1 pseudorandom code at 2.5 Gb/s; (b) NRZ 2^{23}–1 pseudorandom code at 3.0 Gb/s

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