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# Low-power, high-speed, and area-efficient sequential circuits by quantum-dot cellular automata: T-latch and counter study

**Key words:** Quantum-dot cellular automata (QCA); Quantum-dot; T-latch; T-flip-flop; Counter; Selective counter; QCADesigner; QCAPro

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# Motivation

1. Quantum-dot cellular automata (QCA) is a new nanotechnology for the implementation of nano-sized digital circuits.
2. This nanotechnology is remarkable in terms of speed, area, and power consumption compared to complementary metal-oxide-semiconductor (CMOS) technology and can significantly improve the design of various logic circuits.
3. Latches and counters are blocks which used mainly in arithmetic logic unit (ALU). Therefore, designing these circuits in QCA technology is of high importance.

# Main idea

1. We propose a new method for implementing a T-latch in QCA technology.
2. The proposed method uses the intrinsic features of QCA in timing and clock phases, and therefore, the proposed cell structure is less occupied and less power-consuming than existing implementation methods.
3. Also, new T-latch with set/reset terminals is proposed.
4. In addition, new counters are designed in QCA nanotechnology.

# Method

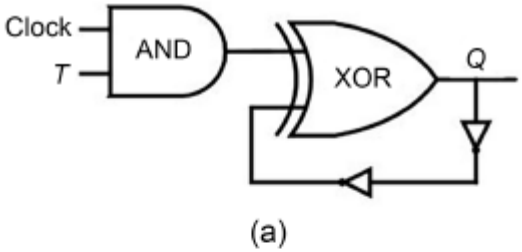
1. We propose a new method for implementing a T-latch in QCA technology.
2. The proposed method uses the intrinsic features of QCA in timing and clock phases, and therefore, the proposed cell structure is less occupied and less power-consuming than existing implementation methods.
3. In the proposed T-latch, compared to previous best designs, reductions of 6.45% in area occupation and 44.49% in power consumption were achieved.

# Method (Cont'd)

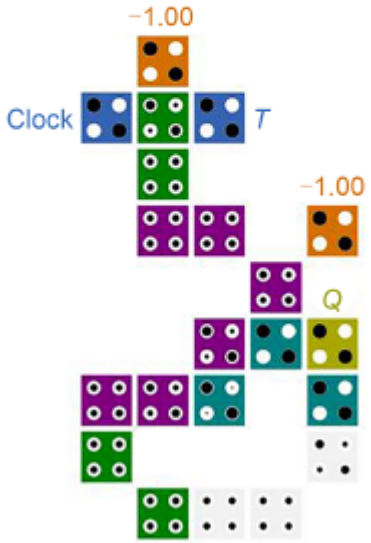
4. A reset-based T-latch and a T-latch with set and reset capabilities are also designed.
5. Using the proposed T-latch, a new 3-bit counter is developed which reduces 2.14% of cell numbers compared with the best of previous designs.
6. Moreover, based on the 3-bit counter, a 4-bit counter is designed, which reduces 0.51% cell numbers and 4.16% cross-section area compared to previous designs.
7. In addition, two selective counters are introduced to count from 0 to 5 and from 2 to 5.

# Major results

## The proposed T-latch

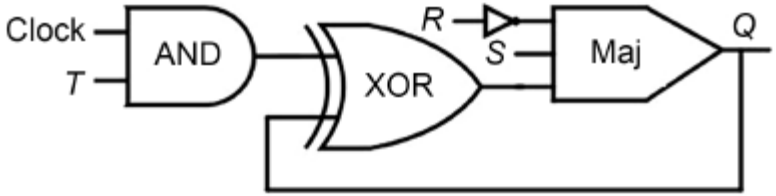



(a)

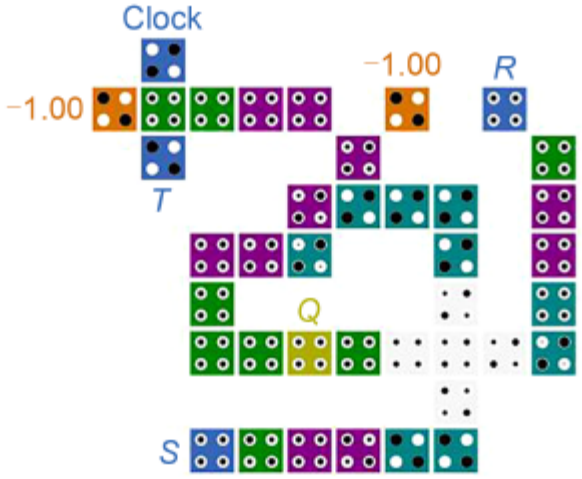



(b)

## The proposed T-latch with set and reset



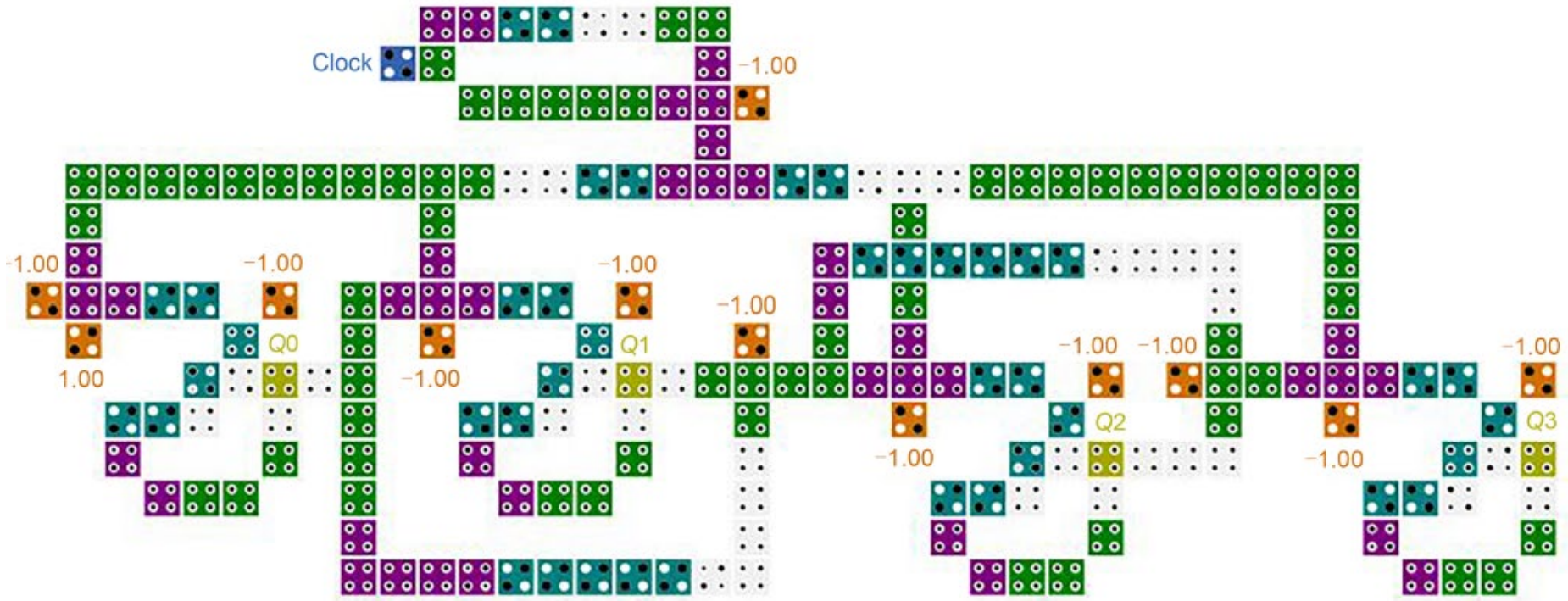

(a)




(b)

# Major results (Cont'd)

**The proposed 4-bit counter**



# Major results (Cont'd)

**Table 3 Comparison of the proposed designs and others**

| Reference | Cell number | Area ($\mu m^2$) | Latency ($\times 10^{-12}$ s) | Total energy dissipation at 0.5Ek (meV) | Cost | New Cost | Set input | Reset input |
|---|---|---|---|---|---|---|---|---|
| Bhavani and Alinvinisha (2015) | 67 | 0.08 | 1.25 | – | – | – | No | No |
| Torabi (2011) | 66 | 0.06 | 1.25 | 88.72 | – | – | No | No |
| Dutta and Mukhopadhyay (2014) | 58 | 0.06 | 1.25 | – | 7.5 | – | No | No |
| Angizi et al. (2014) | 55 | 0.06 | 1.5 | 55.46 | – | – | No | No |
| Angizi et al. (2015) | 46 | 0.06 | 1 | 31.36 | 4.5 | 8.46 | No | No |
| Rad and Heikalabad (2017) | 23 | 0.03 | 0.5 | 30.87 | 3.75 | 3.47 | No | No |
| Majeed et al. (2019) | 21 | 0.0186 | 0.75 | 29.22 | 2.25 | 1.22 | No | No |
| Fig. 3b | 21 | 0.0174 | 0.75 | 16.22 | 3.75 | 1.05 | No | No |
| Fig. 5b | 33 | 0.03 | 1.25 | 19.01 | 5 | 2.85 | No | Yes |
| Fig. 6b | 39 | 0.035 | 1.25 | 22.66 | 5 | 3.96 | Yes | Yes |

# Conclusions

1. In this research, we have discussed the principles of quantum cell design. Also, simple and useful designs of T-latches, T-latches with reset input, and T-latches with set and reset inputs have been presented.
2. In addition, a level-to-edge converter has been used for clock of T-latches which leads to TFF topologies.
3. We have also designed, with the help of the suggested flip-flops, a 3-bit counter, a 4-bit counter, a 0–5 selective counter, and a 2–5 intermediate selective counter.

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