Yang LIU, Jie LI, Han WANG, Debiao ZHANG, Kaiqiang FENG, Jinqiang LI, 2021. A BCH error correction scheme applied to FPGA with embedded memory. *Frontiers of Information Technology & Electronic Engineering*, 22(8):1127-1139. https://doi.org/10.1631/FITEE.2000323

A BCH error correction scheme applied to FPGA with embedded memory

Key words: Error correction algorithm; Bose–Chaudhuri–Hocquenghem (BCH) code; Field programmable gate array (FPGA); NAND flash

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Motivation

1. Given the potential for bit flipping of data on a memory medium, it is crucial to adopt an error correction algorithm with strong error-correction capabilities to guarantee data accuracy and system reliability.

2. For field programmable gate array (FPGA) based storage systems, it is necessary to effectively adopt the limited resources of FPGA, so the complexity of the error correction algorithm must be strictly limited.

Main idea

1. A high-speed parallel Bose–Chaudhuri–Hocquenghem (BCH) error correction scheme with modular characteristics, combining logic implementation and a look-up table, is proposed.

2. It is suitable for data error correction on a modern FPGA full with on-chip embedded memories.

3. We elaborate on the optimization method for each part of the system and analyze the realization process of this scheme.

Method

1. In the error detection module, resource sharing and time multiplexing technologies are employed to reduce the chip area.

2. A direct tree-decision architecture is proposed for calculating the error-locator polynomial.

3. We propose to pre-calculate the two representations of the elements in the Galois field (GF) (vector form and power form of the primitive element). Then they are stored as the look-up table in the embedded memory on the FPGA, so that the polynomial multiplication and division described by the complex combinatorial logic are converted into simple power-sum operations.

Major results

1. A direct and clear iterative path

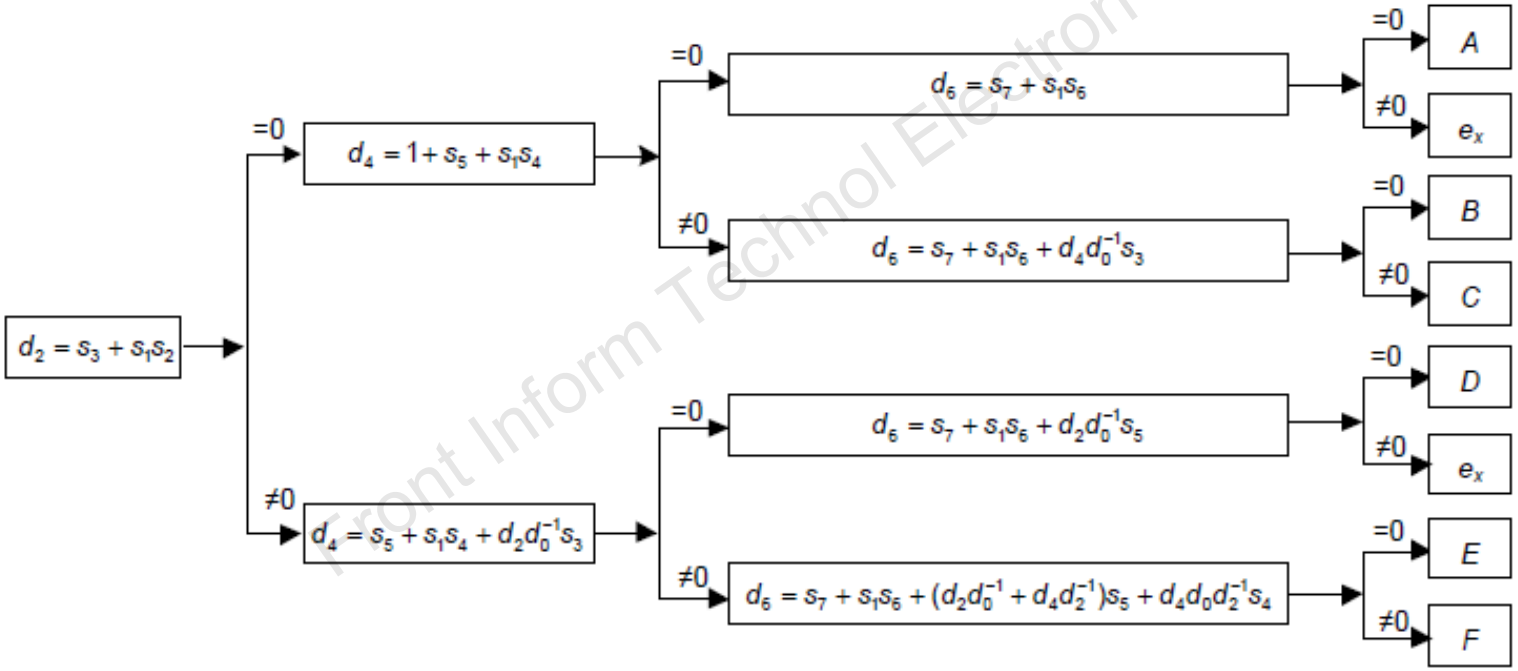

Fig. 7 A straightforward tree-decision architecture for t=4

Major results (Cont'd)

2. The early termination method and the root distance reduction method are used to speed up the decoding process.

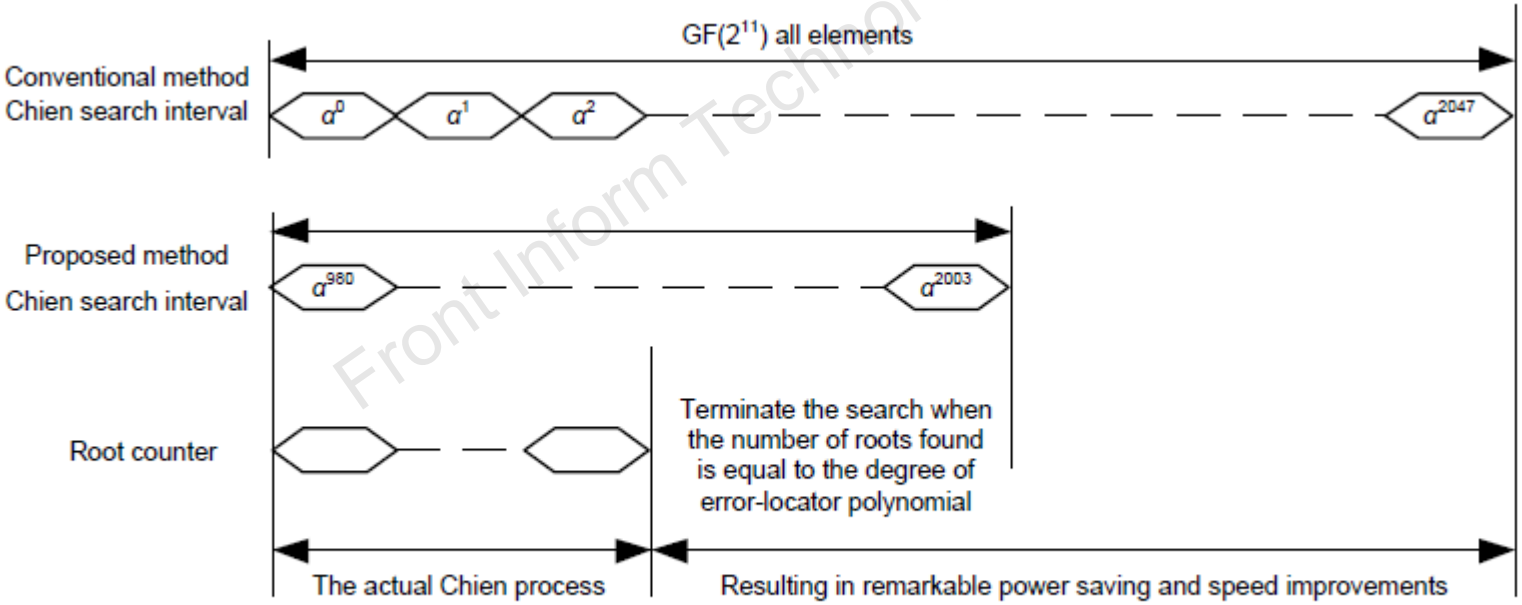

Fig. 9 Early termination method and root distance reduction method

Major results (Cont'd)

3. Performance comparison of the five syndrome calculation methods

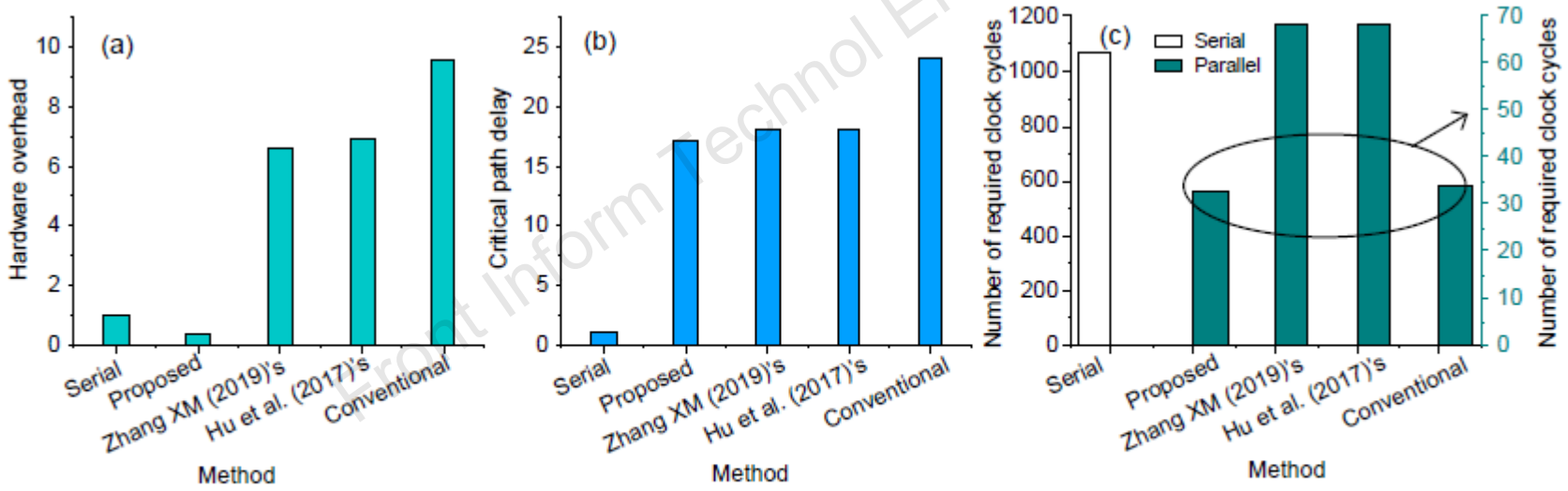

Fig. 12 Performance comparison of the five syndrome calculation methods: (a) hardware overhead; (b) critical path delay; (c) number of required clock cycles

Major results (Cont'd)

4. The final error-locator polynomial corresponding to each path

Table 2 Final error-locator polynomial and the number of errors

Symbol	$\sigma^{(7)}(x)/\sigma^{(8)}(x)$	Number of errors
A	$1+s_1x$	1
B	$1+s_1x+d_4d_0^{-1}x^4$	4
C	$1+s_1x+d_6d_4^{-1}x^2+d_6d_4^{-1}s_1x^3+d_4d_0^{-1}x^4$	4
D	$1+s_1x+d_2d_0^{-1}x^2$	2
E	$1+s_1x+(d_2d_0^{-1}+d_4d_2^{-1})x^2++d_4d_2^{-1}d_0x^4$	3
F	$1+s_1x+(d_2d_0^{-1}+d_4d_2^{-1}+d_6d_4^{-1})x^2$ $+(d_4d_2^{-1}d_0+d_6d_4^{-1}s_1)x^3+d_6d_4^{-1}d_2d_0^{-1}x^4$	4

Conclusions

1. A time multiplexing technology is used in the error detection module to reduce the hardware overhead by more than 95%.

2. In determining the error-locator polynomial module, a direct and clear iterative path is planned. This reduces the complexity of the algorithm.

3. The polynomial multiplication and division described by the complex combinatorial logic are converted into simple power-sum operations, so that the path delay is reduced by 61.5%.

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