Chengcheng CHEN, Yuhao ZHOU, Juncai HE, Dongge QIN, Zhanhui SHI, Wei ZHANG, Jicong DUAN, Zhenxue HE, Limin XIAO, 2026. Multiobjective optimization for mixed polarity Reed–Muller logic circuits based on a multi-strategy quantum wolf pack algorithm. *ENGINEERING Information Technology & Electronic Engineering*, 27(10):260146. https://doi.org/10.1631/ENG.ITEE.2026.0146

Multiobjective optimization for mixed polarity Reed–Muller logic circuits based on a multi-strategy quantum wolf pack algorithm

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Key words: Cooperative optimization; Mixed polarity Reed–Muller; Quantum wolf pack algorithm; Pareto non-dominated sets

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Motivation

- Targeting the limitations of existing mixed polarity Reed–Muller (MPRM) circuit optimization methods, which suffer from long runtime, limited scalability to large-scale circuits, and difficulty in obtaining high-quality Pareto optimal solutions for simultaneous area and power optimization, a multi-strategy quantum wolf pack algorithm (MQWPA) is proposed to efficiently search for the ternary polarity space and achieve effective cooperative optimization.

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Main idea

- An MQWPA is proposed, which follows a simplicity- and efficiency-oriented philosophy to improve search efficiency and diversity in a large-scale MPRM polarity space.
- A ternary quantum encoding and rotation-based updating mechanism is proposed, which matches the three-valued MPRM polarity representation and enables efficient exploration of discrete polarity configurations.
- An efficient area and power optimization approach (EAPOA) is proposed based on MQWPA, which searches for high quality Pareto non-dominated solutions of XNOR/OR-based circuits.

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Method

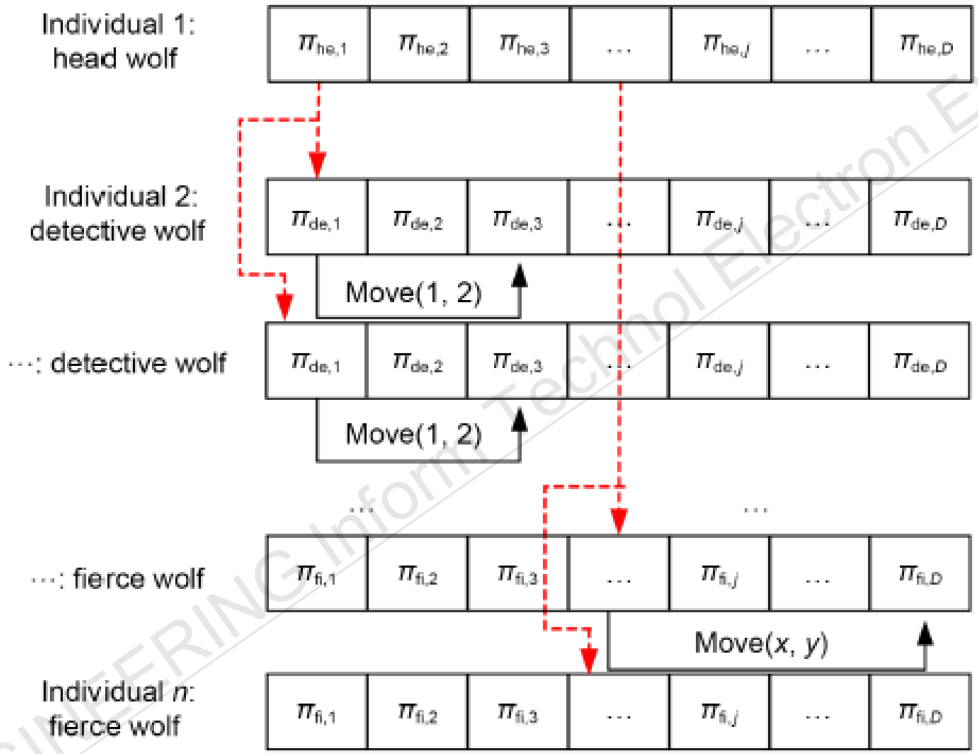


Fig. 2 Overview of the mutation strategy

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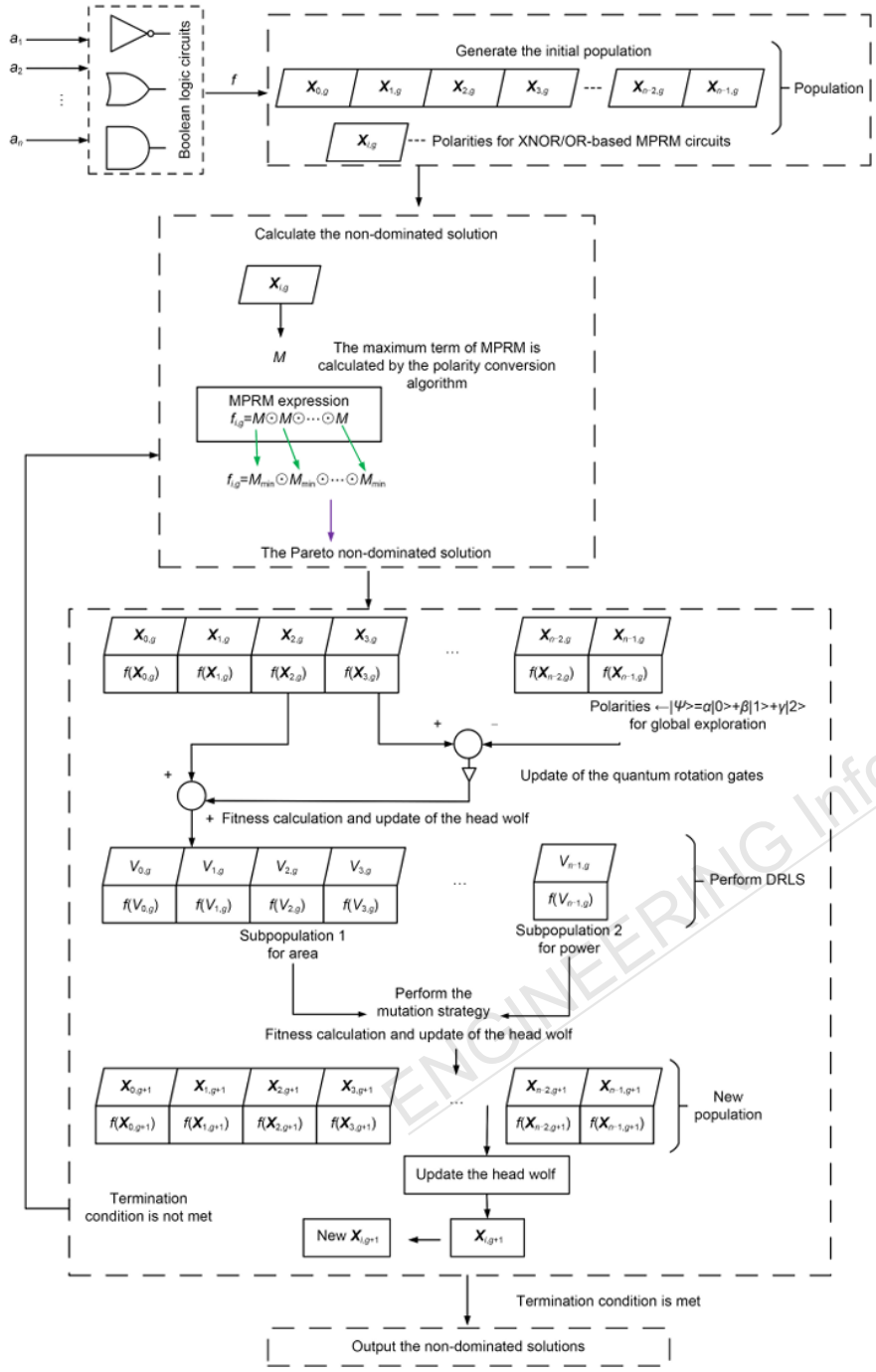


Fig. 5 Overview of the EAPOA

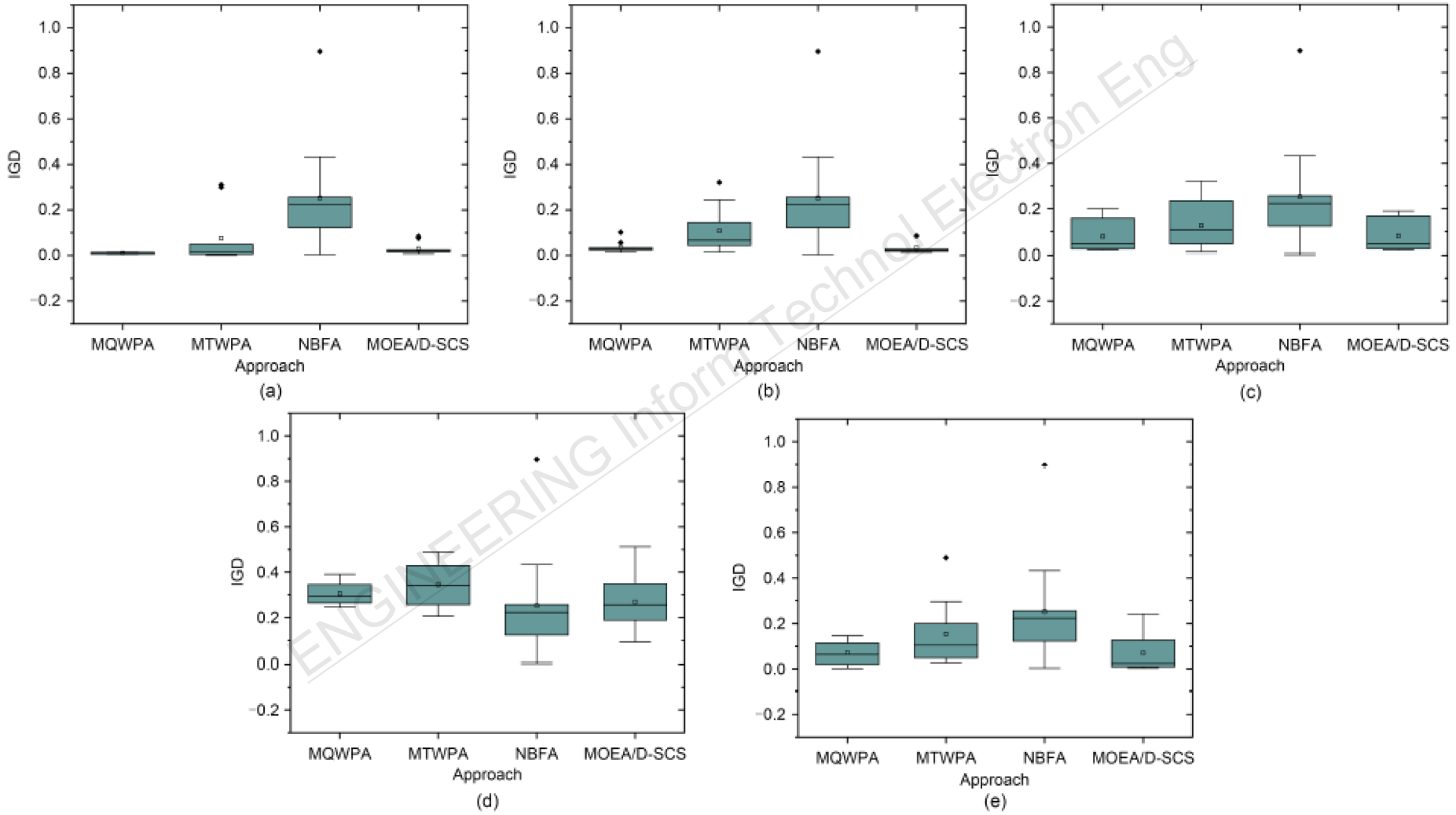
Method

The selection rule for Δ is

$$\begin{cases} \text{If } s=0, b=1 \rightarrow \boldsymbol{U}_{0,1}(+\Delta), \\ \text{If } s=1, b=0 \rightarrow \boldsymbol{U}_{0,1}(-\Delta), \\ \text{If } s=0, b=2 \rightarrow \boldsymbol{U}_{0,2}(+\Delta), \\ \text{If } s=2, b=0 \rightarrow \boldsymbol{U}_{0,2}(-\Delta), \\ \text{If } s=1, b=2 \rightarrow \boldsymbol{U}_{0,3}(+\Delta), \\ \text{If } s=2, b=1 \rightarrow \boldsymbol{U}_{0,3}(-\Delta), \end{cases}$$

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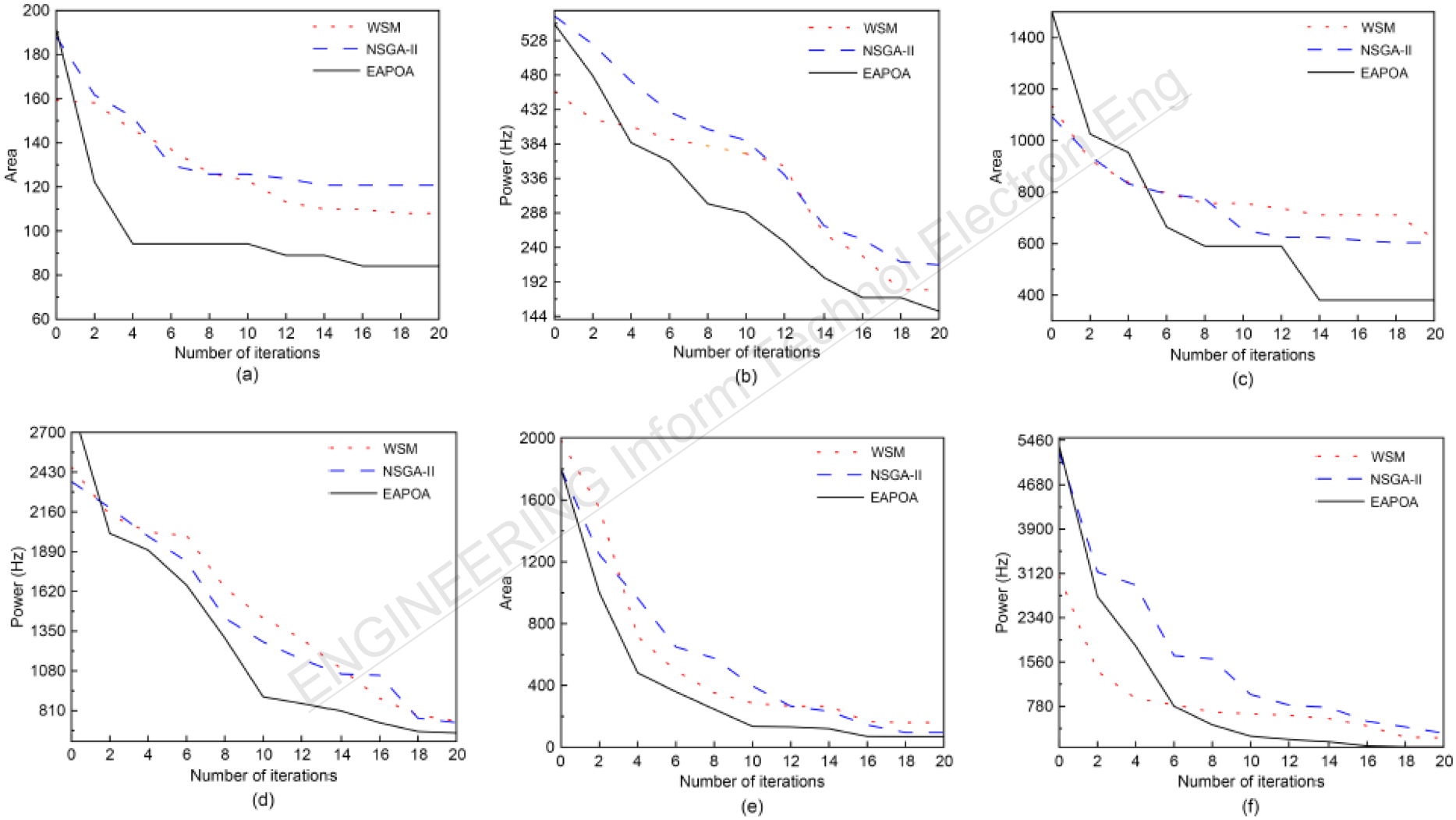
Results



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Fig. 6 Statistical boxplots on ZDT test functions: (a) ZDT1; (b) ZDT2; (c) ZDT3; (d) ZDT4; (e) ZDT6

Results



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Fig. 7 Convergence curves of different circuits: (a) area of the br2 circuit; (b) power of the br2 circuit; (c) area of the amd circuit; (d) power of the amd circuit; (e) area of the bcc circuit; (f) power of the bcc circuit

Results

Table 6 Experimental results on time

Approach	Time (s)												
	rd53	con1	5xp1	rd84	sao2	br1	br2	amd	alu4	table5	bcc	bcd	e64
WSM	5.86	4.32	5.68	10.51	10.71	8.23	4.75	7.78	16.90	20.12	54.83	16.48	500.14
NSGA-II	5.72	6.51	5.55	12.01	15.94	5.96	5.01	13.91	15.39	25.22	64.91	40.12	659.30
EAPOA	6.22	7.01	6.11	9.56	10.01	3.85	4.06	6.05	10.22	16.33	29.99	11.36	300.10
Save1	−6.14%	−62.27%	−7.57%	9.04%	6.54%	53.22%	14.53%	22.24%	39.53%	18.84%	45.30%	31.07%	40.00%
Save2	−8.74%	−7.68%	−10.09%	20.40%	37.20%	35.40%	18.96%	56.51%	33.59%	35.25%	53.80%	71.68%	54.48%

Save1 and Save2 are the time-saving rates of EAPOA relative to WSM and NSGA-II

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Conclusions

In this work, we propose an EAPOA for MPRM logic circuits, which searches for Pareto non-dominated solution sets corresponding to MPRM circuits. The effectiveness of the EAPOA on optimal solutions, time, and convergence is verified by comprehensive experiments, which can be used as a promising approach for developing electronic design automation tools.

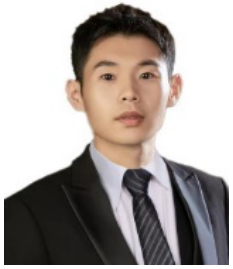
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