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Digital-to-analog converter free architecture for digital reconfigurable intelligent surface

Key words: Reconfigurable intelligent surface; Hardware implementation; High-order modulation

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Motivation

1. Owing to the potential benefits of multiple paths generated by the large-scale elements, reconfigurable intelligent surface (RIS) structure tends to exhibit considerable potentiality in wide-area coverage and terahertz communication.

2. The power consumption of a single RIS element reaches the mW-level, with the result that the power consumption of a RIS structure reaches the W-level after the integration of hundreds of elements, a phenomenon that runs contrary to the original intention underlying passive communication.

3. The use of a voltage grading method is the currently prevailing state-of-the-art technical recommendation for the division of different constellation points, but the voltage regulation range is limited.

Method

Even as the number of RIS elements increases,
the proposed architecture maintains power consumption at a low level.

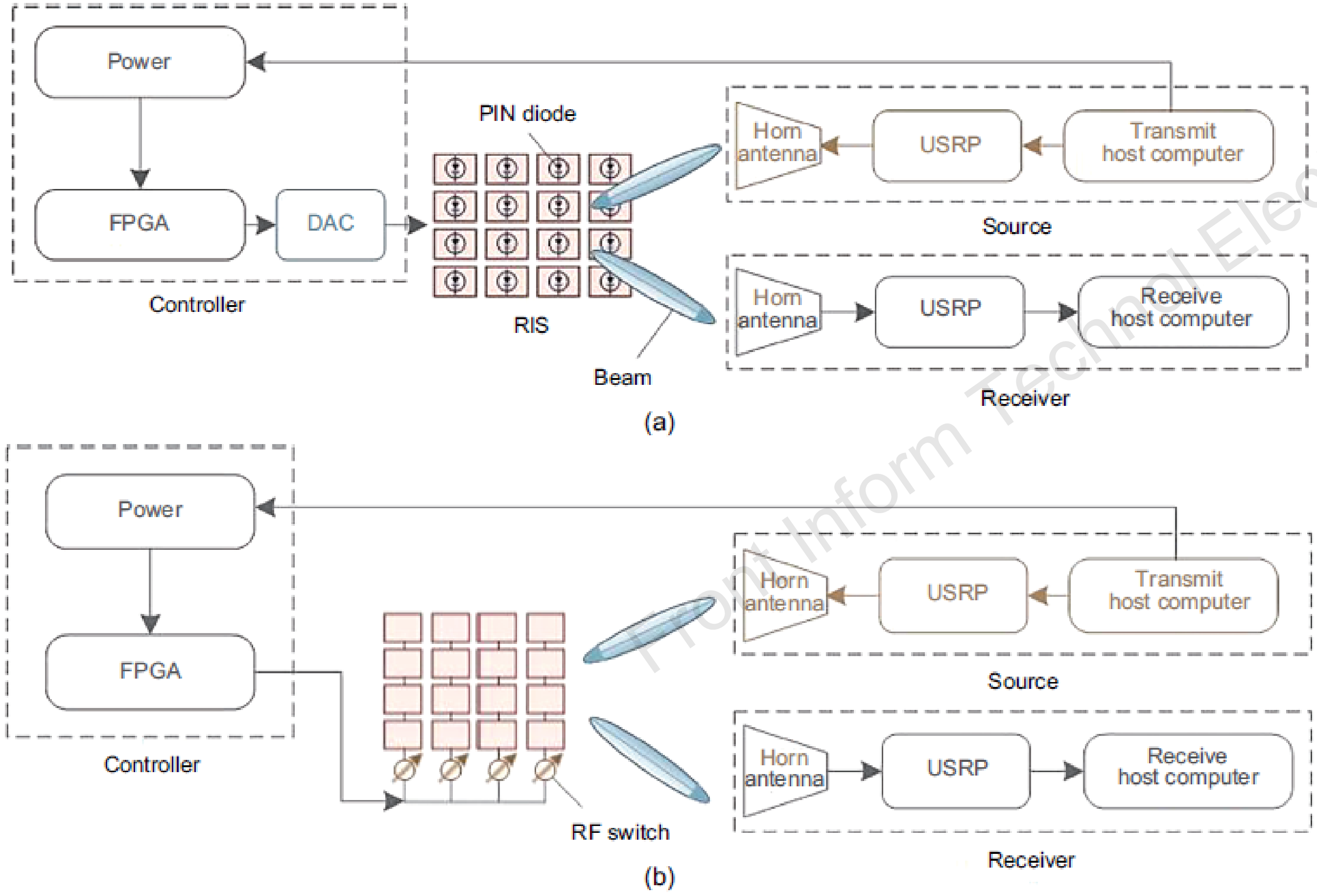

Fig. 1 System structure: (a) a traditional system structure of digital RIS; (b) the proposed DAC-free system structure of digital RIS

Table 1 Power comparison among an active RIS, a traditional passive RIS, and the proposed RIS structure

Core component	Power		
	Active	Traditional	Proposed
Patch/Metamaterial	0	0	0
DAC	1 mW	1 mW	
PIN diode	250 mW	250 mW	
RF switch			1 µW
Amplifier	1.2 W		
FPGA	300 µW	300 µW	300 µW

Method

Transmission line based phase shifter design: easy for adjustment and high precision

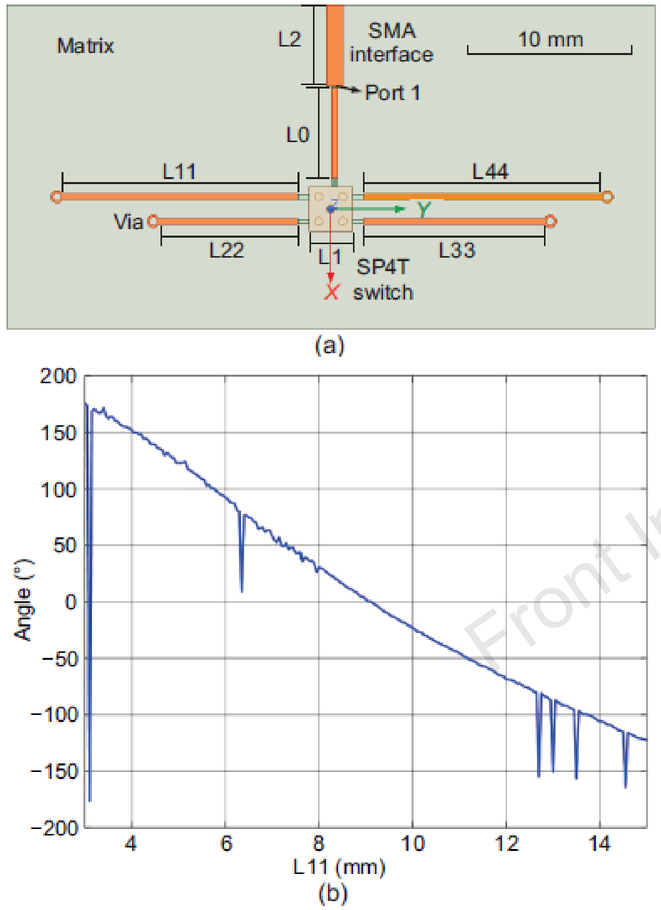

Fig. 2 HFSS model of the 2-bit phase shifter: (a) HFSS model of the SP4T switch and phase shifter; (b) simulation results of the phase angle

Table 2 Parameter settings

Parameter	Value	Description
T	35 µm	Thickness of the immersion gold
H	0.203 mm	Media thickness
W50	0.359 mm	Width of the 50-Ω transmission line
L1	2.7 mm	Pad length of the SP4T switch
L2	5 mm	Pad length of the SMA interface
R1	10 mil	Inner diameter of the via
R2	15 mil	Outer diameter of the via
L11	5.2 mm	
L22	11.3 mm	Simulation results of the lengths
L33	8.7 mm	of the transmission lines
L44	14.65 mm	

Method

High-order modulation scheme: 16-QAM with four reflection coefficients

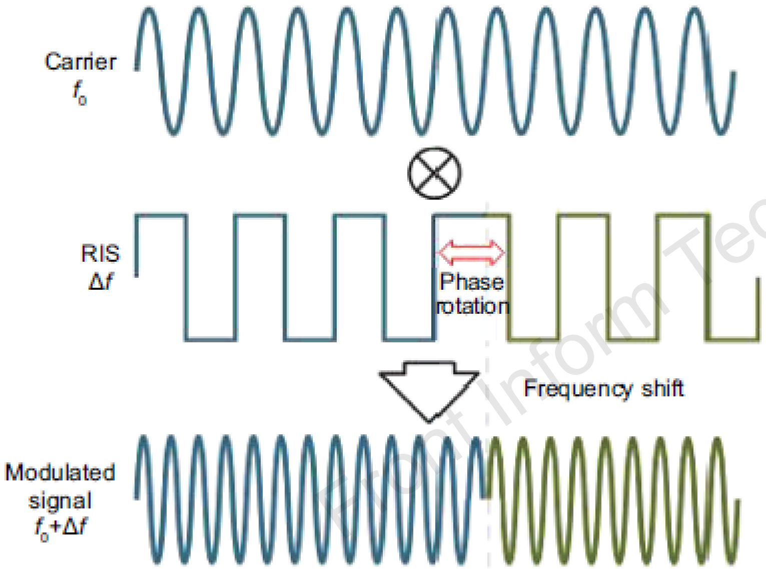

Fig. 3 Modulation principle

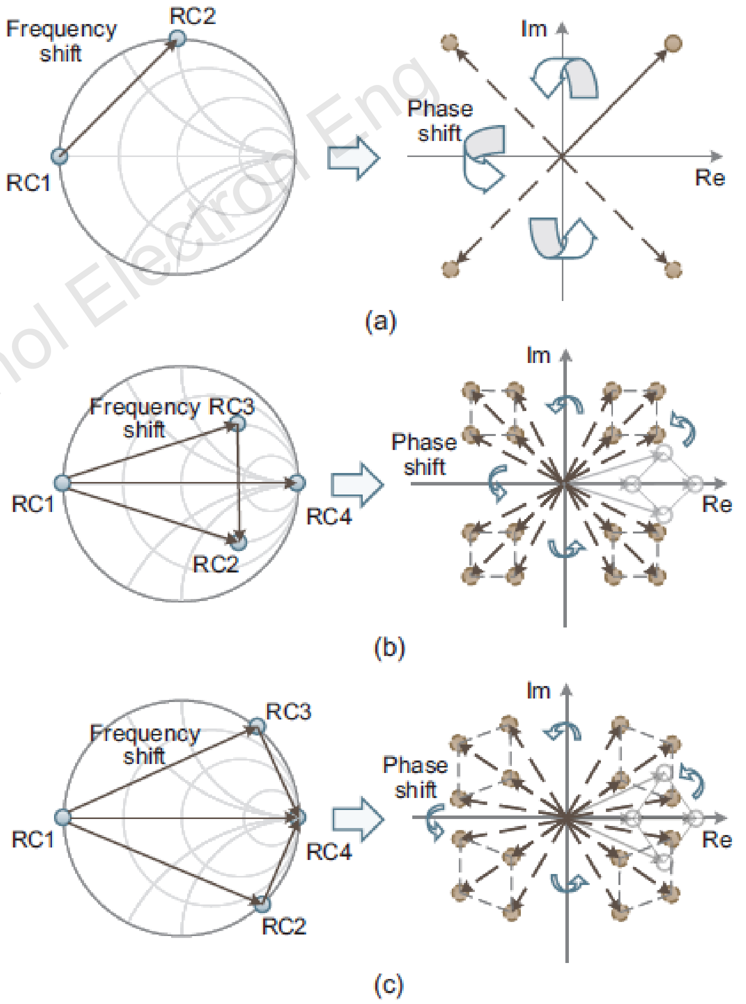

Fig. 4 High-order modulation scheme: (a) QPSK; (b) standard 16-QAM; (c) near-standard 16-QAM

Method

Simulations and experiments: a 4*4 digital RIS for 16-QAM transmission

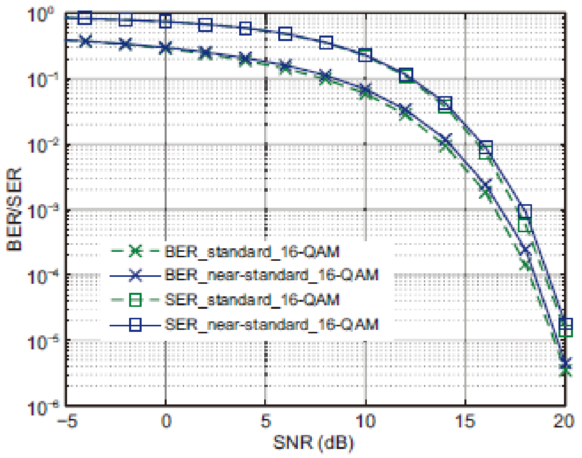

Fig. 6 BER and SER performances of the proposed modulation method

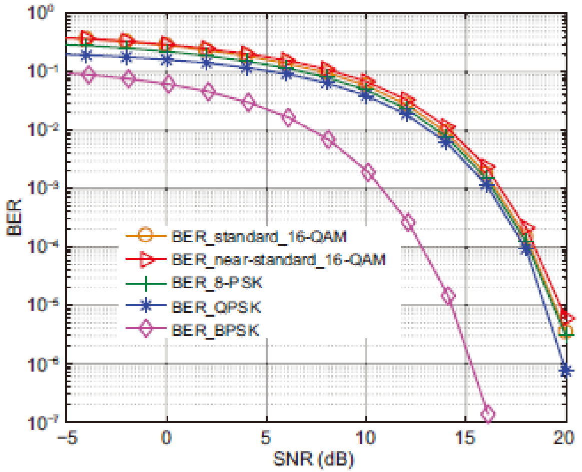

Fig. 7 Comparison of the proposed scheme and traditional schemes

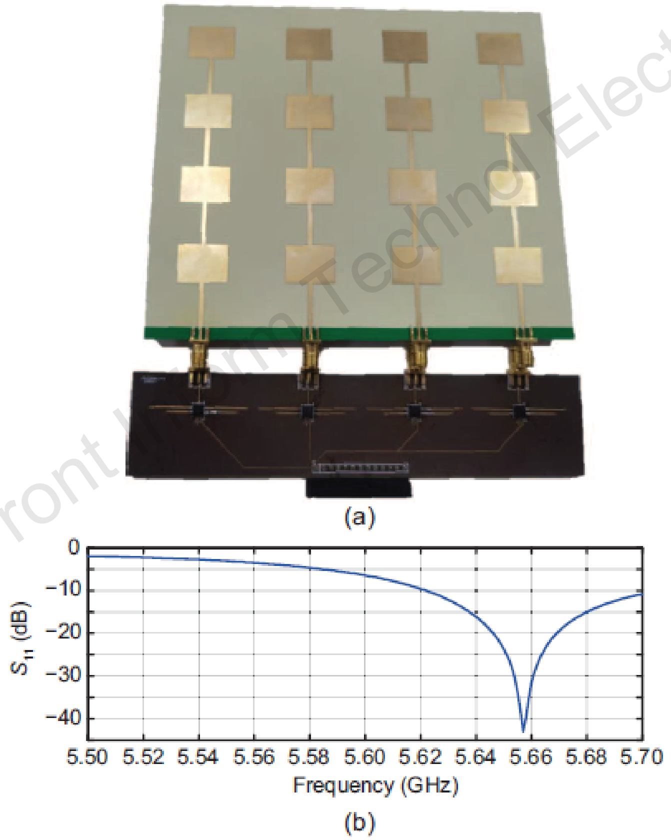

Fig. 8 Prototype of the proposed RIS structure (a) and S_{11} of RIS elements (b)

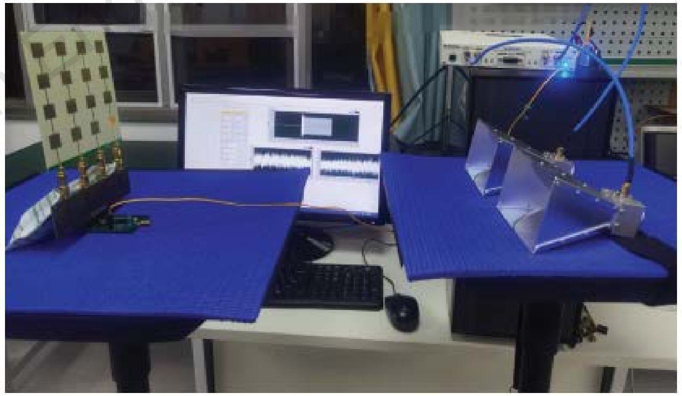

Fig. 9 Test scenario

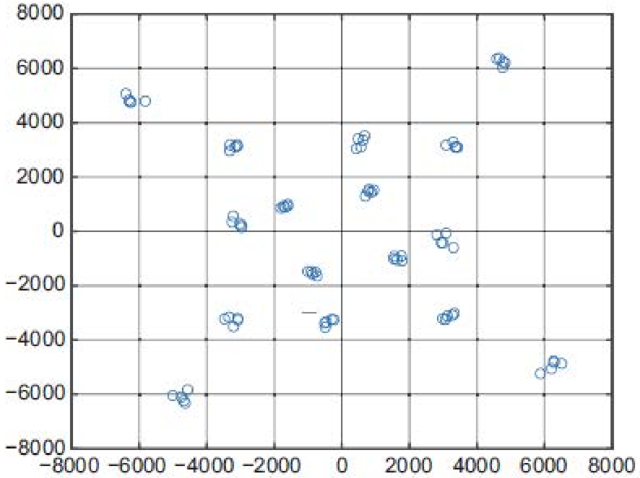

Fig. 10 Demodulation results

Conclusions

1. We proposed a DAC-free architecture for digital RIS structure.
2. We analyzed high-precision phase shifters and novel high-order modulation schemes for the proposed architecture.
3. Simulation and experimental results confirm the feasibility of the proposed algorithm.

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