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Energy-efficient power amplifiers and linearization techniques for massive MIMO transmitters: a review

Key words: Energy-efficient; Linearization; Massive multiple input multiple output (mMIMO); Monolithic microwave inte-grated circuit (MMIC); Power amplifier

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Motivation

- Highly efficient power amplifiers (PAs) and associated linearization techniques have been developed to accommodate the explosive growth in the data transmission rate and application of massive multiple input multiple output (mMIMO) systems.
- System- and circuit-level designers must propose sound and implementable techniques and workarounds to maintain acceptable performance for the mMIMO transmitters from the energy efficiency and signal linearization perspectives.

Main idea

1. Highly efficient Doherty PA MMIC for 5G mMIMO

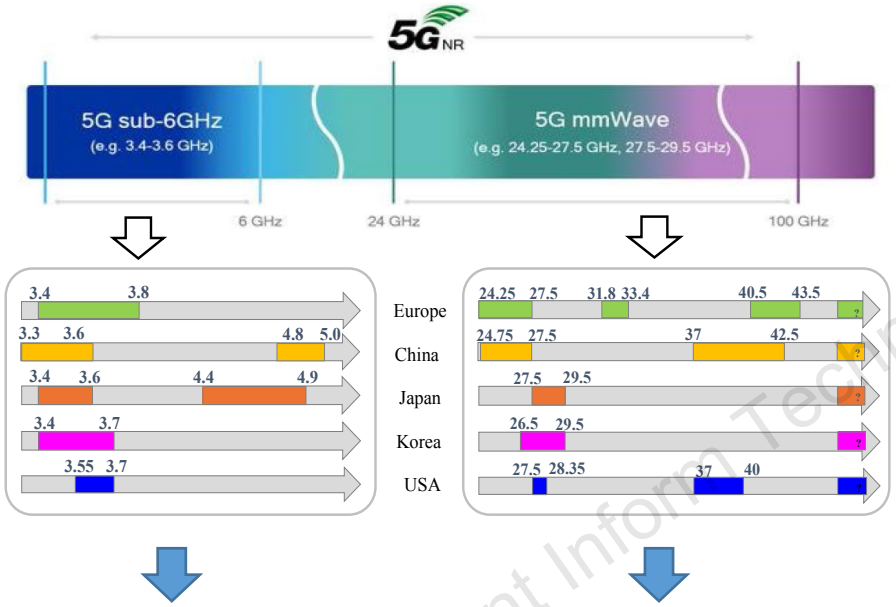
- Design of sub-6 GHz DPA with full, hybrid, and partial integration
- Design of mm-Wave DPA based on III-V semiconductors and the Si-based process

2. PA linearization techniques for the mMIMO transmitter

- Digital predistortion in a fully digital, hybrid, and analog beamforming based mMIMO system
- Circuit-level linearity enhancement techniques

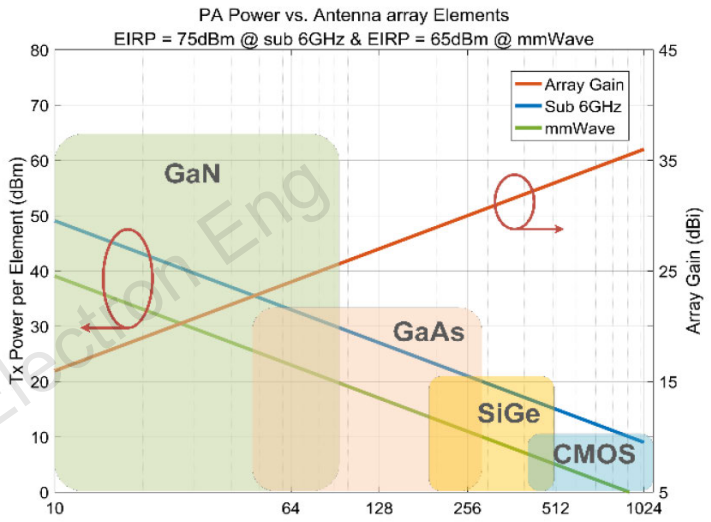
1. Highly efficient Doherty PA MMIC for 5G mMIMO

5G frequency band



- Smaller array size
- Fully digital BF architecture
- Higher output power per channel

- Larger array size
- Hybrid BF architecture
- Lower output power per channel

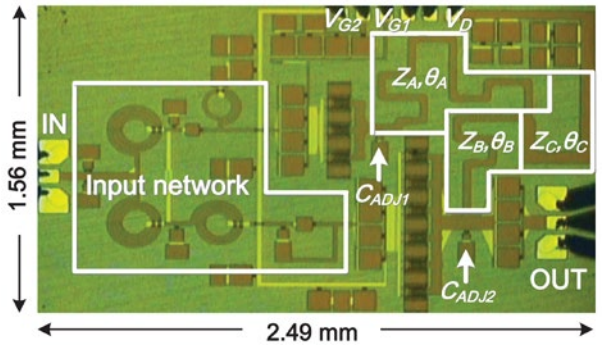


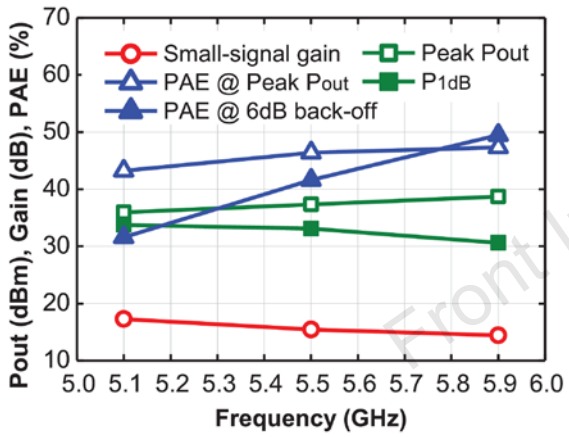
Typical PA specification

Spec.	Sub-6 GHz	mm-Wave
Freq.	3.4–3.8 GHz/ 4.8–5.0 GHz	24.75–27.5 GHz/ 37–42.5 GHz
BW	>200 MHz	>800 MHz
P_{out}@sat	>43 dBm	>25 dBm (III-V)/ 17 dBm (Si)
Average eff.	>40%	>20%
ACPR	<-45 dBc	<-27.5 dBc
EVM	<5% (64QAM)/ <3% (256QAM)	<5% (64QAM)/ <3% (256QAM)

Design of sub-6 GHz DPA

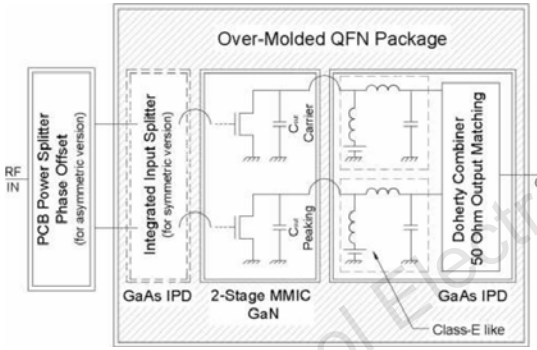
Fully integrated MMIC

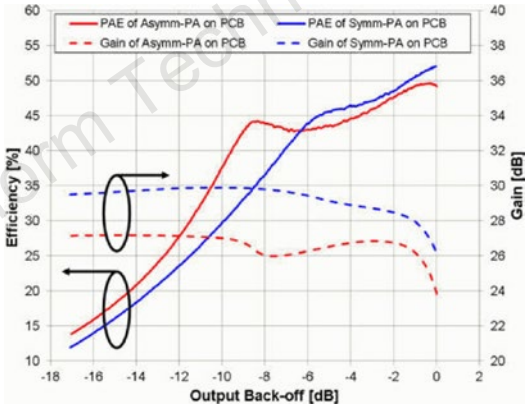




A state-of-the-art DPA with a 6-dB back-off PAE up to 49.5%

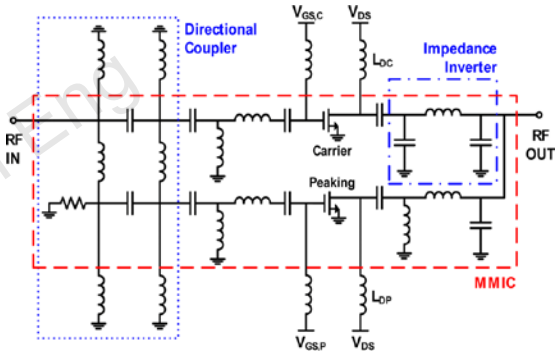
Hybrid integrated MMIC

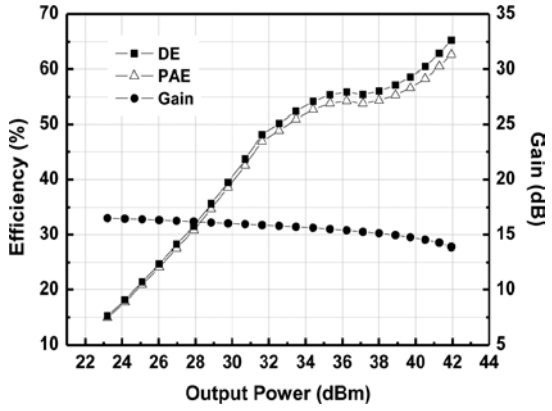




A hybrid MMIC DPA: area-consuming passive networks are implemented on IPDs in the same QFN package

Partially integrated MMIC

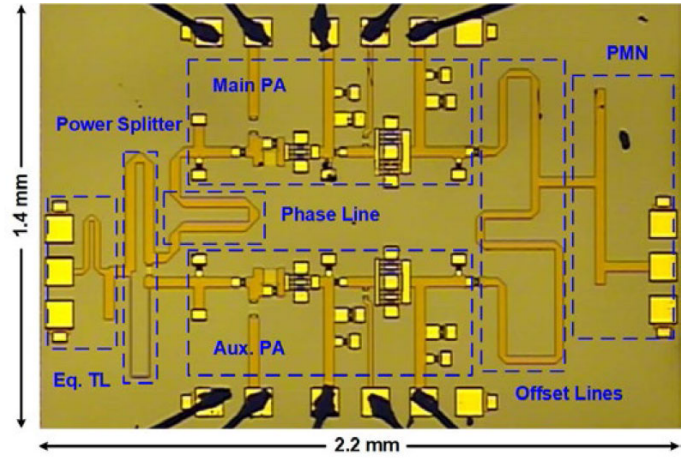


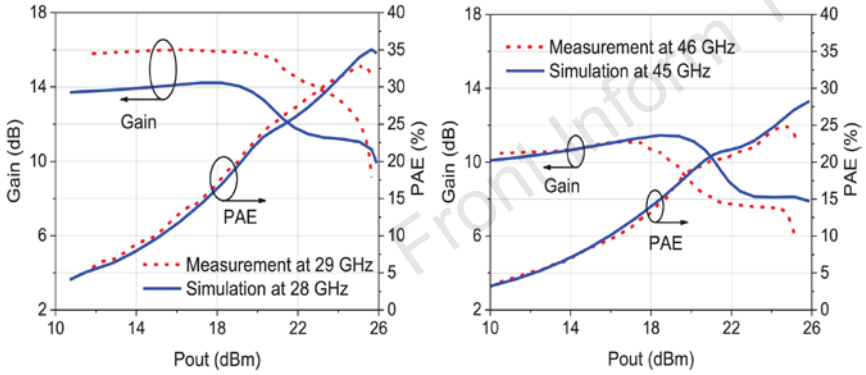


Example: low-loss surface-mounted off-chip inductors are used to enhance the efficiency

Design of mm-Wave DPA

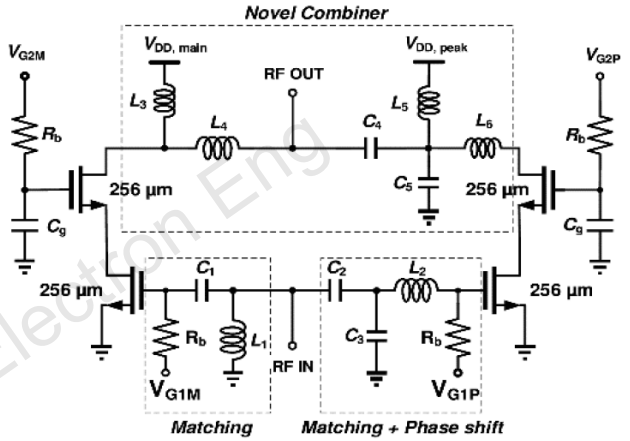
Based on III–V semiconductor

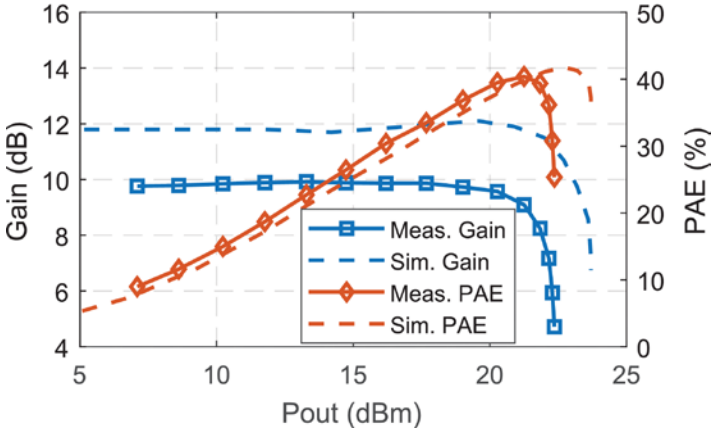




The first demonstration of mm-Wave dual-band DPAs and its measurement results

Based on the Si-based process

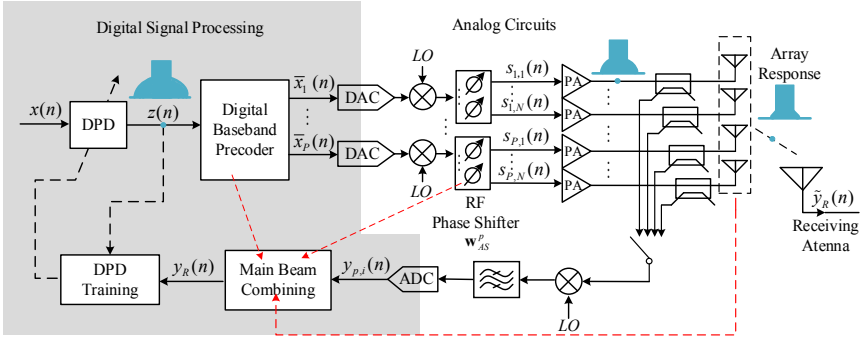




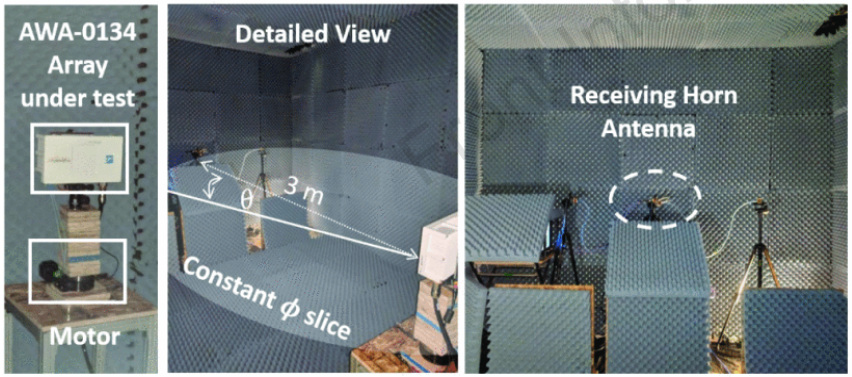
A 28 GHz DPA in CMOS SOI achieves the state-of-the-art performance with a low-loss combiner synthesis technique.

2. PA linearization techniques for the mMIMO transmitter

Digital predistortion technique



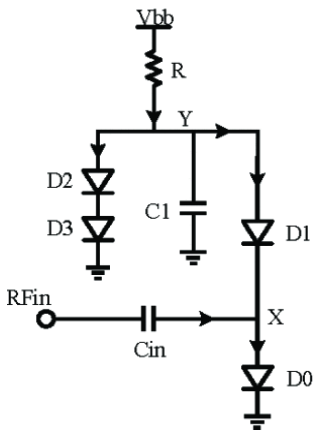
Beam-oriented DPD structure: linearization of the main beam signal rather than the individual PA

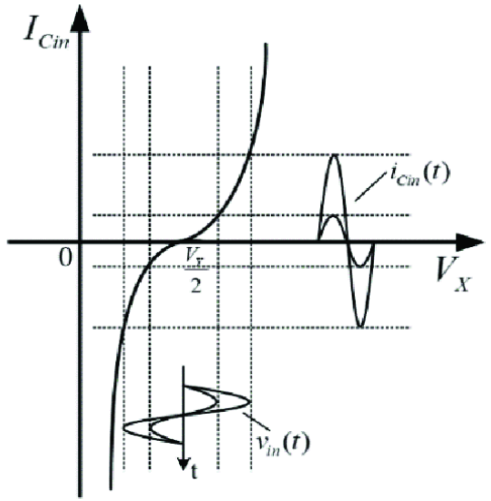


A 2×64 element array experimental measurement setup

Circuit-level linearity enhancement

- Linearization bias circuits
- Analog predistortion
- Antiphase techniques
- Third-order intercept cancellations
- Harmonic short circuit
- …





The equivalent circuit of the linearization bias circuit and its input I–V characteristic curve

Conclusions

- To discuss the integrated Doherty PA MMIC in a 5G massive MIMO system, different semiconductor processes and architectures have been compared and analyzed.
- Digital predistortion, as the most commonly used PA linearization technique, needs to evolve to be adapted to massive MIMO systems.
- Some creative circuit-level linearity enhancement techniques are needed to simultaneously improve the compensation accuracy and reduce the power consumption.