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Exploring high-performance processor architecture beyond the exascale

Key words: High-performance computing; Beyond the exascale; Processor architecture; Application-customized hardware; Distributed computational resources

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Motivations

1. Scientific computation and engineering applications have an insatiable need for computational power.
2. There are several challenges associated with high-performance processor architecture design:
 - (1) Sustainable performance;
 - (2) Energy Efficiency;
 - (3) Performance needs from emerging applications.

Main ideas

1. Goals of architecture design for high-performance processor beyond the exscale:

- (1) Effective performance scaling;
- (2) Effective resource utilization;
- (3) Adaptation to diverse applications.

2. High-performance processor architecture design beyond the exascale should achieve an appropriate balance among computational capability, resource utilization, and application needs.

Methods

1. Many-core processor architecture with scalar processing and application-specific acceleration (Massa):

- (1) Scalar many-core processor;
- (2) Application-specific acceleration.

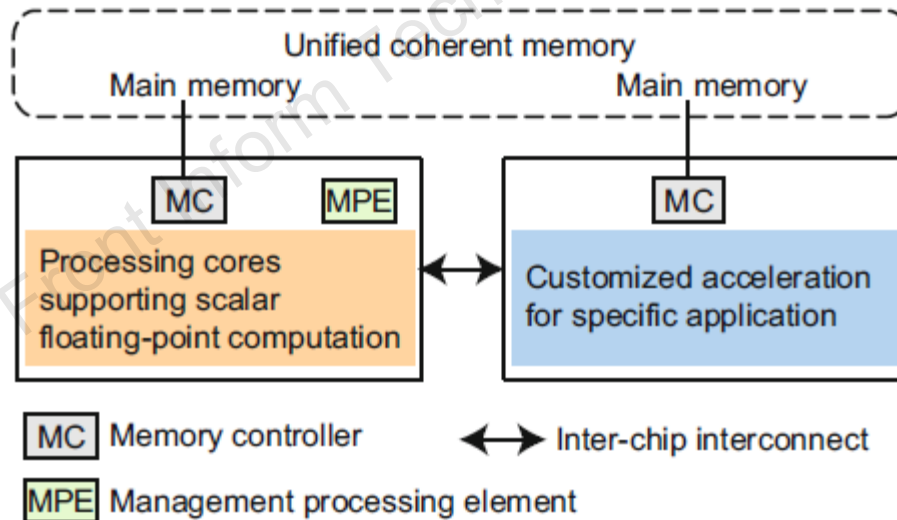


Fig. 1 The high-performance many-core processor architecture with scalar processing and application-specific acceleration (Massa)

Method

2. Modest performance needs are simply met by the host processor running alone. While extreme performance needs from specific applications can be addressed by the coprocessor in Massa.
3. Technique of application-customized hardware is exploited to provide acceleration for demanding applications.
4. The inter-chip interconnect in Massa provides a dedicated fabric for the host processor and the coprocessor to communicate with each other.

Conclusions

1. Effective performance scaling, efficient resource utilization, and adaptation to diverse applications are three goals of architecture design for high-performance processor beyond the exascale.
2. Massa architecture aim to achieve those goals by coupling a scalar processing many-core processor with application-specific coprocessors and employing techniques of distributed computational resource and application-customized hardware.
3. Future research includes an alternative unified coherent memory mechanism, designing a customized coprocessor for scientific computation, and engineering applications and demonstrate the promise of Massa architecture.