Ying-hui Zhong, Shu-xiang Sun, Wen-bin Wong, Hai-li Wang, Xiao-ming Liu, Zhi-yong Duan, Peng Ding, Zhi Jin. Two-step gate-recess process combining selective wet-etching and digital wet-etching for InAlAs/InGaAs InP-based HEMTs. *Frontiers of Information Technology & Electronic Engineering*, 2017, **18**(8): 1180-1185. https://doi.org/10.1631/FITEE.1601121

Two-step gate-recess process combining selective wet-etching and digital wet-etching for InAlAs/InGaAs InP-based HEMTs

Key words: High electron mobility transistors (HEMTs); Gate-recess; Digital wet-etching; Selective wet-etching

Contact: Ying-hui Zhong
E-mail: zhongyinghui@zzu.edu.cn
ORCID: http://orcid.org/0000-0001-9983-6729

Introduction

- The thickness of InGaAs cap and InAlAs barrier layers are merely several dozens of nanometers. Good selectivity is necessary to make gate-recess etching automatically stop at InAlAs barrier layer, and only then can the gate electrode be placed directly on barrier layer.

- The distance between the gate and channel is just determined by the thickness of InAlAs barrier layer in high-selective gate-recess etching process. Given that, alternative non-selective digital wet-etching is intensely required to further improve the flexibility and controllability of fabrication process.

- A two-step gate-recess process which couples high-selective wet-etching and non-selective digital wet-etching techniques is proposed for InAlAs/InGaAs InP-based HEMTs.

Gate-recess process

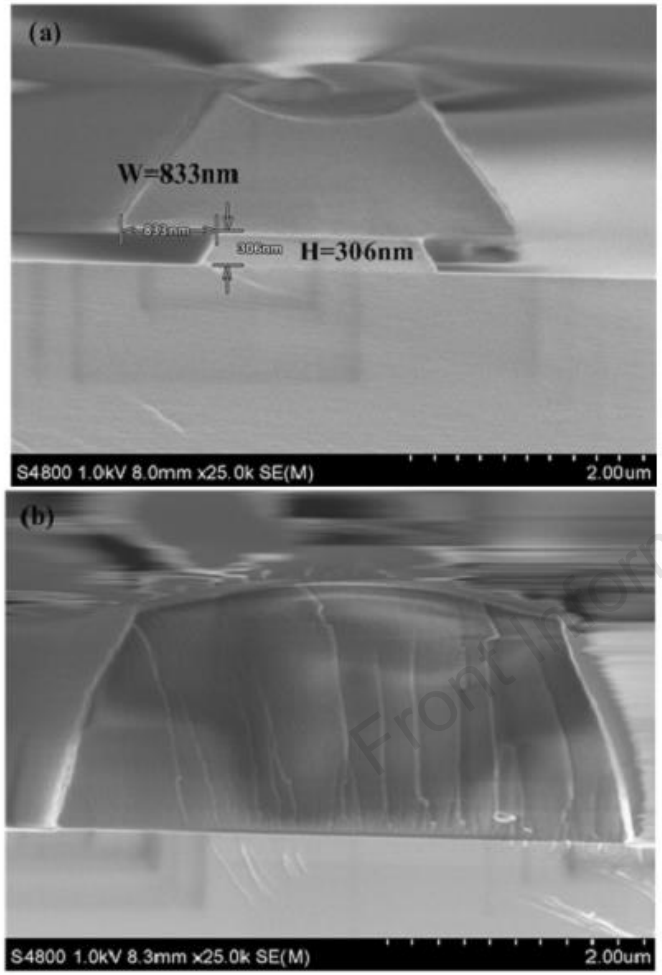

Fig. 2 The SEM photography of cross-sectional samples after high selective wet-etching for 5 mins. (a) InGaAs/InP sample, (b) InAlAs/InP sample

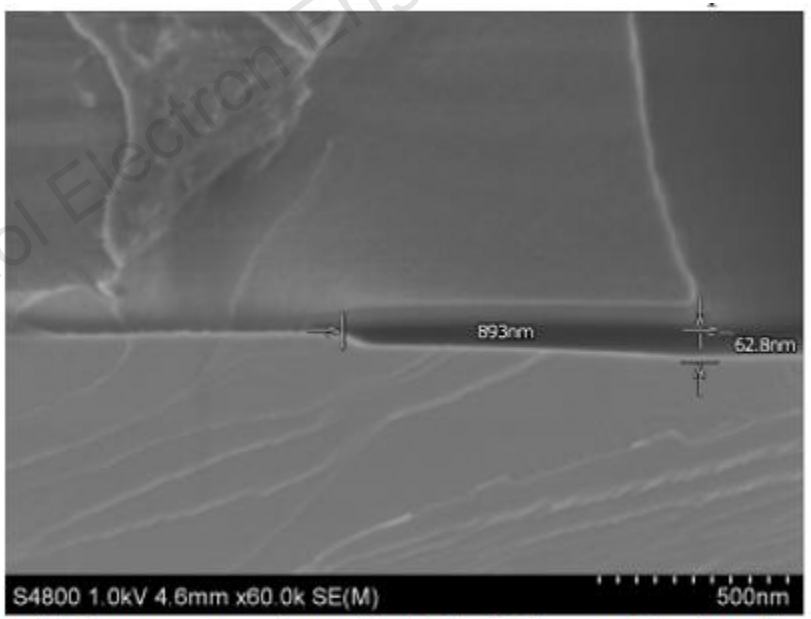

Fig. 4 The cross-section of InAlAs/InP sample after 50 times digital wet-etching cycles

Results

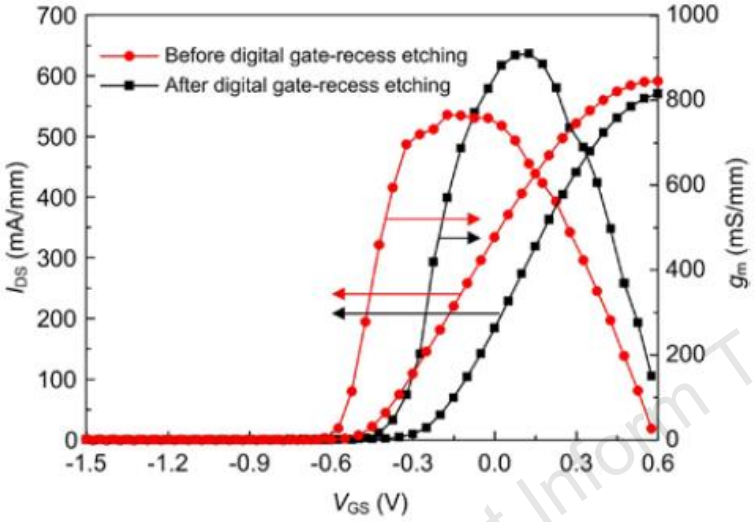

Fig. 5 The transfer characteristic curves of InP-HEMTs before and after digital gate-recess etching

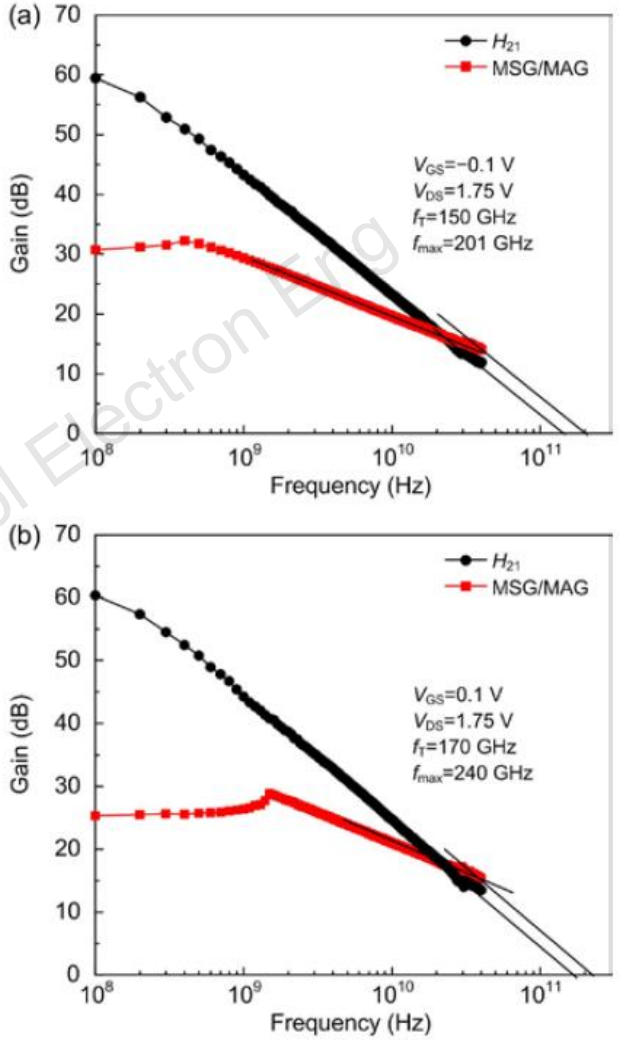

Fig. 6 H_{21} and MAG/MSG versus the frequency of InP-based HEMTs before (a) and after (b) digital gate-recess etching

Conclusions

- The high-selective wet-etching is developed to get rid of the InGaAs cap material without influencing the InAlAs barrier layer, and the etching selectivity ratio of InGaAs material to InAlAs material has exceeded 100 by using the mixture solution of succinic acid and H_2O_2.
- The non-selective digital wet-etching process is developed on the basis of a separately controlled oxidation/de-oxidation technique, and each digital etching cycle performs 1.2 nm InAlAs material.
- The two-step gate-recess etching technique has been successfully incorporated into InP-based HEMTs fabrication. Consequently, InP-based HEMTs have demonstrated superior extrinsic transconductance and RF characteristics than devices just by selective gate-recess etching process.