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A multistandard and resource-efficient Viterbi decoder for a multimode communication system

Key words: Reconfigurable Viterbi decoder; Multi-parameter; Low resource consumption; Standard convolutional symbols generator (SCSG); Fully optional polynomials

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Motivation

1. With the diversification of the application scenarios, telecommunications terminal devices are required to operate on multiple communication standards, and the Viterbi algorithm must support multiple standards.

2. Research on reconfigurable Viterbi algorithm was mainly concentrating on dynamic reconfigurability, high throughput, and multiple parameters. However, little research has been devoted to fulfilling all of the conditions for a reconfigurable Viterbi decoder, such as reconfigurable properties, speed, and resource consumption.

Main idea

- **Flexible reconfiguration**:
  - ✓ Configuration unit;
  - ✓ Recalculating of branch metric;
  - ✓ Rearranging the correspondence between branch metrics and paths;
- **Low resource consumption**:
  - ✓ Calculating standard convolutional symbols by iterative method;
  - ✓ Calculating the full results by reusing the lower-bit results;
  - ✓ Combination of serial operation and parallel calculation.

Structure of the proposed Viterbi decoder

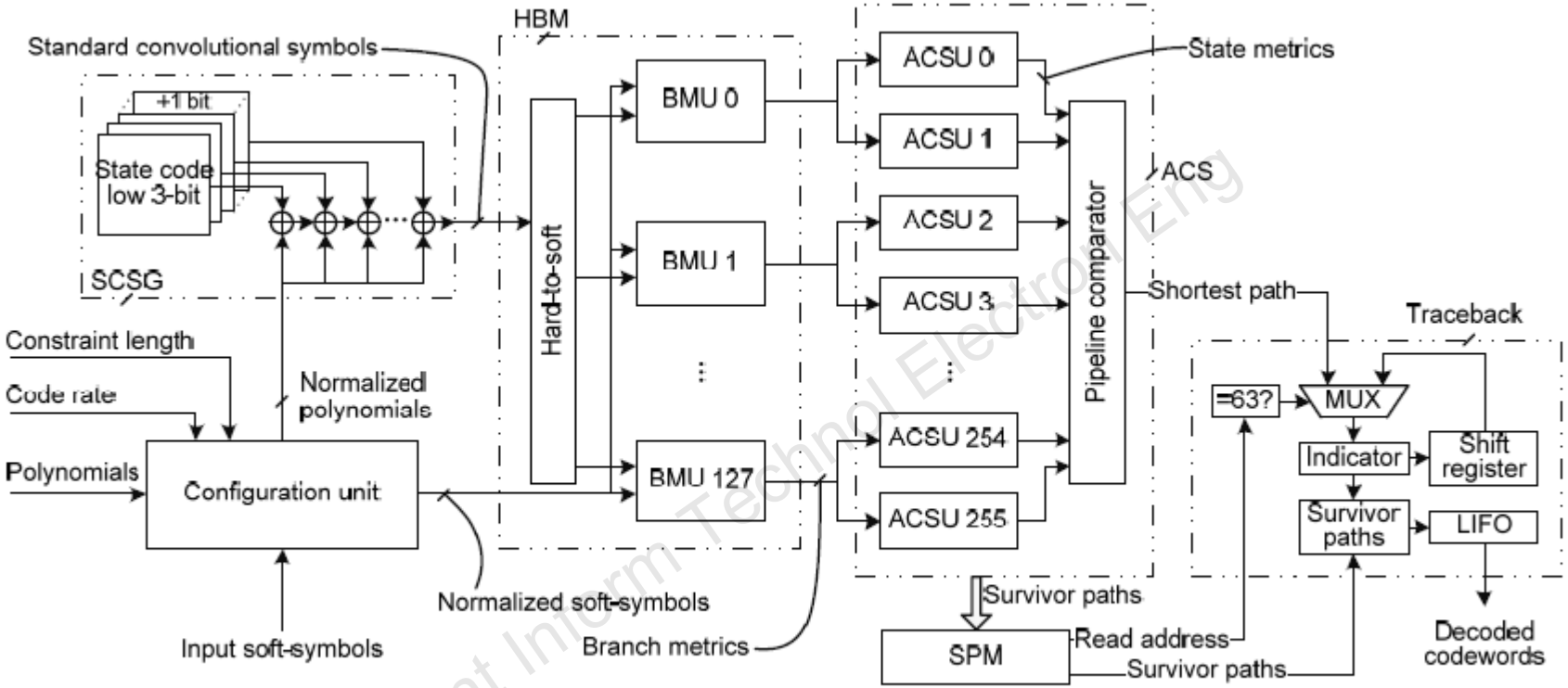


Fig. 1 Block diagram of the reconfigurable Viterbi decoder

- The configuration unit (CU) generates normalized symbols and polynomials according to the input parameters.
- SCSG is in charge of the generation of all the states and the calculation of standard convolutional symbols.

Configuration unit (CU)

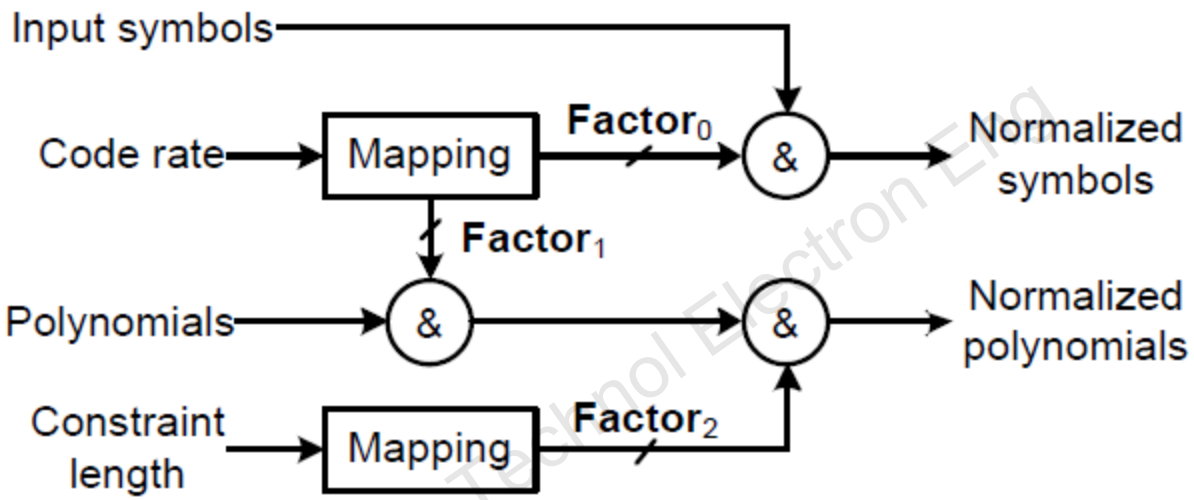
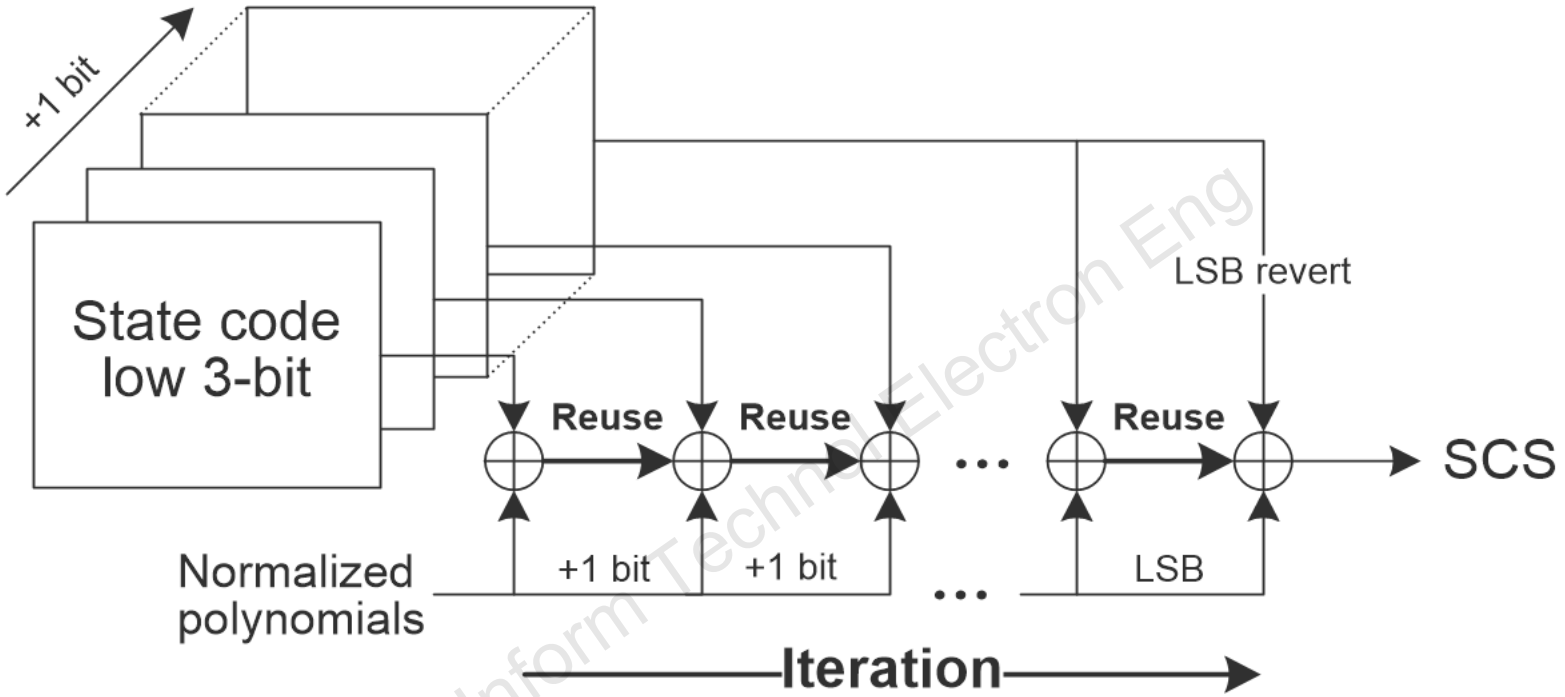


Fig. 2 Fabric of the configuration unit

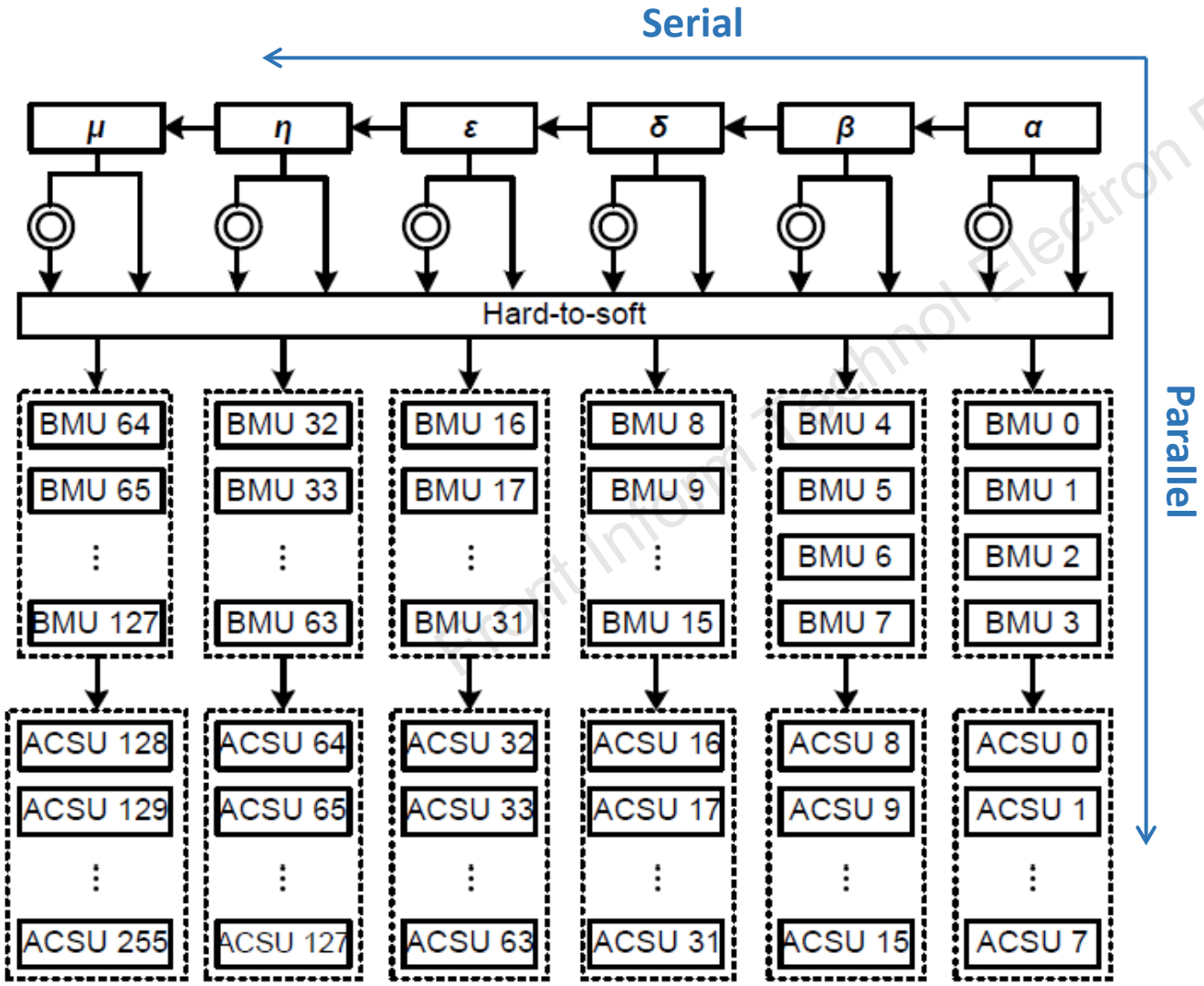
- CU is an LUT-like model, the output of it will change immediately when the input parameters alter.
- The normalized symbols and polynomials are fed into SCSG and BMUs to recalculate branch metrics and convolutional symbols.

Iterative and reusable method in SCSG



- All the states are derived from the low 3-bits of the starting state code.
- The standard convolutional symbols (SCS) will come out after several iterative calculations.
- Each step will reuse the results of the lower-bit.

Combination of serial operation and parallel calculation



The flow of iterative computations is serial.

At each iteration stage, all the calculations, such as the branch metrics' computation, are computed concurrently.

Major results (1)

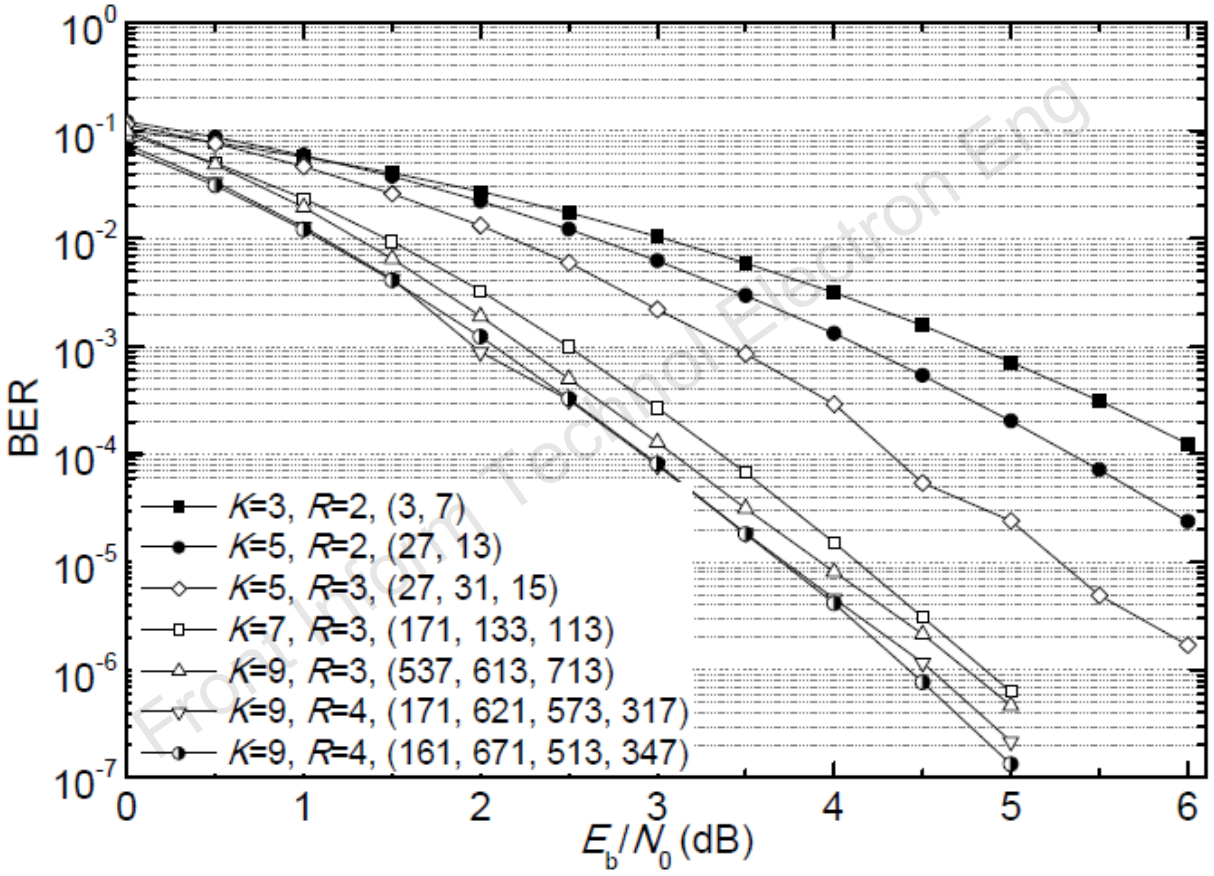


Fig. 5 Bit error rate of the proposed architecture

The numbers in parentheses indicate the polynomials in octal format

Major results (2)

The SCSG-based Viterbi decoder has been implemented on Xilinx Virtex-7 device. The detailed features of the proposed architecture and the reported works are shown in the following table. In comparison, both the throughput and the compatibility of the SCSG-based decoder were improved.

Table 3 Comparison of key features of the architectures reported

Reference	Constraint length	Code rate	Maximum throughput (Mbps)	Number of logic gates (k)
This paper	3–9	1/2, 1/3, 1/4	200	162
Cavallaro and Vaya (2003)	3–9	1/2, 1/3	60.6	190
Batcha and Sha'ameri (2007)	5,7	1/2, 1/3	150	–
Campos and Cumplido (2006)	3–7	1/2, 1/3	70	175
Vennila et al. (2013)	3–7	1/2, 1/3	81	113
Niktash et al. (2006)	7, 9	1/2, 1/3	27, 10	–
Bissi et al. (2008)	4–9, 10–14	1/2, 1/3	0.337	1.314
Swaminathan et al. (2002)	7, 9	1/2, 1/3	3.125, 12.5	95
Benaissa and Zhu (2003)	7–10	1/2	101	172

Although some of the reported architectures were implemented on different FPGA platforms, the authors gave the equivalent number of logic gates.

Conclusions

1. Inspired by the observations in a recent survey, this paper presents a fully flexible reconfigurable Viterbi decoder with a novel standard convolutional symbol generator (SCSG).

2. The SCSG-base Viterbi decoder can support a constraint length of 3–9, code rates of 1/2, 1/3, 1/4, and fully optional polynomials, the maximum throughput is about 200 Mbps and logic gate consumption is 162 k, these results show that the SCSG improves the flexibility and the throughput of the decoder without sacrificing the area.