Hadi JAHANIRAD, 2023. Dynamic power-gating for leakage power reduction in FPGAs. *Frontiers of Information Technology & Electronic Engineering*, 24(4):582-598. https://doi.org/10.1631/FITEE.2200084

Dynamic power-gating for leakage power reduction in FPGAs

Key words: Field programmable gate array (FPGA); Leakage power; Power-gating; Transistor-level circuit design

Corresponding author: Hadi JAHANIRAD
E-mail: h.jahanirad@uok.ac.ir

ORCID: https://orcid.org/0000-0001-8586-6281

Motivation

1. In modern FPGAs, power consumption is a big concern. Despite their advantages (reconfigurability, short time to market, and so on), high power consumption makes FPGAs unattractive for low-power concerned. This paper proposes a low-power design for FPGAs.

2. Power-gating as a promising low leakage technique has not been applied to the active mode operation of FPGA modules in previous studies. Our proposed design extends the application of the power-gating technique to active mode operation.

3. Delivering the power control signals (PCSs) to the FPGA modules was a complex problem in previous low-power designs. In this paper, an efficient architecture is proposed for PCS delivering.

Main idea

1. Presentation of an efficient architecture for delivering PCSs to power-gating regions (PGRs).

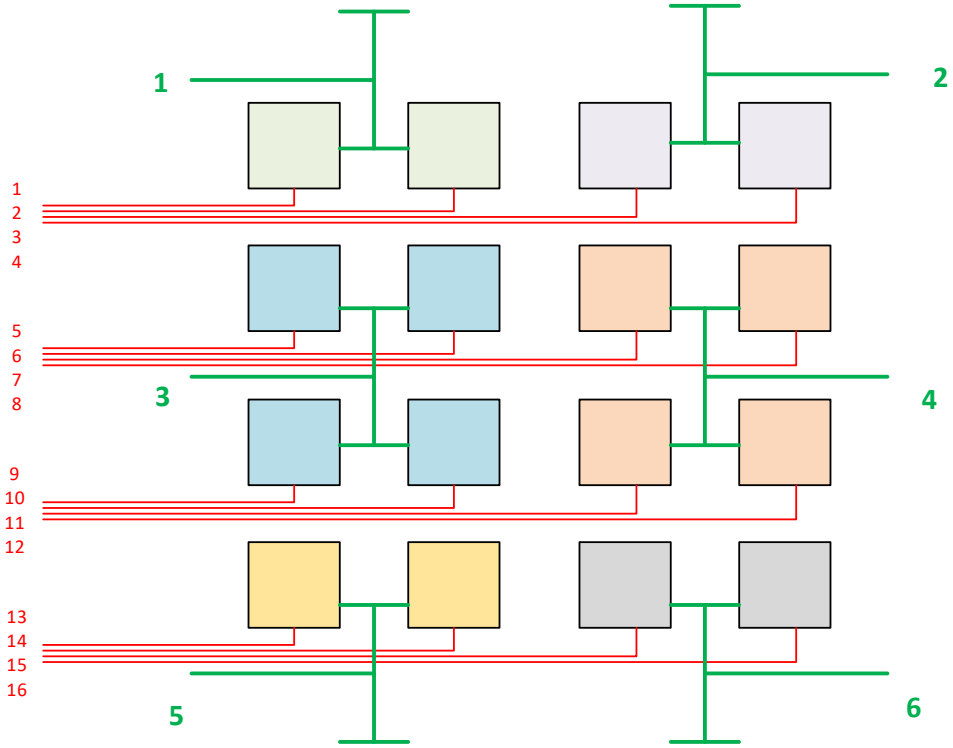
2. Dynamic power-gating (DPG) of the logic and routing resources with a long idle period.

3. Re-design of the main modules (configurable logic blocks (CLBs), switch boxes (SBs), and connection boxes (CBs)) so that the unused resources are statically power-gated.

4. Handling of leakage power consumption in the active mode of internal modules.

Method

1. The fixed PGRs are defined in FPGA, and an H-tree architecture is implemented to route the PCSs to the defined PGRs.



Method (Cont'd)

2. The lower supply voltage of every module in a PGR is directly connected to the related PCS to eliminate the extra power-gating transistor.

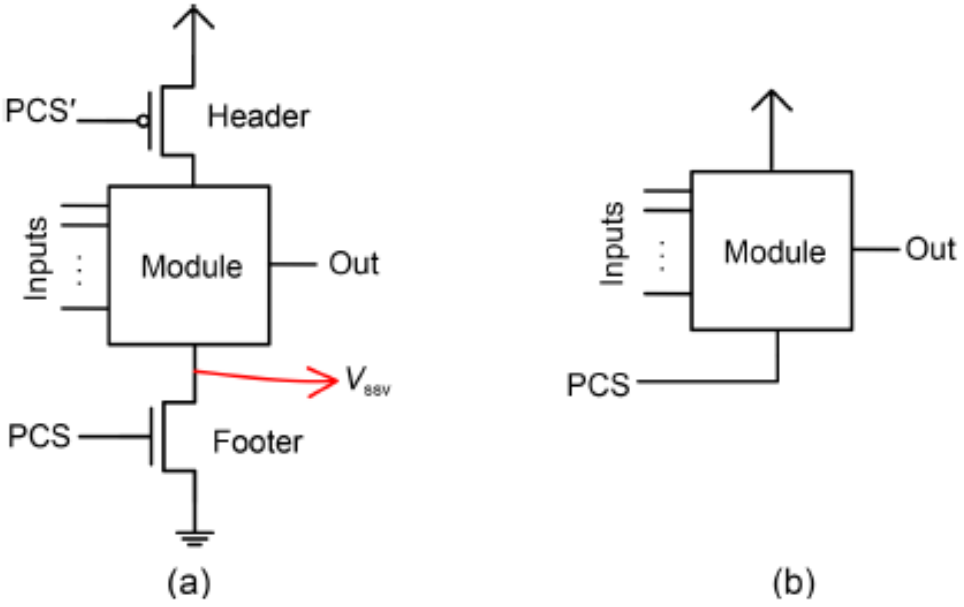


Fig. 3 Power-gating of a module: (a) conventional method; (b) proposed method (PCS: power control signal)

Method (Cont'd)

3. A new power-gating design is proposed for every module of the FPGA wherein the leakage power in both sleep and active modes is reduced efficiently.

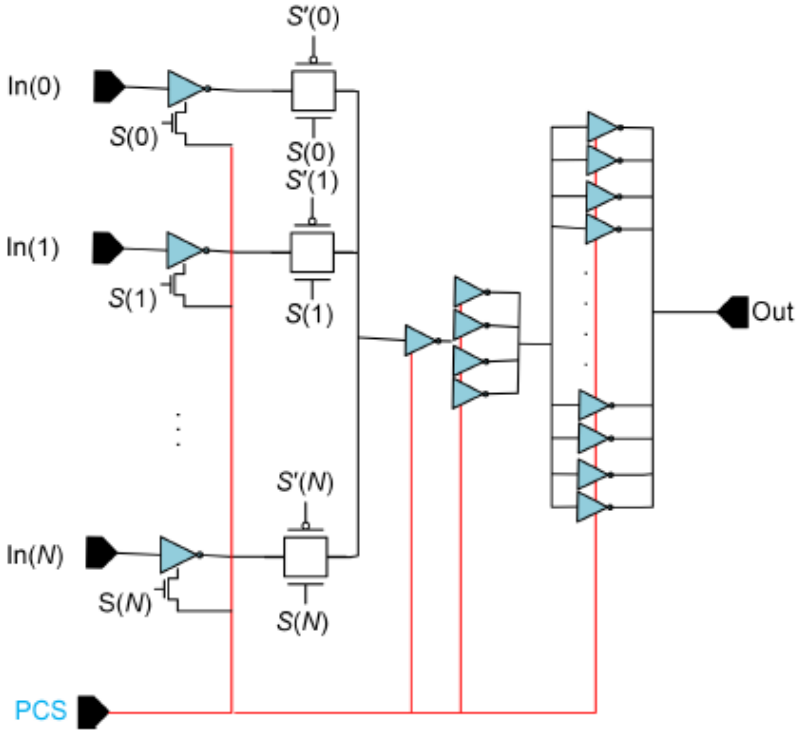


Fig. 11 Internal circuitry of the switch box (SB)/connection box (CB) multiplexer

Method (Cont'd)

4. DPG is realized using the signals generated by the power controller module.

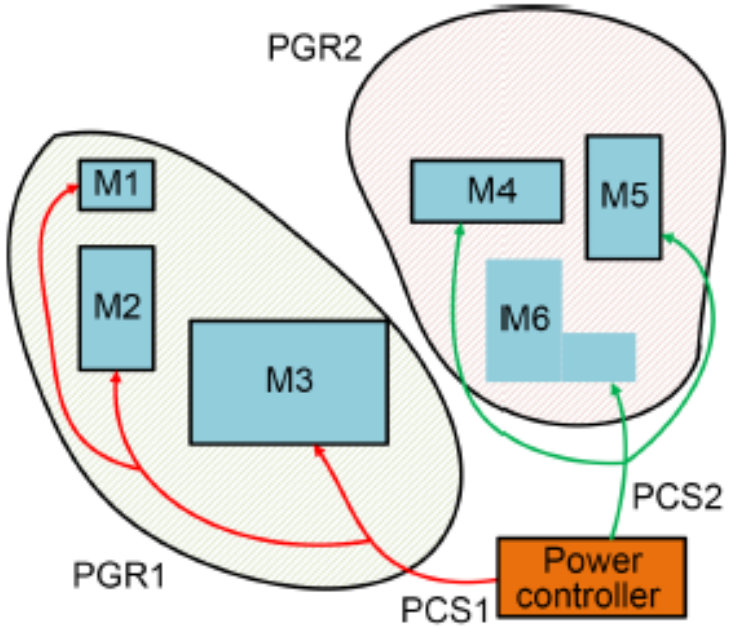


Fig. 1 A digital system consisting six modules and two PGRs (PCS: power control signal; PGR: power-gating region)

Major results

1. The policy of inserting extra transistors to turn off the unused resources in the crossbar, CB, and SB modules results in 40% and 35% active leakage reduction compared to the static power-gating (Static-PG) and non-gated (NG) approaches, respectively.

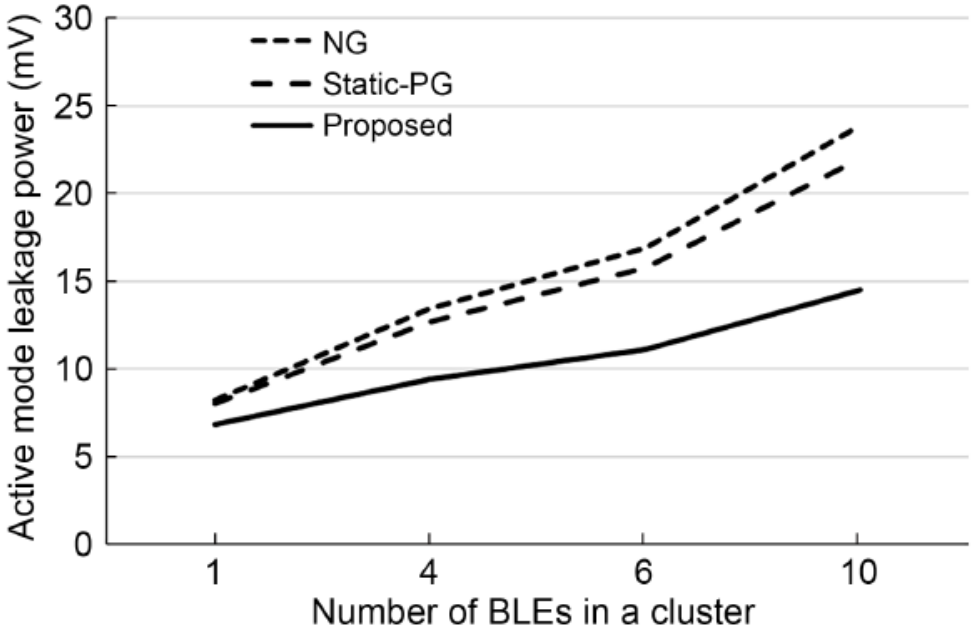


Fig. 12 Tile leakage reduction in active mode

Major results (Cont'd)

2. The leakage power is reduced by about 95% in the sleep mode in our proposed design.

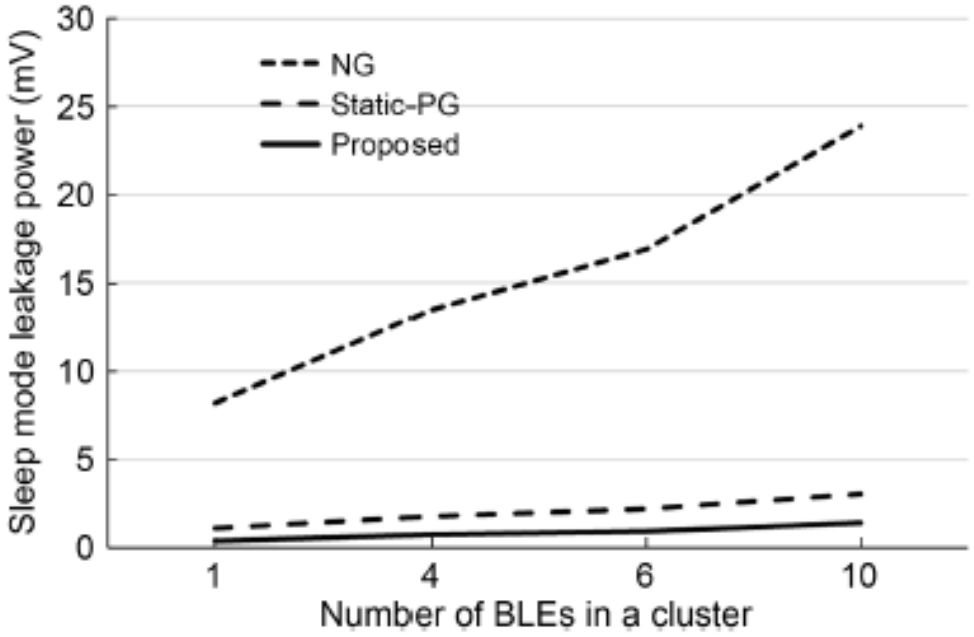


Fig. 13 Tile leakage reduction in sleep mode

Major results (Cont'd)

3. The proposed method reduces leakage power consumption by more than 55% (15%) for synthetic benchmark circuits compared with the Static-PG (DPG) approach.

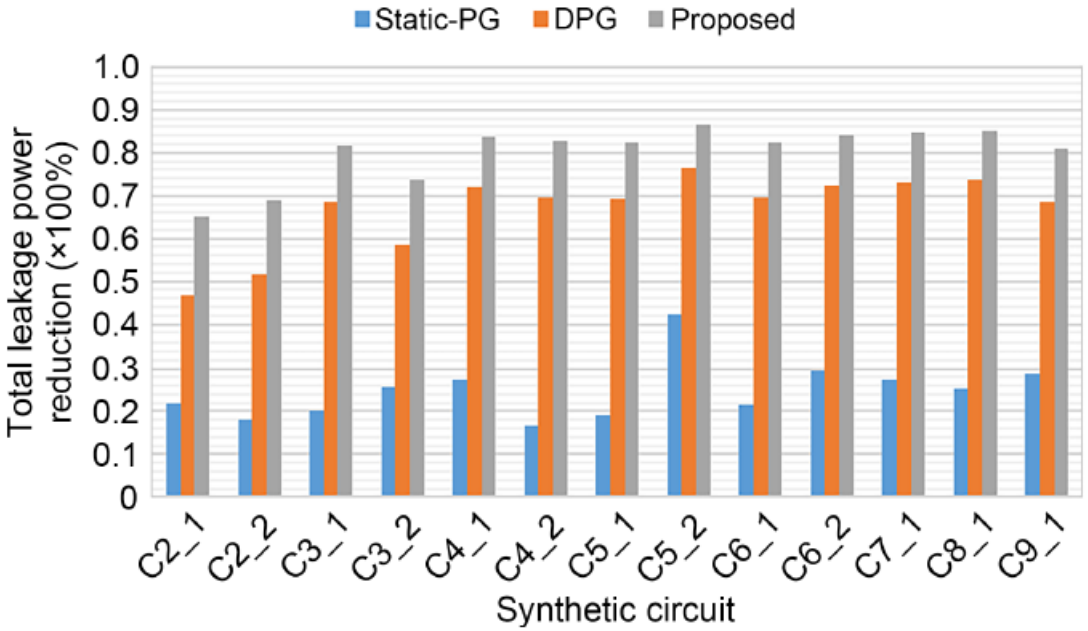


Fig. 15 Total leakage power reduction

Conclusions

In this paper, a low-power FPGA architecture is developed in which the dynamic power-gating technique is employed to reduce the leakage power consumption of internal modules. Two main features distinguish the proposed design from previous ones. First, a low-cost routing network is proposed to implement the power control signals. Second, each module is re-designed to reduce the leakage power in both the active and sleep modes. Simulation results demonstrate a 95% reduction of leakage power consumption in sleep mode. The total power consumption is reduced by 80% in the proposed design, which is 15% better than that of the best state-of-the-art design. Meanwhile, the area overhead of the proposed design (less than 4.3%) outperforms those of the previous architectures.

Hadi JAHANIRAD received his BS degree in electrical engineering from the Department of Electrical Engineering, Khaje Nasir Toosi University, Tehran, Iran, in 2006, and his MS and PhD degrees from Iran University of Science and Technology, Tehran, Iran in 2008 and 2012, respectively. Since 2013, he has been with the Department of Electrical Engineering, University of Kurdistan, Sanandaj, Iran, where he is now an associate professor. His main research interests are digital system design, VLSI design, reliability analysis of logic circuits, digital circuit testing, approximate computing, and evolutionary computing.