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# A driving pulse edge modulation technique and its complex programming logic devices implementation

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**Key words:** Driving pulse edge modulation, Switching voltage spike, Complex programmable logic device (CPLD), Active gate drive

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# Introduction

- With the continual increase in switching speed and rating of power semiconductors, a switching voltage spike becomes a serious problem.

- Traditional and active drive are two main types of gate drivers in applications. With the development of digital drive techniques, some new strategies have been employed.

- This paper describes a new technique of driving pulse edge modulation and its CPLD implementation. Experimental results demonstrate the effectiveness and practicability of the proposed method.

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# Main idea

- Reducing the IGBT's turn-on and turn-off speed is effective in restraining the switching voltage spike.

- Regardless of the Miller effect, the behavior of the traditional driving circuit can be treated as the charging and discharging processes of an RC circuit under a square wave power supply. The gate voltage of an IGBT during the switching period has a cumulative effect.

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# Main idea (Con'd)

- The gradually rising and falling edges of the gate driving pulse signal can be mapped into pulse trains, and the gate driving voltage turns accordingly into the accumulation of each pulse's response.

- Take the IGBT turn-on process, as an example. A pulse train can be imposed before the traditional gate driving signal. By mapping the driving pulse edge into a pulse train, the modulation of the pulse edge can be changed into the modulation of the width and density of the pulse train.

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# Method

- Bidirectional pulse train modulation
  - The modulated pulse width modulation (MPWM) signal is realized by imposing a series of positive and negative levels. When the signal is positive, the positive driving voltage $v_{ge,on}$ is used, and when the signal is negative, the negative driving voltage $v_{ge,off}$ is used.

  - During the IGBT's turn-on period, if the response capability of the driving circuit is limited, the edge of the gate driving voltage will appear as an obvious zigzag. As a result, the gate voltage will fluctuate around the turn-on threshold voltage which will cause the pseudo turn-on of the IGBT.

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# Method (Con'd)

- Unidirectional pulse train modulation
  - When modulating the rising edge, the high level signal means connecting to the positive driving voltage $v_{ge,on}$ and the low level signal means connecting to nothing, which will keep the gate voltage stable. When modulating the falling edge, the high level signal means connecting to the negative driving voltage $v_{ge,off}$ and the low level signal means connecting to nothing.

  - The method is more complicated because of its separate control of positive and negative driving voltages, but it can solve the pseudo turn-on problem.

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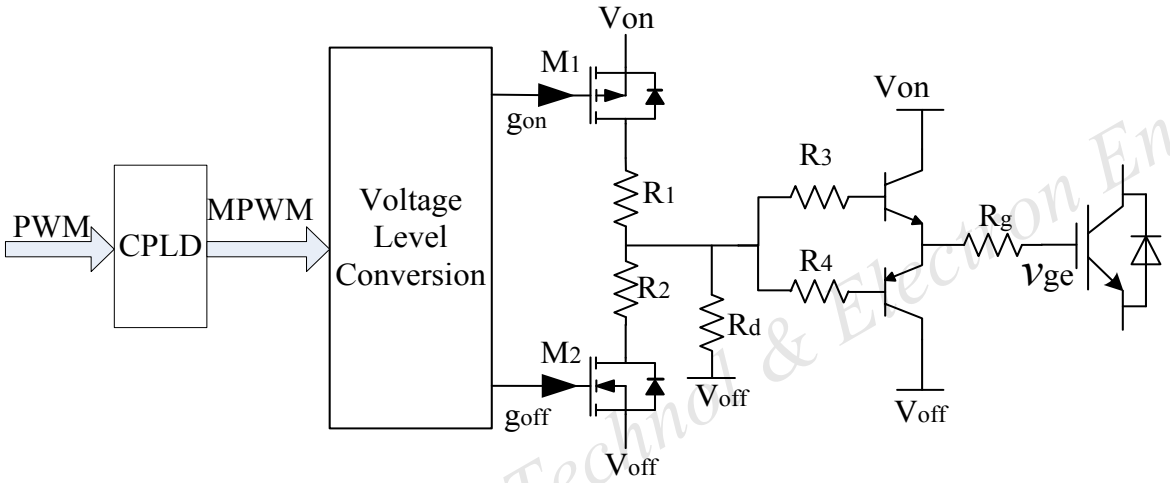
# Method (con'd)

- Concrete driving circuit using CPLD

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– Under the BPTM operation mode, MOSFET1 and MOSFET2 switch on and off alternately to modulate the driving pulse edge.

– Under the UPTM operation mode, only one MOSFET switches on and off to modulate the driving pulse edge, and the other MOSFET's driving signal is blocked.

# Major results

(1) The gate voltage increases with serration using the BPTM method, and the gate voltage increases without a falling segment using the UPTM method.

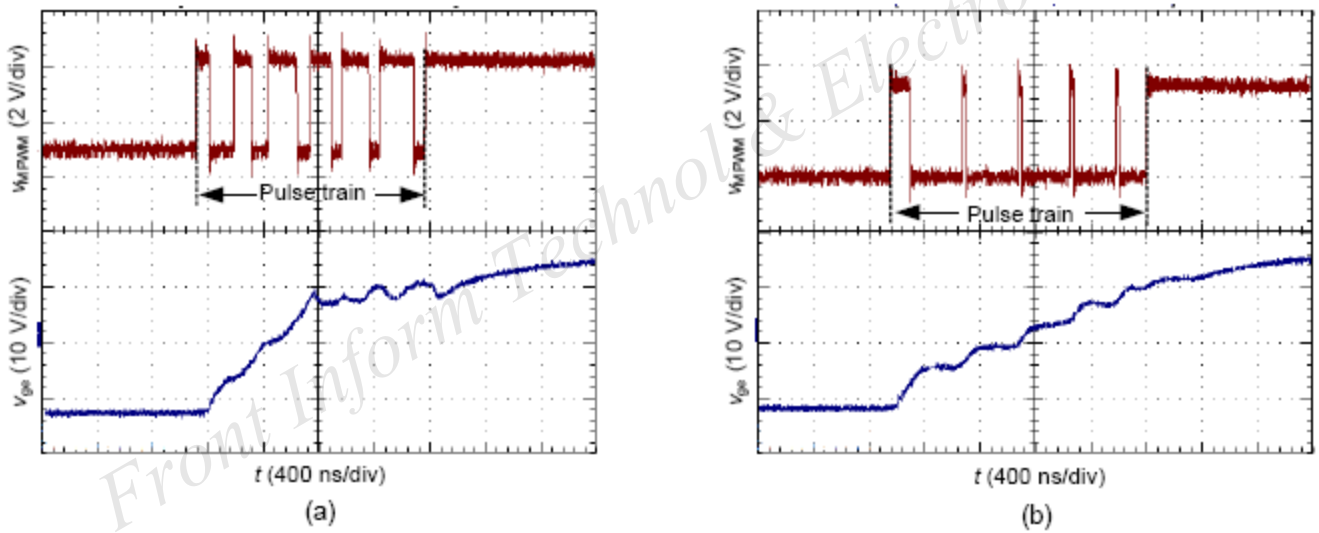


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**Fig. 11 MPWM signals and IGBT gate voltage with additional pulses during the turn-on period: (a) BPTM; (b) UPTM**

# Major results (Con'd)

(2) Compared with the traditional driving method, the gate voltage using these two methods rise slowly, especially with the UPTM method.

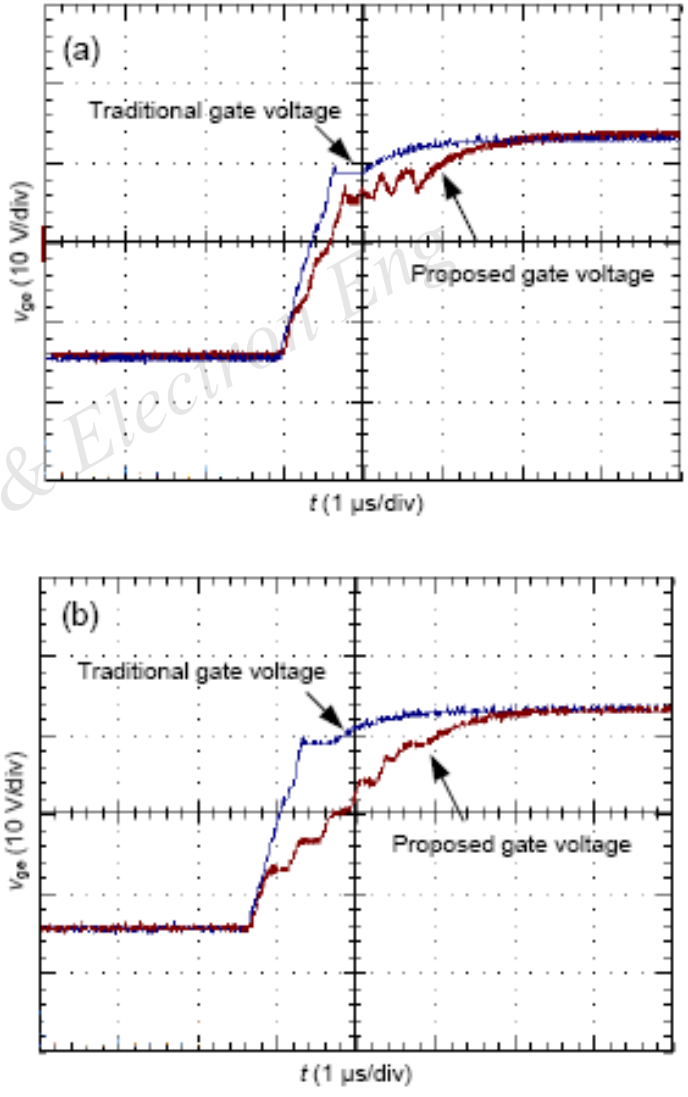


**Fig. 12 Waveforms of IGBT gate voltages before and after adopting the pulse edge modulation technique: (a) BPTM; (b) UPTM**

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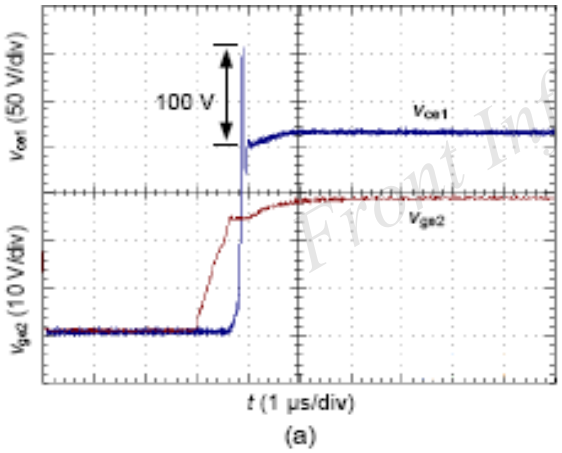
# Major results (Con'd)

(3) After using the two driving pulse edge modulation methods, the collector-emitter voltage spike of complementary transistor was almost zero when the IGBT turns on at a high speed.



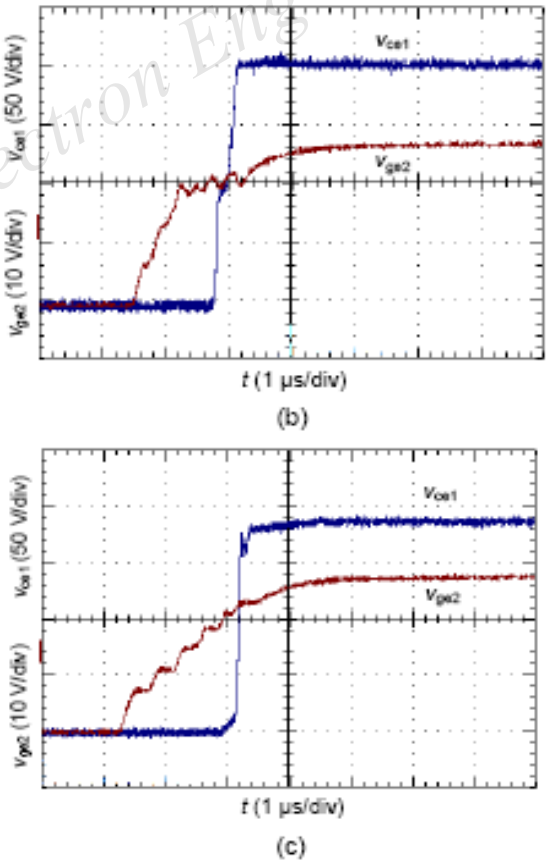




**Fig. 13** Waveforms of the IGBT gate voltage of $Q_2$ and collector-emitter voltage of $Q_1$: (a) TDS; (b) BPTM; (c) UPTM

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# Major results (Con'd)

(4) Pseudo turn-on problem with BPTM method :

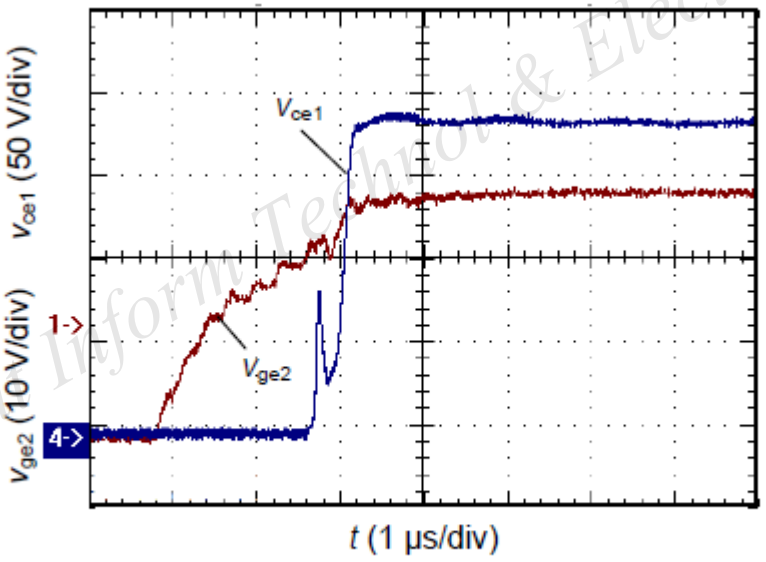


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**Fig. 14 Pseudo turn-on problem with the BPTM method**

# Major results (Con'd)

(5) The waveforms of collector-emitter voltage, collector current, and device power dissipation during IGBT turn-on and turn-off periods with the three different drive conditions:
Using the proposed BPTM technique, the switching voltage spike totally disappeares and the reverse current is much smaller. Furthermore, the turn-off power dissipation is further reduced. However, in spite of the smaller collector current, the total turn-on power loss is larger on account of the slow conduction process.

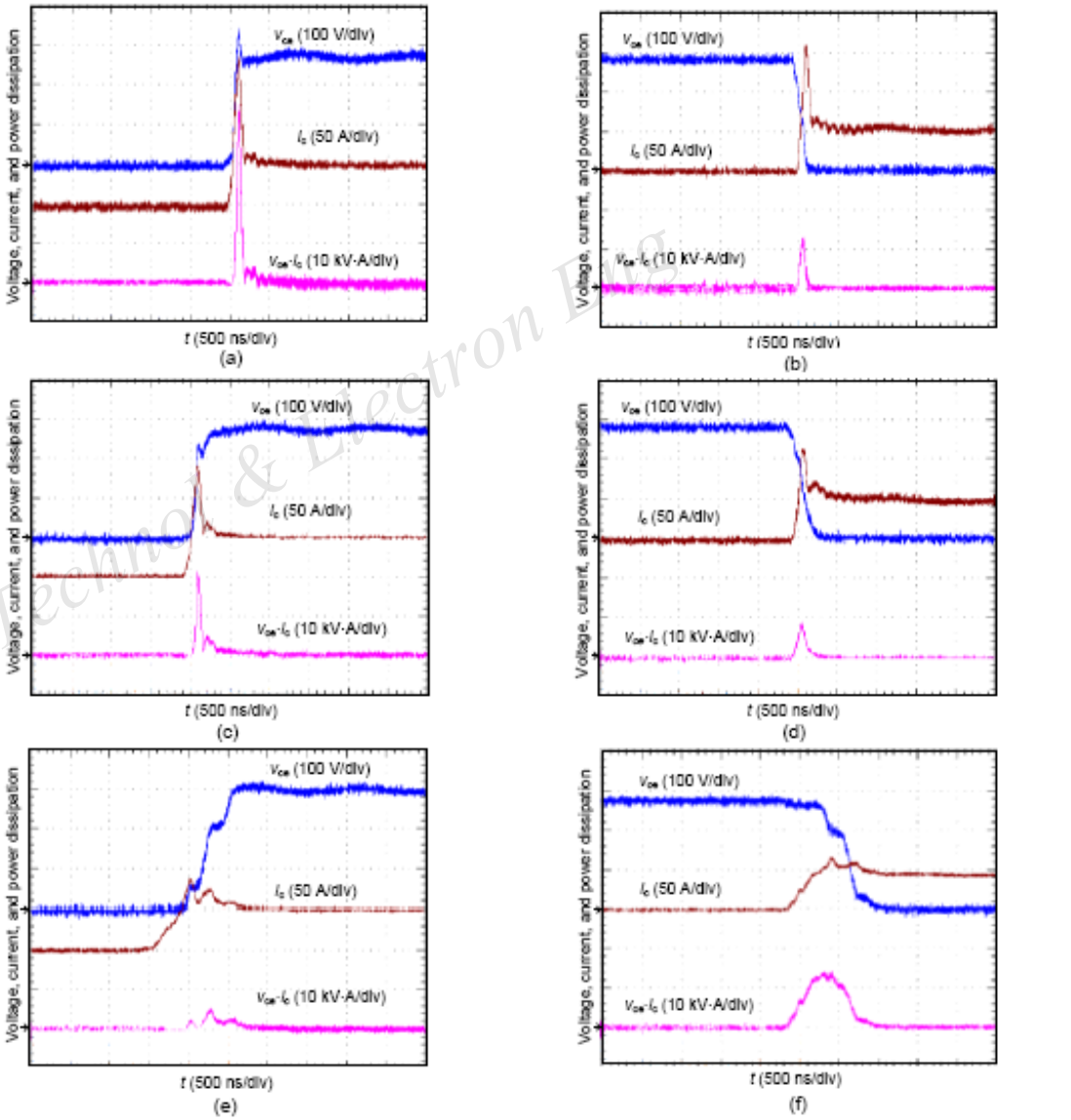


Fig. 15 Waveforms of the IGBT collector-emitter voltage, collector current, and power dissipation during the turn-on period (right column) and turn-off period (left column) using a traditional driver with small gate resistance ((a) and (b)), a traditional driver with large turn-on gate resistance ((c) and (d)), and our proposed pulse edge modulation technique ((e) and (f))

# Conclusions

A new driving pulse edge modulation technique based on a digital driver for regulating the IGBT turn-on and turn-off speed is introduced. The main features can be summarized as follows:

1. Modulation can be achieved totally by using digital techniques and can be used in different working conditions without changing the structure of drive circuits.

2. Only one CPLD (or FPGA) is used and no specific properties are required.

3. The pseudo turn-on problem can be solved by using the UPTM method, and the low requirement on the response speed of the driving circuit gives it better applicability.

4. The method is flexible in application due to its digitalization.

Future work will address further practical applications of the proposed gate driver.

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