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A V-band high-linearity BiCMOS mixer with robust temperature tolerance*

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Abstract: A high-linearity down mixer with outstanding robust temperature tolerance for V-band applications is proposed in this paper. The mixer's temperature robustness has been greatly enhanced by employing a negative temperature-compensation circuit (NTC) and a positive temperature-compensation circuit (PTC) in the transconductance (g_m) stage and intermediate frequency (IF) output buffer, respectively. Benefiting from the active balun with enhanced g_m and emitter negative feedback technique, the linearity of the mixer has been significantly improved. For verification, a double-balanced V-band mixer is designed and implemented in a 130 nm SiGe BiCMOS process. Measured over the local oscillator (LO) bandwidth from 57 GHz to 63 GHz, the mixer demonstrates a peak conversion gain (CG) of −0.5 dB, a minimal noise figure (NF) of 11.5 dB, and an input 1 dB compression point ($IP_{1\,dB}$) of 4.8 dBm under an LO power of −3 dBm. Furthermore, the measurements of CG, NF, and $IP_{1\,dB}$ exhibit commendable consistency within the temperature range of −55 ℃ to 85 ℃, with fluctuations of less than 0.8 dB, 1 dB, and 1.2 dBm, respectively. From 57 GHz to 63 GHz, the measured LO-to-radio frequency (RF) isolation is better than 46 dB, the measured return loss at the RF port is >29 dB, and at the LO port it exceeds 12 dB. With a 2.5 V supply voltage, the mixer power consumption is 15.75 mW, 18.5 mW, and 21 mW at temperatures of −55 ℃, 25 ℃, and 85 ℃, respectively. Moreover, the mixer chip occupies a total silicon area of 0.56 mm^2 including all testing pads.

Key words: V-band; Down-conversion mixer; SiGe BiCMOS; Temperature compensation; High-linearity; Active balun
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1 Introduction

Recently, there has been a growing demand for various wireless applications with high data rates and large bandwidth in the V-band (40–75 GHz), such as short-range ultra-high-speed communication (Sutbas et al., 2022; Vardarli et al., 2022), wireless backhaul communication (Mazor et al., 2017), and radar detection (Inanlou et al., 2014; Longhi et al., 2020; Cui et al., 2023), which have attracted widespread attention from academia and industry. Specifically, the 60 GHz band falls within the unlicensed spectrum for commercial wireless communication and is utilized in the WiGig standard (IEEE 802.11ad) (Mazor et al., 2017). It supports multi-gigabit-per-second wireless communication applications, including wireless personal area networks (WPANs) and wireless local area networks (WLANs). In these scenarios, high-performance wireless hardware is essential for achieving the optimal utilization of spectrum resources. As a critical foundational component

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of receivers, down-conversion mixers transform radio frequency (RF) signals into intermediate frequency (IF) or baseband (BB) signals. With the continuous reduction in device size, the silicon germanium (SiGe) BiCMOS process has emerged as a formidable contender against gallium arsenide (GaAs), indium phosphide (InP), and other III–V group compound semiconductor technologies, because it enables cost-effective, highly integrated, and mass-produced millimeter wave (mm-wave) integrated circuits (ICs) (Chen et al., 2020). However, the behavior of silicon-based mixers, including metrics like conversion gain (CG), noise figure (NF), and linearity, can exhibit significant fluctuations with varying ambient temperatures, thereby directly causing deterioration of receiver sensitivity and dynamic range. Therefore, it is highly anticipated that the mixers exhibit excellent robustness against temperature variation.

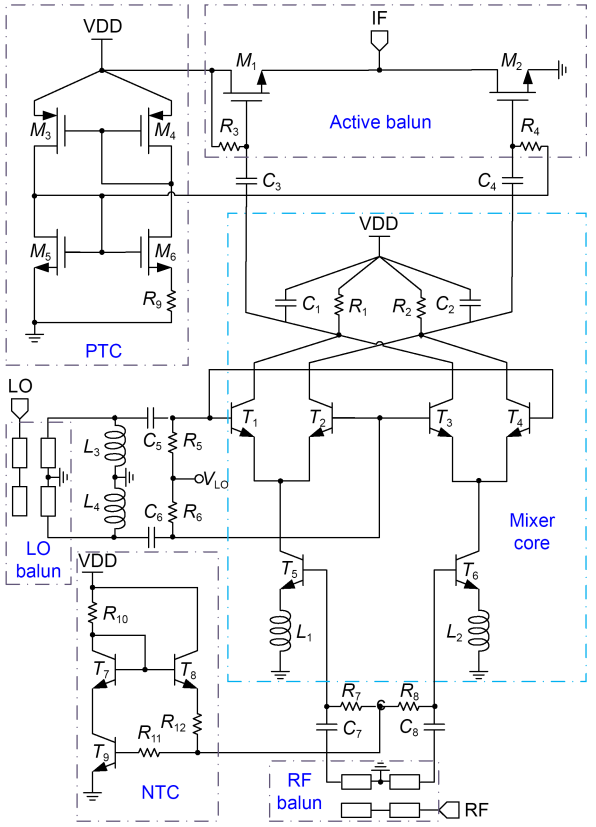
Many articles focus on mixers that achieve high CG, suppress noise, improve image rejection, and so on (Chou et al., 2012; Kim et al., 2012; Wei et al., 2012; Chiou et al., 2013; Wu et al., 2015; Chi and Chuang, 2016; Kolios and Kalivas, 2016; Choi et al., 2017; Ciocoveanu et al., 2018, 2019a, 2019b; Liu et al., 2018; Kashani et al., 2019; Yu and Kang, 2020; Ahmed et al., 2021; Krishnamurthy et al., 2021; Duan et al., 2023; Yu et al., 2024). In the literature, some publications have reported mixers with temperature-insensitive characteristics. In Yu et al. (2024), a novel passive double-balanced ring structure was employed in a 60–90 GHz mixer-first receiver, achieving high linearity and low local oscillator (LO) leakage. Additionally, two temperature-compensation circuits were implemented for the mixer core and IF amplifier, significantly improving the temperature robustness of the receiver. The fabricated prototype supported a wide temperature range from −20 ℃ to 100 ℃, with CG, 1 dB input compression point ($IP_{1\,dB}$), and NF variations of less than 1.6 dB, 1.0 dBm, and 2.9 dB, respectively. Mazor et al. (2017) reported a highly linear 60 GHz BiCMOS down-conversion mixer with an attenuation mode. For non-attenuation mode, it exhibited a tested CG of 6 dB, a tested input third-order intercept point (IIP3) of 10 dBm, and a tested NF of 12 dB. Despite incorporating temperature bias circuits, the CG, NF, and IIP3 of the mixer still varied by 2.7 dB, 1.9 dB, and 6.1 dBm, respectively, over the temperature range of −40 ℃ to 85 ℃. To improve process–voltage–temperature (PVT) variations, Ciocoveanu et al. (2018) exploited a self-biasing V_{th} tracking circuit to apply a 60 GHz modified Gilbert-cell mixer fabricated in a 28 nm complementary metal-oxide-semiconductor (CMOS) technology. The prototype exhibited a CG of 4.7 dB, an $IP_{1\,dB}$ of −3 dBm, and an NF of 12.3 dB. The observed changes in the mixer's CG, $IP_{1\,dB}$, and NF by 3.6 dB, 2.4 dBm, and 2.7 dB, respectively, across the temperature range of −30 ℃ to 120 ℃, indicates considerable room for improvement. More recently, a 76–81 GHz transceiver with bidirectional mixer was designed for automotive radar applications (Duan et al., 2023). By employing multiple temperature-compensation techniques, this mm-wave transceiver chip demonstrated good temperature robustness ranging from −45 ℃ to 125 ℃, achieving an NF of 11.2 dB, an $IP_{1\,dB}$ of −7 dBm, and an output power of 14.5 dBm. Several V-band mixers developed in the CMOS technology have been reported (Chou et al., 2012; Wei et al., 2012; Chiou et al., 2013; Choi et al., 2017; Kashani et al., 2019; Krishnamurthy et al., 2021). A down-conversion mixer operating at 60 GHz was developed employing active balun and transconductance linearization methods (Choi et al., 2017). The mixer delivered a CG of 5.6 dB, an $IP_{1\,dB}$ of −7 dBm, an output third-order intercept point (OIP3) of 12.4 dBm, and an NF of 10.9 dB. Kashani et al. (2019) reported a V-band low-noise mixer-first architecture. A revised single-balanced configuration served as the mixer's core, enhancing both the CG and NF while maintaining power efficiency and linearity. The fabricated mixer achieved a maximum CG of 12.1 dB, a minimum NF of 6.5 dB, an $IP_{1\,dB}$ of −5 dBm, and a low core power consumption of 3 mW. Some other high linearity silicon mixers were reported. They achieved an $IP_{1\,dB}$ of −7 dBm (Chou et al., 2012), −6 dBm (Wei et al., 2012), −1 dBm (Chiou et al., 2013), and −2 dBm (Krishnamurthy et al., 2021). Based on the literature mentioned above, the main challenge in designing high-performance mm-wave mixers lies in balancing the trade-off between CG, NF, linearity, and power consumption under wide temperature operating conditions. Therefore, there is a significant demand for new approaches that can achieve robust overall performance while being insensitive to temperature variations.

In this study, a V-band down-conversion mixer is designed and implemented using a 130 nm SiGe

BiCMOS process. A negative temperature-compensation circuit (NTC) and a positive temperature-compensation circuit (PTC) are respectively applied to the mixer's transconductance (g_m) stage and IF output buffer to achieve excellent wide temperature tolerance. The incorporation of emitter negative feedback and active balun with enhanced g_m greatly improves the mixer's linearity. The proposed design techniques have been validated in a V-band mixer, demonstrating excellent temperature robustness and high linearity. This paper is organized as follows: Section 2 focuses on the design and implementation of the V-band mixer; Section 3 presents the measurement results to validate the design; conclusions are presented in Section 4.

2 Circuit analysis and design

Fig. 1 illustrates the architecture of the proposed V-band down-conversion mixer, featuring a double-balanced Gilbert-cell mixer core, an output IF buffer equipped with an active balun, a PTC module, an NTC module, and two Marchand RF/LO baluns. RF/LO baluns perform single-to-differential rotation and ensure 50 Ω matching at the input ports RF/LO. The mixer core employs a double-balanced Gilbert cell, primarily consisting of the switch stage, g_m stage with inductive degeneration, and resistor and capacitor (RC) load stage. The switch stage consists of two pairs of NPN-type heterojunction bipolar transistors (HBTs), T_1 and T_2 and T_3 and T_4, driven by a differential LO signal. The two pairs of HBTs operate at low overdrive voltages, thereby reducing the required LO injection power. The g_m stage comprises two HBTs T_5 and T_6 along with two negative feedback inductors L_1 and L_2. This implementation improves linearity and expands the bandwidth. The load stage is composed of two parallel RC pairs, namely R_1 and R_2 and C_1 and C_2, which effectively filter out high-frequency interference and enhance LO suppression at the IF terminal. The active balun composed of n-type metal-oxide-semiconductor field-effect transistors (NMOSFETs) M_1 and M_2 serves as a differential-to-single IF output buffer, while further enhancing the linearity of the mixer. To achieve wide temperature operation characteristics, two temperature-compensation circuits are employed. An NTC module is utilized to generate a negative temperature coefficient



M_1, M_2	256 μm/1.2 μm	T_8	120 nm/16 μm	R_{11}, R_{12}	3.2 kΩ/670 Ω
M_3	4.8 μm/1 μm	T_9	120 nm/5.5 μm	C_1, C_2	500 fF
M_4	4 μm/1 μm	R_1, R_2	146 Ω	C_3, C_4	30 pF
M_5	2 μm/1 μm	R_3, R_4	569 kΩ	C_5, C_6	260 fF
M_6	16 μm/1 μm	R_5, R_6	519 Ω	C_7, C_8	200 fF
T_1–T_6	120 nm/4 μm	R_7, R_8	187 Ω	L_1, L_2	115 pH
T_7	120 nm/520 nm	R_9, R_{10}	13.6 kΩ/1.4 kΩ	L_3, L_4	90 pH

Fig. 1 Schematic of the proposed V-band mixer

bias current, applied to the base nodes of g_m stages T_5 and T_6 through bias resistors R_7 and R_8, achieving temperature compensation for its g_m. Additionally, a PTC circuit is used to output a positive temperature coefficient bias voltage, applied to the active balun, thereby effectively compensating for the output IF buffer. Fig. 1 displays the optimized dimensions of the key active devices and the values of passive elements for the proposed mixer.

2.1 Negative temperature coefficient compensation circuit

Due to inherent factors of silicon-based processes, characteristics of active devices such as g_m and threshold voltage vary with environmental temperature changes. As depicted in Fig. 2, in the absence of temperature-compensation circuits, the mixer's CG

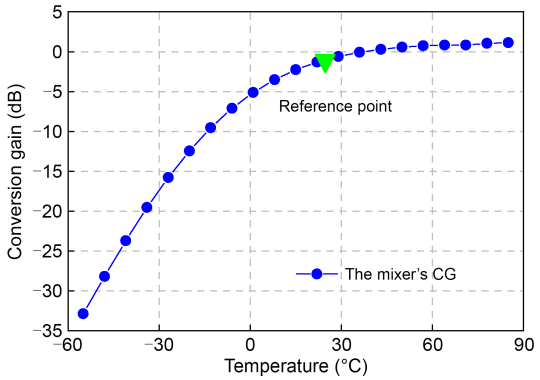


Fig. 2 Simulated results of conversion gain (CG) versus temperature variation

sharply increases with temperature elevation and eventually stabilizes.

Compared with MOSFET devices, HBT devices are more sensitive to temperature variations. Therefore, the first consideration is to introduce a compensation circuit in the g_m stage composed of T_5 and T_6. As shown in Fig. 3, the collector current of the g_m stage transistors increases significantly with ambient temperature. CG is directly associated with the collector current. Thus, temperature compensation for CG can be achieved by generating a negative temperature coefficient base current to reduce the fluctuation of the collector current (Razavi, 2000). Based on this idea, Fig. 4 outlines the design process for implementing a temperature-compensation circuit through a three-step procedure.

As illustrated in Fig. 5, the circuit is implemented using transistors T_1–T_3 and resistors R_1–R_2. The derivation of NTC is as follows. The collector current for the HBT device T_3 can be expressed as follows:

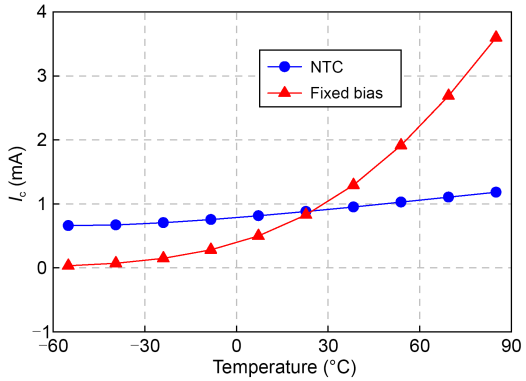


Fig. 3 Simulated collector current of g_m stage transistors versus temperature variation

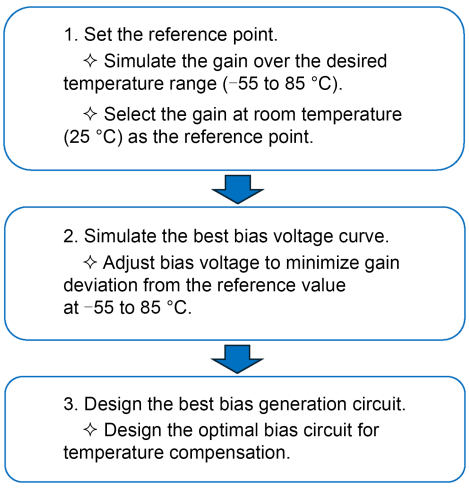


Fig. 4 The three-step process for designing a temperature-compensation circuit

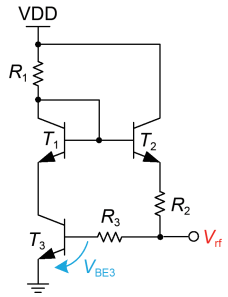


Fig. 5 The proposed negative temperature coefficient compensation circuit

$$I_{c3} = I_{s3} \exp\left(\frac{V_{BE3}}{V_T}\right), \tag{1}$$

where $V_T=KT/q$, and the saturation current $I_{s3}\propto\mu KTn_i^2$. Here, K is the Boltzmann constant, T is the temperature in Kelvin, q is the charge carried by a single electron, μ represents the carrier mobility, and n_i denotes the intrinsic carrier concentration of silicon. The relationship between these parameters and the temperature can be expressed as $\mu\propto\mu_0 T^2$, and $n_1^2\propto T^3\exp\left(\frac{-E_g}{KT}\right)$. In this design, the E_g of HBT is approximately 1 eV, and the saturation current can be represented as

$$I_{s3} = bT^{4+m} \exp\left(\frac{-E_g}{KT}\right), \tag{2}$$

where b is a proportional factor, $m\approx-1.5$, and the output voltage V_{rf} can be written as

$$V_{\mathrm{rf}} = V_{\mathrm{BE3}} = V_T \ln\left(\frac{I_{\mathrm{c3}}}{I_{\mathrm{s3}}}\right). \tag{3}$$

The output voltage V_{rf} is determined by the voltage between the base and the emitter of transistor T_3. To simplify the analysis, we can temporarily assume that I_{c3} remains unchanged, as follows:

$$\frac{\partial V_{\mathrm{BE3}}}{\partial T} = \frac{\partial V_T}{\partial T}\ln\left(\frac{I_{\mathrm{c3}}}{I_{\mathrm{s3}}}\right) - \frac{V_T}{I_{\mathrm{s}}}\frac{\partial I_{\mathrm{s3}}}{\partial T}. \tag{4}$$

The partial derivative of saturated current in Eq. (2) is

$$\frac{\partial I_{\mathrm{s3}}}{\partial T} = bT^{3+m}\exp\left(\frac{-E_g}{KT}\right)\left(4+m+\frac{E_g}{KT}\right). \tag{5}$$

Based on Eqs. (4) and (5), the partial derivative of the output voltage with respect to temperature is

$$\frac{\partial V_{\mathrm{rf}}}{\partial T} = \frac{V_{\mathrm{BE3}} - (4+m)V_T - \dfrac{E_g}{q}}{T}. \tag{6}$$

Eq. (6) provides the temperature coefficient of the voltage difference between the base and the emitter, namely the output voltage V_{rf}, at a given temperature. From this equation, we can observe its dependency on V_{BE3}. When V_{BE3}≈820 mV and T=300 K, the temperature coefficient is around −0.8 mV/°C. As plotted in Fig. 6, the output voltage V_{rf} exhibits negative temperature characteristics, consistent with the derivation mentioned above. By utilizing the designed NTC, the output voltage V_{rf} gradually decreases as the temperature rises. The V_{rf} is applied to the g_m stage, effectively suppressing the increase in collector currents of transistors T_5 and T_6. Fig. 3 illustrates the variation trends of the collector currents of transistors T_5 and T_6 with or without an NTC. Consequently, this achieves temperature compensation for the g_m stage.

2.2 Positive temperature coefficient compensation circuit

Due to intrinsic factors within the NMOSFET device, g_m of the NMOSFET devices decreases with increasing temperature, thereby reducing the gain of the output IF buffer (Wang et al., 2024). By increasing the bias voltage of the NMOSFET transistors, g_m can be enhanced to compensate for the gain.

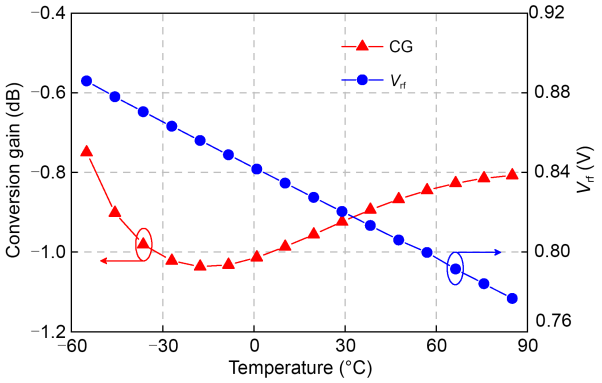


Fig. 6 Simulated results of temperature variation versus CG and output voltage V_{rf}

The proposed PTC, as depicted in Fig. 7a, represents a self-biased current source generation circuit. It comprises a linear current source formed by P-channel MOSFET (PMOSFET) transistors $\mathrm{MP_3}$ and $\mathrm{MP_4}$ and a nonlinear current source constituted by NMOSFET transistors $\mathrm{MN_1}$ and $\mathrm{MN_2}$ along with the resistor R. The ratio of width to length between $\mathrm{MP_3}$ and $\mathrm{MP_4}$ is K:1, and the ratio of width to length between $\mathrm{MN_2}$ and $\mathrm{MN_1}$ is N:1, with both K and N being >1.

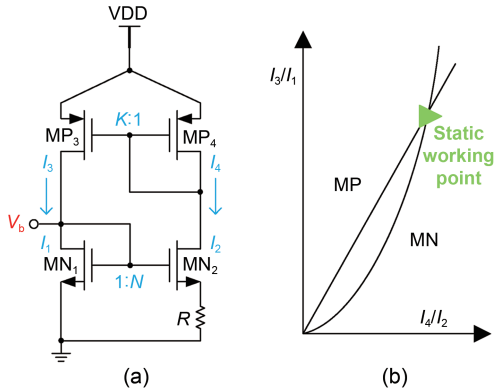


Fig. 7 Positive temperature coefficient compensation circuit (a) and static working point (b)

The static working point diagram of the self-biased current source circuit is shown in Fig. 7b. The line MP represents the current variation on $\mathrm{MP_3}$ and $\mathrm{MP_4}$ in the linear current source, with a slope equal to the current ratio K:1 of $\mathrm{MP_3}$ to $\mathrm{MP_4}$. The curve MN represents the current variation on $\mathrm{MN_2}$ and $\mathrm{MN_1}$ in the nonlinear current source, with a slope equal to the reciprocal of the current ratio of $\mathrm{MN_2}$ to $\mathrm{MN_1}$. This

slope variation includes both positive and negative feedback. Initially, the current in the branch is very small, and the voltage drop across the resistor R can be neglected. MN_2 copies the current from MN_1 to the right branch in an N:1 ratio, and then MP_3 copies the current from MP_4 to the left branch in a K:1 ratio, which constitutes positive feedback. As the current increases, the voltage drop across the resistor cannot be ignored. The resistor starts to provide negative feedback, weakening the ability of MP_3 to replicate the current. Eventually, MP and MN will have two intersection points, and the non-zero intersection point is called the static working point.

The ratio of the current in the left branch to the current in the right branch is K:1. Neglecting the body effect and assuming the current in the right branch is I, the formula for the current–voltage relationship in the saturation region of the left branch is

$$KI = \frac{1}{2}\mu C_{ox}(W/L)_1(V_{GS1} - V_{TH})^2. \tag{7}$$

From Eq. (7), we can obtain

$$V_{GS1} = \sqrt{\frac{2KI}{\mu C_{ox}(W/L)_1}} + V_{TH}. \tag{8}$$

According to Kirchoff's voltage law (KVL) equation, we can write

$$V_{GS1} = V_{GS2} + IR, \tag{9}$$

which gives

$$\sqrt{\frac{2KI}{\mu C_{ox}(W/L)_1}} + V_{TH} = \sqrt{\frac{2I}{\mu C_{ox}(W/L)_2}} + V_{TH} + IR, \tag{10}$$

$$I = \frac{2}{\mu C_{ox}(W/L)_1}\frac{1}{R^2}\left(\sqrt{K} - \frac{1}{\sqrt{N}}\right)^2. \tag{11}$$

By combining Eq. (7) and taking the partial derivative with respect to temperature T, we can obtain

$$\frac{\partial V_b}{\partial T} = \frac{\partial V_{GS1}}{\partial T} = \frac{2Km\left(1 - \frac{1}{\sqrt{KN}}\right)\left(\frac{T}{T_0}\right)^{-m-1}}{\mu(T_0)T_0C_{ox}(W/L)_1R} + \frac{\partial V_{TH}}{\partial T}, \tag{12}$$

where m lies in the range 1.5–2.0, $\mu(T_0)$ represents the mobility of charge carriers at a reference temperature T_0, and $(W/L)_1$ and $(W/L)_2$ refer to the width-to-length ratios of the NMOSFET transistors MN_1 and MN_2 in Fig. 7, respectively. The left term in the equation is >0. By selecting appropriate values for K, N, and R, the positive temperature-compensation bias voltage shown in Fig. 8 can be obtained. As shown in Fig. 8, the PTC generates an output voltage that increases as the temperature rises to compensate for the g_m of the buffer, thereby stabilizing the CG.

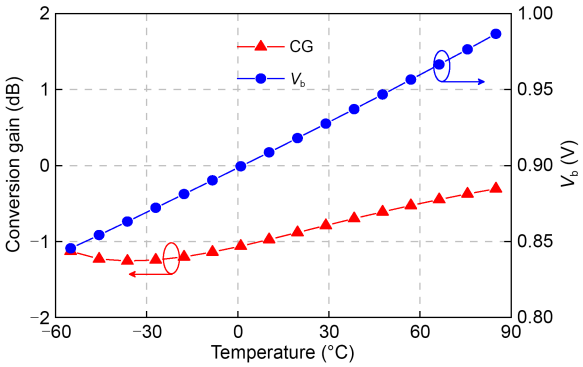


Fig. 8 Simulated results of temperature versus CG and the bias voltage

2.3 Active balun

The active balun proposed in Fig. 9a serves as an output IF buffer while converting from differential to single-ended signals, achieving impedance matching and high linearity simultaneously. To ensure good linearity, both transistors M_1 and M_2 are required to operate in saturation. The equivalent small-signal model of the active balun is shown in Fig. 9b. By analyzing the small-signal model, the current can be calculated as follows:

$$\begin{aligned} I_1 &= g_{m1}V_{GS1} + \frac{V_{GS1}}{r_{o1}} = -g_{m1}V_{if} - \frac{V_{if}}{r_{o1}}, \\ I_2 &= g_{m2}V_{GS2} + \frac{V_{GS2}}{r_{o2}} = g_{m2}V_{if} + \frac{V_{if}}{r_{o2}}. \end{aligned} \tag{13}$$

The output current can be expressed as

$$I_{out} = I_1 - I_2 = -V_{if}\left(g_{m1} + g_{m2} + \frac{1}{r_{o1}} + \frac{2}{r_{o2}}\right), \tag{14}$$

where g_{m1} and g_{m2} represent transconductance of MOS transistor M_1 and M_2, respectively, r_{o1} and r_{o2} represent

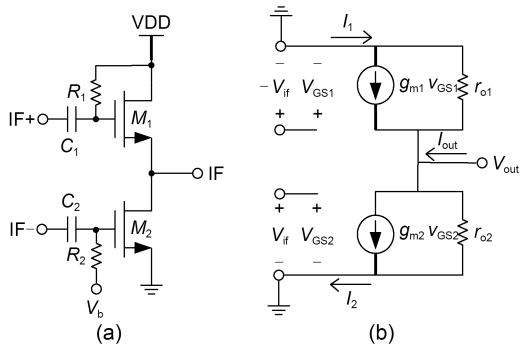


Fig. 9 Schematic of active balun (a) and its small-signal equivalent model (b)

output resistance of MOS transistor M_1 and M_2, respectively, and V_{if} represents input voltage signal at IF. As demonstrated in Eq. (14), the common source and common drain configuration are employed to enhance the output current I_{out} and the output voltage swing, thus improving the linearity.

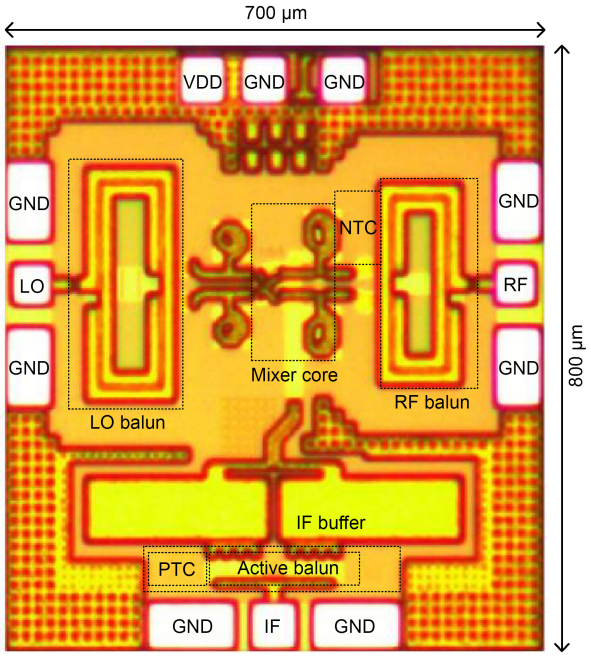


Fig. 10 Die micrograph of the proposed V-band mixer

3 Experimental results and discussion

The proposed V-band double-balanced down-conversion mixer with excellent temperature robustness is designed and fabricated in a 130 nm SiGe BiCMOS, which is a high-performance technology that is compatible with the 130 nm CMOS process. The NPN-type HBT transistor for RF applications achieves a cutoff frequency f_T around 260 GHz and a maximum oscillation frequency f_{MAX} around 320 GHz. To achieve more accurate performance of the mixer, passive components, including baluns, inductors, capacitors, testing pads, interconnections, and vias, are optimized through a full-wave three-dimensional electromagnetic field simulator and circuit co-simulations. A die microphotograph of the V-band mixer chip is shown in Fig. 10. The whole chip area including two on-chip transformer baluns and all testing pads is 0.56 mm^2.

Utilizing a probe station (MPI TS200-SE) equipped with ground–signal–ground (G–S–G) probes with a pitch of 150 μm, on-wafer *S*-parameter measurements are conducted within the 57–63 GHz frequency range. This setup is complemented by a Keysight PNA-X-N5247B network analyzer, supporting NF applications, and a Keysight N6705C DC power analyzer renowned for its high resolution. Calibration is achieved through the standard short-open-load-through (SOLT) method. The proposed mixer's temperature characterization employs the AC3 Fusion thermal chuck system from ERS electronic GmbH to regulate the ambient temperature of the probe station. It accommodates operating temperatures ranging from −65 ℃ to 400 ℃, offering a temperature accuracy of ±0.1 ℃ and a display resolution of 0.01 ℃.

Fig. 11 illustrates the simulated and measured variations of CG versus LO frequency for the mixer at temperatures of −55 ℃, 25 ℃, and 85 ℃. With the IF frequency fixed at 0.1 GHz, the RF frequency ranges from 56.9 GHz to 62.9 GHz, while the LO

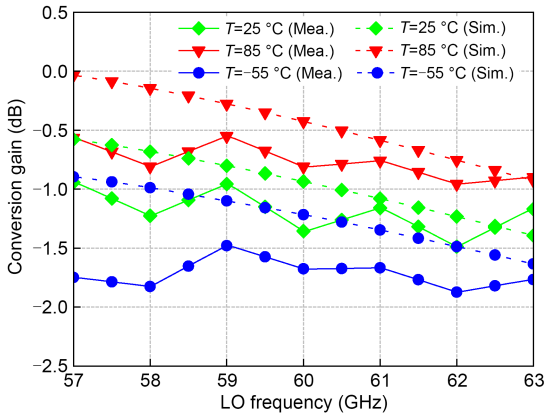


Fig. 11 Measured (Mea.) and simulated (Sim.) CG under −55 ℃, 25 ℃, and 85 ℃

frequency under −3 dBm injection power varies from 57 GHz to 63 GHz. It can be seen that the CG variation remains less than ±0.4 dB from 57 GHz to 63 GHz, corresponding to ±0.0028 dB/℃. The consistency among these measured data indicates the effectiveness of the proposed temperature-compensation technique. The simulated and measured results exhibit good agreement.

The Keysight PNA-X-N5247B network analyzer, equipped with NF functionality, is also employed to evaluate the NF metrics of the mixer chip. In Fig. 12, the simulated and measured NF results are depicted. Within the target frequency range of 57–63 GHz, the measured NFs demonstrate good flatness, with variations of <1 dB. For instance, at room temperature (25 ℃), the measured NF increases from 11.5 dB to 12 dB. Across all test temperatures, the variation in NF is better than ±0.5 dB. The power-handling capability with the LO frequency from 57 GHz to 63 GHz of the mixer is presented in Fig. 13. Benefiting from the employed emitter negative feedback and active balun technology with transconductance enhancement, the measured $IP_{1\,dB}$ exceeds 3.9 dBm within the frequency band of interest, while the variation in $IP_{1\,dB}$ at different operating temperatures is less than ±0.6 dBm. All measurements presented previously are conducted within a temperature range from −55 ℃ to 85 ℃.

The measured isolation from the LO port to the RF port and the return losses at the LO and RF ports are depicted in Fig. 14. It is evident that the isolation between the LO and RF ports exceeds 46 dB within the bandwidth of 57–63 GHz. Within the measured frequency range of interest, the measured return loss

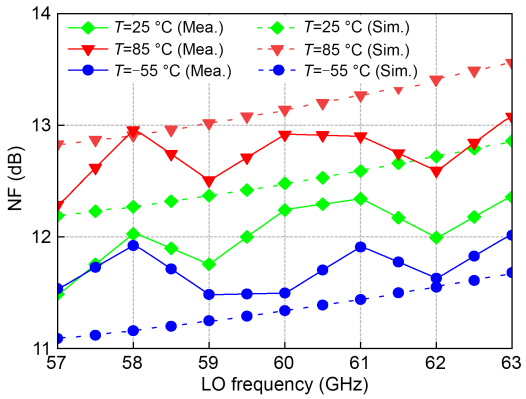


Fig. 12 Measured and simulated noise figure (NF) under −55 ℃, 25 ℃, and 85 ℃

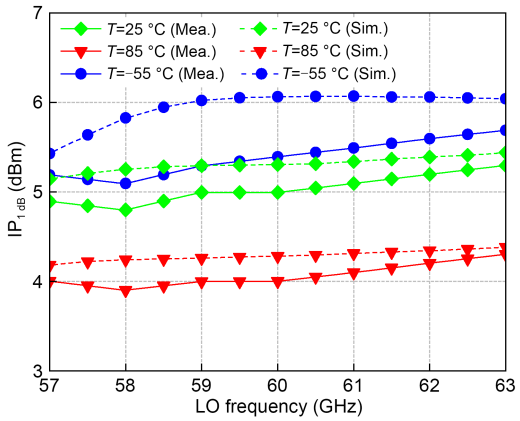


Fig. 13 Measured and simulated input 1 dB compression point ($IP_{1\,dB}$) under −55 ℃, 25 ℃, and 85 ℃

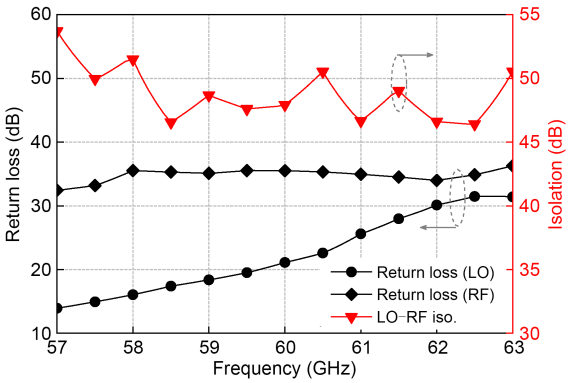


Fig. 14. Measured return loss and isolation (iso.) for local oscillator (LO) frequencies from 57 to 63 GHz

at the RF port is better than 29 dB, while at the LO port, it is >12 dB. Operating at a supply voltage of 2.5 V, the mixer exhibits DC power consumption of 15.75 mW, 18.5 mW, and 21 mW at temperatures of −55 ℃, 25℃, and 85 ℃, respectively.

Table 1 summarizes the performance of the proposed V-band mixer and recently reported CMOS/SiGe BiCMOS mixers. The proposed mixer demonstrates outstanding temperature robustness by incorporating PTC and NTC techniques, allowing it to maintain excellent overall performance under wide temperature operation. Within the temperature range of −55 ℃ to 85 ℃, the measured CG, NF, and $IP_{1\,dB}$ variations are better than 0.8 dB, 1 dB, and 1.2 dBm, respectively. Compared with the recently reported mixers, the proposed mixer exhibits competitive performance of wide temperature characteristics, high linearity, and low power consumption.

Table 1 Performance summary and comparison with the recently reported mixers

Reference	Temperature (℃)	Process	Frequency (GHz)	P_{LO} (dBm)	CG (dB)	NF (dB)	$IP_{1\ dB}$ (dBm)	LO–RF iso. (dB)	Power (mW)	Area (mm^2)
Mazor et al., 2017	−55–85	130 nm SiGe	57–66	0	6.1–8.8*	11.4–13.3*	−9.5–−3.4*	>46*	55^	0.47
Yu et al., 2024	−20–100	28 nm CMOS	60–90	N/A	16–18.4	7.5–11.2	−5–−4	>35.8	41.5^	0.46
Ciocoveanu et al., 2018	−30–120	28 nm CMOS	60	−2	2.9–6.5#	11–13.7#	−4.2–−1.8#	N/A	1.8^	0.24
Duan et al., 2023	−45–125	65 nm CMOS	76–83	N/A	26–68$	11.2–12.5	−7	N/A	N/A	0.85
This work	−55–85	130 nm SiGe	57–63	−3	−1.6–−0.8	11.5–12.5	4–5.2	>46	15.7–21	0.56

Post-layout simulation results, * chart estimation, ^ at room temperature, $ with low noise figure amplifier, N/A: no data

4 Conclusions

A positive and negative temperature-compensation technique is developed and successfully implemented in a V-band down-conversion mixer using a 130 nm SiGe BiCMOS process. This advancement enables the mixer to maintain consistent CG, NF, and linearity during large ambient thermal variation. In the temperature span from −55 ℃ to 85 ℃, the variations in CG, NF, and $IP_{1\ dB}$ measurements are all superior to 0.8 dB, 1 dB, and 1.2 dBm, respectively. The incorporation of emitter negative feedback and an active balun has greatly improved the mixer's linearity. Consequently, within the frequency range of 57–63 GHz, the measured $IP_{1\ dB}$ exceeds 5.1 dBm, 4.8 dBm, and 3.9 dBm at temperatures of −55 ℃, 25 ℃, and 85 ℃, respectively. Furthermore, at temperatures of −55 ℃, 25 ℃, and 85 ℃, the mixer consumes DC power of 15.75 mW, 18.5 mW, and 21 mW, respectively. The proposed mixer exhibits performance that is competitive with that of other mixers and therefore has potential as a building component for mm-wave ultra-high-speed communication transceivers.

Contributors

The conceptualization of the study was carried out by Jiang LUO and Yao PENG. The methodology was developed by Jiang LUO and Yizhao LI. The original draft of the manuscript was written by Yizhao LI, while the review and editing were performed by Jiang LUO, Yao PENG, and Qiang CHENG. The supervision of the project was provided by Yao PENG and Qiang CHENG. All the authors have reviewed and approved the final version of the manuscript for publication.

Conflict of interest

All the authors declare that they have no conflict of interest.

Data availability

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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