Frontiers of Information Technology & Electronic Engineering
www.jzus.zju.edu.cn; engineering.cae.cn; www.springerlink.com
ISSN 2095-9184 (print); ISSN 2095-9230 (online)
E-mail: jzus@zju.edu.cn

A stepless-power-reconfigurable converter for a constant current underwater observatory*

Yujia ZANG[1,2], Yanhu CHEN[†‡1], Canjun YANG[1], Haoyu ZHANG[1], Zhiyong DUAN[1], Gul MUHAMMAD[1]

[1]*State Key Laboratory of Fluid Power and Mechatronic Systems, Zhejiang University, Hangzhou 310027, China*

[2]*Ji Hua Laboratory, Foshan 528200, China*

[†]E-mail: yanhuchen@zju.edu.cn

Received May 27, 2021; Revision accepted Nov. 28, 2021; Crosschecked Dec. 9, 2021

Abstract: The conversion from constant current (CC) to constant voltage (CV) is one of the key technologies of CC underwater observatory systems. A shunt regulator with high stability and high reliability is usually used. Applications, however, are limited by high heat dissipation and low efficiency. In this paper, with an improved shunt regulation method, a novel concept of stepless power reconfiguration (SPR) for the CC/CV module is proposed. In cases with stable or slowly changing load, two modes of CC/CV conversion are proposed to reduce unnecessary power loss of the shunt regulator while being able to retain any operator-preset power margin in the system: (1) the manual SPR (MSPR) method based on single-loop control method; (2) the automatic SPR (ASPR) method based on inner-outer loop control method. The efficiency of the system is analyzed. How to select some key parameters of the system is discussed. Experimental results show that MSPR and ASPR are both effective and practical methods to reduce heat dissipation and improve the efficiency of the CC/CV module, while the high stability of the shunt regulator remains.

Key words: Constant current to constant voltage (CC/CV) conversion; Shunt regulator; Stepless power configuration; Underwater observatory

https://doi.org/10.1631/FITEE.2100259 **CLC number:** TP271

1 Introduction

In recent years, a cabled underwater observatory system has become one of the main methods of ocean observation owing to its compatible long-term, real-time, and in-situ properties (Chave et al., 2004; Asakawa et al., 2009; Qu et al., 2015). Constant current (CC) transmission mode and constant voltage (CV) transmission mode are widely applied (Kojima et al., 2005; Chen et al., 2012) for the cost-effective merit of the direct current transmission (Howe et al., 2002). The CC mode is widely used due to its inherent merit of short circuit tolerance (Asakawa et al., 2007; Chen et al., 2019b), while CV is required as the power supply of the scientific instruments used for ocean observation. Therefore, CC to CV (CC/CV) conversion technology has become one of the most critical technologies in the system.

1.1 Typical methods of CC/CV conversion

There are three common methods of CC/CV conversion: Zener diode, active shunt regulator with or without multi-module-stack method, and normal regulator.

In cases of low power applications, Zener diodes are used, a kind of passive shunt regulator, the simplest method (Kojima et al., 2005). Due to the inherent characteristics of CV output, using Zener diode greatly simplifies the manufacturing difficulty of CC/CV converter, which is widely used in the repeaters in a commercial submarine communication

‡ Corresponding author

* Project supported by the National Natural Science Foundation of China (No. 51979246) and the Ningbo Science and Technology Innovation 2025 Major Special Project, China (No. 2020Z075)

ORCID: Yujia ZANG, https://orcid.org/0000-0002-2712-9854; Yanhu CHEN, https://orcid.org/0000-0002-5020-7355

system, an underwater observatory node with relatively low power demand (Kanazawa et al., 2008, 2011), and maintenance systems in observatories (Chen et al., 2015, 2019a; Zhang et al., 2018). Note that a closed-loop direct current to direct current (DC/DC) module for further regulated voltage output may be incorporated into the system (Fig. 1a). However, enough dissipation is required in the Zener diode to ensure high stability of the system and the power capacity is difficult to reconfigure, leading to a challenging cooling system design if a large power is required, which results in a low power capacity of the CC/CV converter.

An active shunt regulator is one method to improve power capacity compared with the passive shunt regulator (Howe et al., 2011). A basic block diagram of a typical active shunt regulator is shown in Fig. 1b. One key component in the active shunt regulator is called balance-load (BL, also known as the "dummy load"). There also is a controller that controls the equivalent resistance of the BL. When the load is within the rated range, the controller controls the BL to make the sum of the load power and the power consumed by the BL to be a constant value in a steady state, so as to realize a regulated output voltage since the CC distribution (Zang et al., 2020). In other words, the steady-state voltage and current on the submarine cable are constant in theory, which makes the system greatly stable. It is very much like that a certain amount of power is temporarily stored on the BL (although it is actually consumed). When the load power increases or decreases, the power consumed by the BL correspondingly decreases or increases. Therefore, the power consumed by the BL can be seen as a power margin left to the load. The higher the power margin (the power consumed by the BL), the greater the amount of load power can increase, however, the lower the power conversion efficiency.

To overcome the problem of low conversion efficiency, one method is to adopt the stack structure which comprises multiple CC/CV modules (Harris and Duennebier, 2002; Asakawa et al., 2003, 2007; Zang et al., 2020), known as the multi-module-stack method (Fig. 1c). In the multi-module-stack CC/CV converter, redundant modules can be bypassed to reduce the consumption of the BL, so as to reach a better efficiency. In addition, the system output capacity can be improved. Therefore, at present, many CC cabled underwater observatory systems with high power requirements adopt the active shunt regulator method, such as the Hawaii-2 Observatory (H2O) (Petitt et al., 2002; Butler, 2003), ALOHA Cabled Observatory (ACO) (Howe et al., 2011, 2015), the development of dense ocean-floor network system for earthquakes and tsunamis (DONET) (Kawaguchi et al., 2008), and DONET-2 (Choi et al., 2013; Kawaguchi et al., 2013). In other words, the active shunt regulator based on multiple CC/CV modules is the mainstream method at present. The efficiency of the system was analyzed in Chen et al. (2020) in detail, from which we can see that the efficiency is still very low under certain load power requirements, and that a lot of heat is still necessary to be dissipated in the BL,

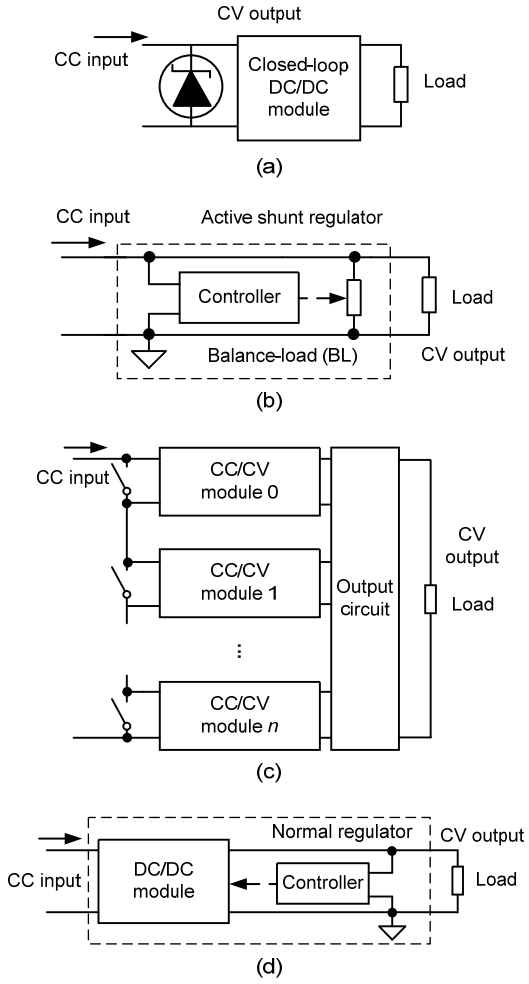

Fig. 1 Common methods of CC/CV conversion: (a) Zener diode; (b) active shunt regulator; (c) multi-module-stack method based on an active shunt regulator; (d) normal regulator

which also poses a challenge to the cooling system design.

Moreover, using the normal regulation method is one of the possible solutions (Fig. 1d). The normal regulator is to directly adjust the system voltage without BL when the load changes, which is very similar to adjusting the current when the load changes in a CV system. Without considering the effect of the long cable, the system can be well stabilized with a compatible feedback design (Saha et al., 2018a, 2018b; Wang HJ et al., 2019). The LCL-T resonant network based DC/DC converter proposed in Saha et al. (2021) achieves very high conversion efficiency (the peak efficiency is approximately up to 96%), which makes this a very promising idea. In Zapolskiy et al. (2018), the electric energy of the solar battery as a current source was converted into CV electric energy, and there was no long cable in the system. In the case of a long cable, Wang HJ et al. (2017) can also stabilize the system; bandwidth is, however, limited by the effect of the cable and the negative impedance characteristics of the converter. Compared with the shunt regulator, the normal regulator may still face challenges of the inherent instability due to the slow dynamic response of a long cable in the CC system, especially when powering a heavy load (Harris and Duennebier, 2002). To sum up, considering that the mainstream CC underwater observatory system still adopts the shunt regulation method at present, the goal of this paper is to improve the shunt regulator instead of doing further research on the normal voltage regulator. We believe that use of the normal regulator is promising and worth further research, but this is not the main topic in this paper.

1.2 Motivation of this paper

If the load power is kept at a high level, this results in a low level of heat dissipation on the BL (Fig. 2a), under which circumstance the shunt regulator is suitable. However, under the following two circumstances, which are very common in underwater observation applications, the aforementioned traditional shunt regulators are not the most cost-effective:

1. Load power demand is relatively stable. For example, load is only some communication equipment and the sensors with stable power demand. In this case, an unnecessary power margin is possibly left on the BL (Fig. 2b). At this point, we need to reduce the unnecessary heat dissipation on the BL. Even if the multi-module-stack method is used to reduce the power of BL, due to the fact that it is a stepped power reconfiguration method, the system cannot guarantee that the power consumed by BL is an ideal value under any stable load state. However, if a method can be used to adjust and control the power of BL without steps, a reasonable power margin can be reserved for the system to prevent the power failure caused by sudden load rise. The unnecessary power consumed by BL can be reduced within the range designed by the designers, and the system efficiency can be relatively improved (Fig. 2c).

2. The load power changes over a wide range, but the changing rate is relatively slow, e.g., the

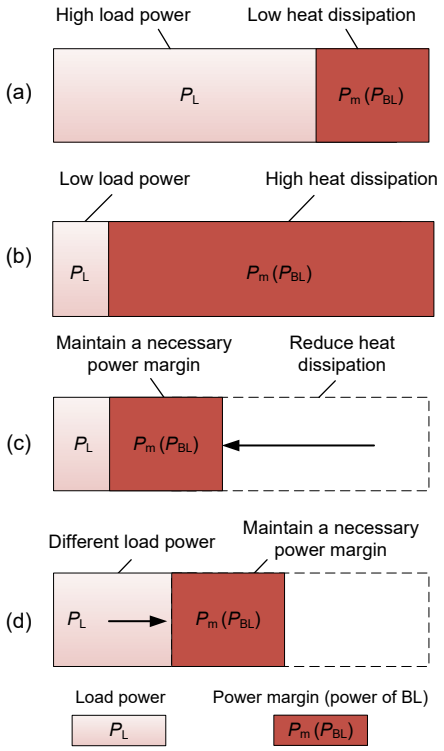

Fig. 2 Motivation for the stepless power reconfiguration (SPR) of the shunt regulator explored in this study

(a) If load power is kept at a high level, it will result in a low level of heat dissipation on the BL; (b) If load power is kept at a low level, an unnecessary power margin is possibly left on the BL, leading to a waste of power; (c) In this study, we adjust the power of BL steplessly, and only a reasonable power margin can be reserved for the system to prevent the power failure caused by sudden load rise; (d) If the load changes slowly, the strategy in this study adjusts the power of BL automatically to ensure that the power margin of the system is kept in a necessary range

charging process of an autonomous underwater vehicle (AUV) (Lin et al., 2019) or other devices. Although the power demand changes greatly at the beginning of charging, the change of power during the charging process is relatively slow (Yong and Rahim, 2013; Khan et al., 2016). In this case, if only the traditional shunt regulation method is adopted, it is obvious that a large amount of power will be dissipated in BL for a long time. It is more suitable if we can use some methods to adjust the power of BL steplessly and automatically, and even if the load slowly changes, the power margin of the system will still be kept in a low and necessary range, so as to reduce the useless dissipation (Fig. 2d).

Therefore, focusing on the above two circumstances, the concept of stepless power reconfiguration (SPR) of the CC/CV module is proposed in this study. Moreover, two practical and effective modes of the CC/CV module are introduced. On the premise that the stability of the system is fully guaranteed, the power thermal dissipation of the BL is reduced, so that the output power of the system is close to the power required by the load, resulting in relatively high conversion efficiency.

2 Stepless power reconfiguration

2.1 System description

The system block diagram of a stepless-power-reconfigurable CC/CV module is shown in Fig. 3. This consists of an open-loop DC/DC module, a BL, an analog-to-digital converter (ADC), a controller, a BL driver, and a closed-loop DC/DC module at the output side. The main function of an open-loop DC/DC module is to scale the current according to a fixed ratio and isolate the voltage of the input side and output side. Note that the internal control duty cycle

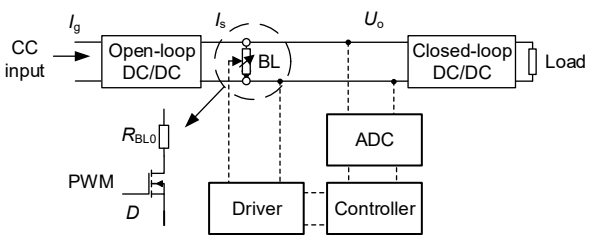

Fig. 3 Block diagram of the stepless-power-reconfigurable CC/CV module

in this DC/DC module is fixed; the current transfer ratio is also fixed. The controller used here is a digital controller; thus, sampling the output voltage from the ADC module, the controller adjusts the resistance value of the BL through the BL driver, so as to regulate the output voltage (U_o) to the expected value (U_{ref}) (Zang et al., 2020). The back-end DC/DC module is a traditional closed-loop DC/DC module required to have a wide input voltage range and a constant output voltage.

The output power of the open-loop DC/DC module is the power capacity of the CC/CV module, consumed by both the BL and the load as aforementioned. Because of the constant and known input current (I_g), the output current (I_s) of the open-loop DC/DC module is also constant and known. Hence, if the output voltage (U_o) can be well regulated to an expected value, the output power of the DC/DC module, namely, the power capacity of the CC/CV module, can also be well reconfigured to an expected value. Therefore, as long as we know how much effective power of the system is consumed by the load, or how much power is dissipated by the BL through the thermal dissipation, we can adjust the output voltage to adjust the power of the BL, so as to adjust the efficiency of the system. In addition, for the load, the back-end closed-loop DC/DC module with a wide input voltage range will further regulate the voltage to a constant value; that is, even if it is U_o that is adjusted to achieve the power capacity reconfiguration, the required voltage of the load can still be fully guaranteed. Moreover, once there is a certain power consumption left on the BL (that is, there is a certain power margin in the system), even if the load has an unexpected power rise, the CC/CV module can still ensure its full stability. Due to the stepless adjustment of U_o, the power reconfiguration is also stepless. This is the main concept of the SPR method.

2.2 Manual stepless power reconfiguration

It is known that under the effect of the controller, when the system reaches its steady state, the system satisfies the following equation:

$$U_o I_s = P_s = P_m + P_L. \tag{1}$$

Here, U_o, I_s, and P_s are the output voltage, output current, and output power of the open-loop DC/DC

module respectively, P_{m} is the power margin of the system, which has different names from different perspectives, and P_{L} is the power consumption of the load.

The idea of manual stepless power reconfiguration (MSPR) is that in practical applications, operators on the shore need to estimate the actual power of the load and set an output voltage according to the load characteristics, and then the power margin will be adjusted to the corresponding value. The output voltage to be set must satisfy

$$U_{\mathrm{o}}=\left(P_{\mathrm{m\_t}}+P_{\mathrm{LMAX}}\right)\Big/I_{\mathrm{s}}, \tag{2}$$

where $P_{\mathrm{m\_t}}$ is the target power margin reserved for the system and P_{LMAX} is the estimated maximum power of the load.

Compared with the traditional method where the output voltage is set constant leading to constant power consumption, MSPR has some obvious advantages: the adjustable or fixed output voltage ensures that the power consumption value of the CC/CV module is an expected value of the operators, and the desired power margin is also achieved. Due to the preset power margin, the steady-state dissipation of the BL can be maintained in a relatively small range, and the efficiency will be correspondingly improved.

2.3 Automatic stepless power reconfiguration

Although MSPR is a quite simple method, it also has some obvious disadvantages. First, because it is calculated by the estimated maximum power of the load, especially for the second circumstance mentioned in Section 1, the actual power margin must be greater than $P_{\mathrm{m\_t}}$ in a long-time range, which is a waste of power. Similarly, due to the submarine cables and other reasons, the voltage adjustment process cannot be too fast, which may cause stability problems (Harris and Duennebier, 2002). It is difficult to avoid voltage changing too fast if applying only MSPR. Therefore, here we allow the BL to have a high dissipation in a period and use a certain delay strategy to reduce the power of the BL into the desired range according to the real-time monitored load power automatically. Therefore, even if the load changes in a certain range, by automatic stepless power reconfiguration (ASPR), the power capacity of the system will be adjusted to keep the power consumption of the BL in the desired range, instead of at a particularly high level. In addition, ASPR can avoid the system stability problem caused by the rapid change of output voltage due to possible poor operation.

An inner-outer loop control strategy is proposed to achieve ASPR (Fig. 4). The inner loop is designed to regulate the output voltage, the same as the traditional method in Zang et al. (2020) and MSPR. The state calculation part is responsible for calculating the real-time power capacity, power margin, load power, target voltage, and other key states. The outer loop uses the calculated target voltage to further adjust the output voltage of the system with a certain inertia delay.

Therefore, the key technologies of the ASPR are: (1) how to obtain the power distribution in Eq. (1) effectively; (2) how to adjust the power margin.

For the first question, although the direct monitoring of load power P_{L} is widely used in engineering (Wang J et al., 2015), the direct goal of ASPR is to adjust the power margin. Instead of monitoring the load power, it is better to obtain the power margin of

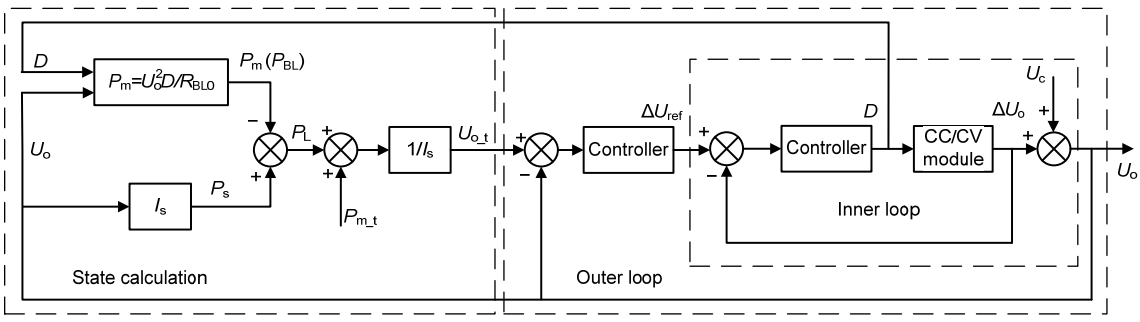

Fig. 4 Block diagram of the inner-outer loop control strategy

the current system directly. The equivalent resistance of the BL used in Fig. 3 varies with the driving duty cycle and satisfies Eq. (3) (detailed analysis and derivation can be found in Section 3):

$$R_{\mathrm{BL}}=R_{\mathrm{BL0}}/D. \tag{3}$$

Here, R_{BL} is the equivalent resistance of the BL, R_{BL0} is the resistance of the fixed resistor, and D is the driving duty cycle. Under the output voltage U_{o}, the power consumption of BL is

$$P_{\mathrm{m}}=P_{\mathrm{BL}}=U_{\mathrm{o}}^2/R_{\mathrm{BL}}=U_{\mathrm{o}}^2D/R_{\mathrm{BL0}}, \tag{4}$$

where P_{BL} is the power consumption of BL.

As long as the output voltage U_{o} and duty cycle D are obtained in real time, the current system power margin P_{m} can be easily obtained. We may as well bring Eq. (4) into Eq. (1), and the current load power can be obtained by

$$P_{\mathrm{L}}=U_{\mathrm{o}}I_{\mathrm{s}}-U_{\mathrm{o}}^2D/R_{\mathrm{BL0}}. \tag{5}$$

In terms of the second question, the relationship among the variables in Eq. (5) is shown in Fig. 5. We can see why the inner-outer loop control strategy is necessary. From Fig. 5a, it is not convenient to adjust D directly by the outer loop given the nonlinear factors when the power margin needs to be adjusted. However, the relationship between the output voltage and power margin is linear as shown in Fig. 5b. Therefore, with the inner-outer loop control strategy, the outer loop needs only to provide a reference voltage U_{ref} to the inner loop, and the inner loop will automatically adjust the value of D to regulate the output voltage. In Fig. 4, since the inner loop adopts the small-signal model in Zang et al. (2020), what is provided by the outer loop is the increment of the reference voltage ΔU_{ref}, and the output voltage value of the inner loop needs to be added with an initial voltage U_{c}. The working points of the system are on the black line if the power margin of the CC/CV module is equal to the target power margin $P_{\mathrm{m\_t}}$ (Fig. 5b). The state calculation part will provide a target output voltage $U_{\mathrm{o\_t}}$, which can achieve the preset $P_{\mathrm{m\_t}}$, to the outer loop. The voltage error signal is obtained by the difference between $U_{\mathrm{o\_t}}$ and U_{o}, through which the controller in the outer loop can

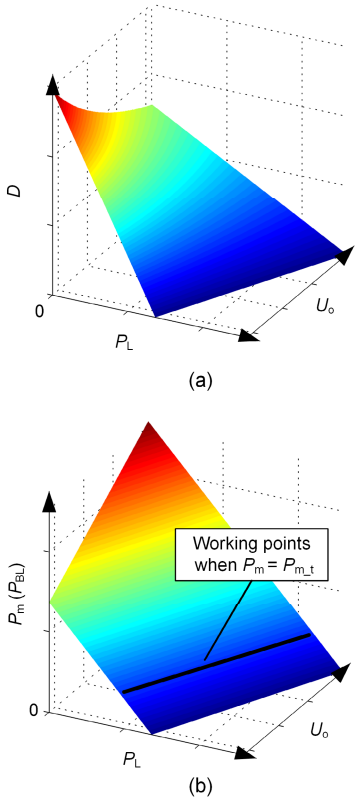

Fig. 5 Schematic relationships among duty cycle, load power, and output voltage (a) and among power margin, load power, and output voltage (b)

output ΔU_{ref} to achieve a certain delay. This is the control method of the outer loop.

As for how to obtain the target output voltage $U_{\mathrm{o\_t}}$, in practical applications, the output current of the system is often known to operators. Therefore, we may as well preset an appropriate $P_{\mathrm{m\_t}}$, and the target output voltage can be calculated and updated in real time through the output voltage and the duty cycle as follows:

1. Obtain the current power capacity of the CC/CV module: $P_{\mathrm{s}}=U_{\mathrm{o}}I_{\mathrm{s}}$.

2. Calculate the current power margin through Eq. (4).

3. Calculate the power load through Eq. (5).

4. Calculate the target output voltage:

$$U_{\mathrm{o\_t}}=(P_{\mathrm{L}}+P_{\mathrm{m\_t}})/I_{\mathrm{s}}. \tag{6}$$

This is the "state calculation" (Fig. 4).

With ASPR applied, the output voltage also changes with the different load power. Compared

with the normal voltage regulator, however, the essence of ASPR is to temporarily consume a certain amount of power on the BL. It still is a shunt regulator, which can be seen as an improved automatic capacity-self-regulated Zener diode as shown in Fig. 1a. The consumption of BL is more like a kind of power reservation. When the load changes, the CC/CV module first lets the BL give up its power to the load and then lets the BL slowly recover to the preset target power margin from the submarine cable. As long as the load power increment does not exceed the power margin, there will be no stability problem. Moreover, the problems of high thermal dissipation and low efficiency of traditional shunt regulators can be solved. This is the main idea of ASPR.

3 System analysis

3.1 Efficiency and target power margin

The conversion efficiency of the CC/CV module is composed of three parts, the efficiencies of the open-loop DC/DC module, the shunt regulator, and the closed-loop DC/DC module. The open-loop DC/DC module has different efficiencies with different topologies applied. Many current to current DC/DC converters have been proposed and analyzed (Asakawa et al., 2007; Wang HJ et al., 2019); these have different characteristics including their efficiency. Similarly, the closed-loop DC/DC module is one of the commercial converters, and its efficiency can also reach a high value. Therefore, in this study, we discuss only the efficiency of the shunt regulator which is the core problem. Due to the changeable output voltage, the working points of open-loop DC/DC and closed-loop DC/DC modules are changed correspondingly, which has a certain impact on their conversion efficiency but will not be discussed in this study.

Different P_{m} values lead to different efficiencies:

$$\eta = P_{\mathrm{L}} / (P_{\mathrm{L}} + P_{\mathrm{m}}). \tag{7}$$

Here, η is the conversion efficiency of the shunt regulator. Thus, with ASPR applied, P_{m} will eventually converge to $P_{\mathrm{m\_t}}$. The smaller the value of $P_{\mathrm{m\_t}}$, the higher the efficiency. However, due to the delay purpose of ASPR, when the increment of the load exceeds P_{m}, a power failure may occur in the system. Therefore, $P_{\mathrm{m\_t}}$ must be determined according to the actual load rather than only seeking a quite high efficiency.

In addition, as shown in Fig. 3, both the open-loop and closed-loop DC/DC modules limit the range of voltage U_{o}. If U_{o} is reduced to a very low value to reduce the power margin of the system to the target power margin when the load power is a relatively small value, the calculated target voltage $U_{\mathrm{o\_t}}$ may be smaller than the minimum voltage value of the system. Similarly, when the load requires relatively large power, $U_{\mathrm{o\_t}}$ may exceed the maximum voltage of the system. We need to saturate the target voltage value calculated by the above method, that is, to limit the range of $U_{\mathrm{o\_t}}$ in the calculation process. Therefore, the minimum voltage and maximum voltage required by the system will have a certain impact on the steady-state power margin. Assuming that the load power is a fixed value, the steady-state power margin can be obtained:

$$P_{\mathrm{ssm}} = \begin{cases} U_{\mathrm{MIN}} I_{\mathrm{s}} - P_{\mathrm{L}}, & U_{\mathrm{o\_t}} < U_{\mathrm{MIN}}, \\ P_{\mathrm{m\_t}}, & U_{\mathrm{MIN}} \le U_{\mathrm{o\_t}} \le U_{\mathrm{MAX}}, \\ U_{\mathrm{MAX}} I_{\mathrm{s}} - P_{\mathrm{L}}, & U_{\mathrm{o\_t}} > U_{\mathrm{MAX}}. \end{cases} \tag{8}$$

Here, P_{ssm} is the steady-state power margin, and U_{MIN} and U_{MAX} are the minimum output voltage and maximum output voltage, respectively. Substitute Eq. (6) into Eq. (8), we can obtain:

$$P_{\mathrm{ssm}} = \begin{cases} U_{\mathrm{MIN}} I_{\mathrm{s}} - P_{\mathrm{L}}, & P_{\mathrm{L}} < U_{\mathrm{MIN}} I_{\mathrm{s}} - P_{\mathrm{m\_t}}, \\ P_{\mathrm{m\_t}}, & U_{\mathrm{MIN}} I_{\mathrm{s}} - P_{\mathrm{m\_t}} \le P_{\mathrm{L}} \le U_{\mathrm{MAX}} I_{\mathrm{s}} - P_{\mathrm{m\_t}}, \\ U_{\mathrm{MAX}} I_{\mathrm{s}} - P_{\mathrm{L}}, & P_{\mathrm{L}} > U_{\mathrm{MAX}} I_{\mathrm{s}} - P_{\mathrm{m\_t}}. \end{cases} \tag{9}$$

Eq. (9) is a piecewise function which varies with different load power. We can obtain the relationship between the steady-state power margin and the load power (Fig. 6). We segment the load according to the load characteristics: it is called the small-load linear section (SLLS) or the large-load linear section (LLLS) if the load power is less than $U_{\mathrm{MIN}}I_{\mathrm{s}}-P_{\mathrm{m\_t}}$ or greater than $U_{\mathrm{MAX}}I_{\mathrm{s}}-P_{\mathrm{m\_t}}$, respectively. The rest is called the intermediate section (IS). It is illustrated from Fig. 6 that when P_{L} is in SLLS, due to the existence of U_{MIN},

the designed target power margin is not fully ensured, while the steady-state power margin is greater than the target power margin, which has no negative effects on the stability. If designers are willing to fully ensure the preset target power margin, then inequality (10) must be satisfied:

$$U_{\mathrm{MIN}} \cdot I_{\mathrm{s}} \le P_{\mathrm{m\_t}}. \tag{10}$$

Namely, SLLS no longer exits. Similarly, when P_{L} is in LLLS, the designed target power margin is also not fully guaranteed, and the steady-state power margin is less than the target power margin which will affect the stability. Therefore, to ensure that the target power margin is sufficient and that the system is highly stable, the load shall not work in LLLS in practical applications.

Consequently, considering the influence of the maximum output voltage and minimum output voltage, the efficiency of the system can be obtained:

$$\eta = \begin{cases} \dfrac{P_{\mathrm{L}}}{U_{\mathrm{MIN}} \cdot I_{\mathrm{s}}}, & P_{\mathrm{L}} < U_{\mathrm{MIN}} I_{\mathrm{s}} - P_{\mathrm{m\_t}}, \\ \dfrac{P_{\mathrm{L}}}{P_{\mathrm{m\_t}} + P_{\mathrm{L}}}, & U_{\mathrm{MIN}} I_{\mathrm{s}} - P_{\mathrm{m\_t}} \le P_{\mathrm{L}} \le U_{\mathrm{MAX}} I_{\mathrm{s}} - P_{\mathrm{m\_t}}, \\ \dfrac{P_{\mathrm{L}}}{U_{\mathrm{MAX}} \cdot I_{\mathrm{s}}}, & P_{\mathrm{L}} > U_{\mathrm{MAX}} I_{\mathrm{s}} - P_{\mathrm{m\_t}}. \end{cases} \tag{11}$$

Eq. (11) is also a piecewise function, which varies with different load power. Without applying ASPR, the conversion efficiency is (Chen et al., 2020):

$$\eta = P_{\mathrm{L}} / (U_{\mathrm{MAX}} \cdot I_{\mathrm{s}}). \tag{12}$$

It is clear that Eq. (12) is the same as that in LLLS; that is, in LLLS, the efficiency is not improved compared with the traditional method. However, the efficiency in SLLS and IS is significantly improved compared with that in the traditional method, as shown in the shaded part of Fig. 7. Moreover, it can be known that a larger target power margin will lead to a smaller SLLS and a larger LLLS, and the efficiency improvement in IS is less significant compared with that in the traditional method. Therefore, if the load power is relatively stable and the efficiency is a priority to designers, the target power margin should not be too large. On the contrary, when the load is not stable enough while stability is the priority, the target power margin should not be too small. The specific value must be determined according to the actual requirements.

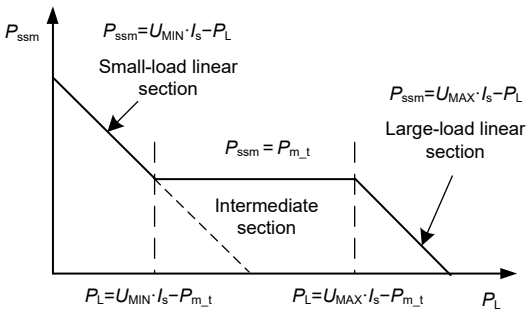

Fig. 6 Schematic steady-state power margin curve

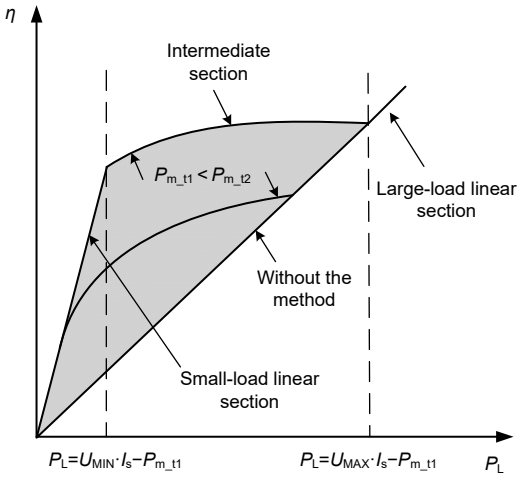

Fig. 7 Schematic efficiency curve

3.2 System strategy with a starting up load

MSPR is a general method, which can meet different load power requirements. ASPR can meet the two circumstances mentioned in Section 1, and either of them is a mode of the CC/CV module. In the traditional CC converter, an analog controller is often the first choice, while in either MSPR or ASPR, a digital controller is the best option. In the above analysis, it is necessary to obtain various real-time states of the system, such as duty cycle and output voltage, so as to obtain the current load power and power margin, which are only the results of input, output, or simple calculation of the controller. At the same time, due to the need for real-time voltage

regulation, the reference voltage using a digital value will bring higher reliability.

An important premise of both MSPR and ASPR is that the incremental power of the load shall not exceed the existing reserved power margin of the system; otherwise, the system may be unexpectedly unstable, which is a characteristic of a shunt regulator. As for MSPR, the system margin can be set as large as possible since it can be manually controlled by the operators. However, for ASPR, the steady-state power margin is theoretically equal to the target power margin that is not a very large value. Even if the load is very stable, there still is a stepping power increase at the moment of load starting. Therefore, we need to combine both MSPR and ASPR under this circumstance. By applying the digital controller, the CC/CV module can be easily switched between MSPR mode and ASPR mode. Before the load is cut in, the CC/CV module should be in MSPR mode, and the output voltage needs to be set at a suitable value according to the method in the previous section. After load cut in, the operators should judge if this load meets either of the two circumstances mentioned in Section 1. If yes, ASPR mode can be turned on to further reduce the power consumption of BL and improve efficiency. If not, MSPR mode needs to be maintained and a possible better output voltage can be set to meet the load requirement and the efficiency consideration.

3.3 Design of BL

The BL in this study adopts the structure introduced in Chen et al. (2019b) and Zang et al. (2020), which consists of only several resistors and switches in series with the advantages of high reliability and easy implementation. For simplicity, these resistors and switches are treated as one equivalent resistor R_{BL0} and one equivalent switch, respectively. Note that the function of the switch should be realized by MOSFET or other semiconductor components that can realize high-speed switch function. When the switches are driven by a pulse width modulation (PWM) wave with a certain duty cycle D as the control signal, the current discontinuously flows through the resistor, resulting in the equivalent resistance of the BL varying with the preset duty cycle. The average current I_{BLA} flowing through resistor R_{BL0} within a period of PWM wave T_{BL} can be derived as

$$I_{\mathrm{BLA}}=\frac{1}{T_{\mathrm{BL}}}\left(\int_0^{DT_{\mathrm{BL}}} i_{\mathrm{BL}}(t)\mathrm{d}t+\int_{DT_{\mathrm{BL}}}^{T_{\mathrm{BL}}} i_{\mathrm{BL}}(t)\mathrm{d}t\right)=D\frac{U_{\mathrm{o}}}{R_{\mathrm{BL0}}}. \tag{13}$$

On this basis Eq. (3) can be obtained. Fig. 8 shows the relationship between the average current and the duty cycle, and the corresponding equivalent resistance value and duty cycle under a constant voltage of 48 V. The experimental results are consistent with calculated results through Eq. (3).

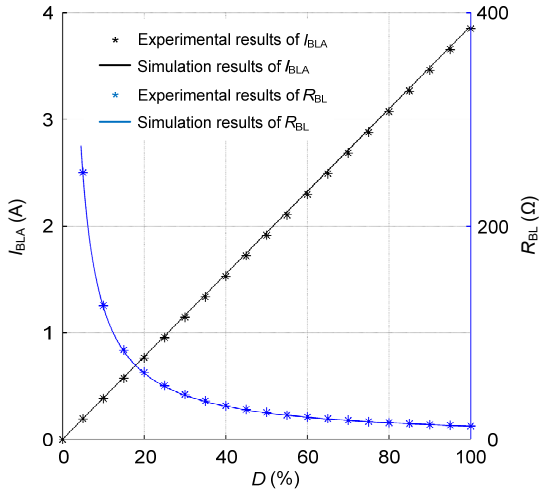

Fig. 8 Experimental results of average current flowing through the BL under the voltage of 48 V and the equivalent resistance of the BL (References to color refer to the online version of this figure)

After obtaining the key relationship among the equivalent resistance of BL, the duty cycle, and the fixed resistance value, we can study the conditions of BL to ensure that ASPR can be realized. According to Eqs. (1) and (4), we can obtain

$$\frac{\left(P_{\mathrm{L}}+P_{\mathrm{m}}\right)^2}{P_{\mathrm{m}}\cdot I_{\mathrm{s}}^2}=R_{\mathrm{BL}}=\frac{R_{\mathrm{BL0}}}{D}. \tag{14}$$

The right side of Eq. (14) is the equivalent resistance of the BL. The left side of Eq. (14) is a value that varies with different power margin and different load power. The value of R_{BL} must ensure that P_{m} can be equal to the target value $P_{\mathrm{m\_t}}$. Since the equivalent resistance of BL has only a minimum value but no maximum value, it is obvious that the minimum value of R_{BL} should be less than the minimum value on the

left side of Eq. (14). Hence, R_{BL0} must satisfy

$$R_{BL0} \le [D]_{MAX} \cdot \left[\frac{(P_L + P_{m\_t})^2}{P_{m\_t} \cdot I_s^2} \right]_{MIN}, \quad (15)$$

where $[\cdot]_{MAX}$ and $[\cdot]_{MIN}$ represent the corresponding maximum and minimum values, respectively.

Thus, when the load power is equal to 0 and the duty cycle is the maximum, the calculated result is the maximum limit of R_{BL0}. Assuming that the duty cycle varies in the range of [0, 1], then inequality (15) can be further simplified as

$$R_{BL0} \le \frac{P_{m\_t}}{I_s^2}. \quad (16)$$

3.4 Stability analysis

Both ASPR and the normal regulation method adjust the input voltage. However, the main differences between ASPR and the normal regulation method are as follows: ASPR is to temporarily consume a certain power on the BL to maintain a sufficient power margin, which makes this method still a shunt regulator. Then the system will not only automatically but also slowly adjust the intermediate stage output voltage (U_o) with the delay strategy as mentioned. This sufficient delay strategy makes the voltage adjustment continue for a few seconds, which is much longer than the millisecond adjustment time of the normal regulation method, so as to alleviate the negative impedance characteristics of the CC/CV module.

Hence, with this delay strategy of the outer loop, we can assume that the stability of the system depends only on the inner loop. The control block diagram of the inner loop is shown in Fig. 9. Note that here we simplify all load on the output side of the DC/DC module into one equivalent resistor R_o. All variables in the figure corresponding to the above variables are just in lowercase and with "^" representing the increment value under a small-signal scale.

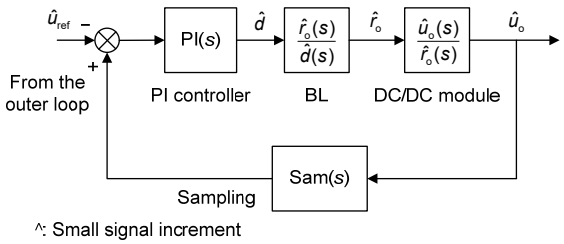

Fig. 9 Control loop of the system under the small-signal scale

To illustrate the stability of the system, there is no harm in adopting the push-pull DC/DC module in Zang et al. (2020), the model of which has been derived as follows:

$$\frac{\hat{u}_o(s)}{\hat{r}_o(s)} = \frac{K^2 I_s L C_i s^2 + I_L}{K^2 L C_i C_o R_o s^3 + K^2 L C_i s^2 + \left(K^2 C_i R_o + C_o R_o\right) s + 1}. \quad (17)$$

The equation characterizes the relationship between the output voltage U_o and the equivalent resistor R_o in a form of the small-signal increment. Due to page limitation, please refer to Zang et al. (2020) for the structure of the push-pull DC/DC module and the meaning of parameters on the right side of Eq. (17). Also using the small-signal model, we can obtain the dynamic equation of BL:

$$\frac{\hat{r}_o(s)}{\hat{d}(s)} = -R_o. \quad (18)$$

In cases where the reference voltage is constant (without considering the outer loop), since the current at the output side of the DC/DC module is constant in the steady state, R_o is constant. The target voltage provided by the outer loop changes slowly; hence, it is advisable to assume that R_o is constant when analyzing the scenario under a specific reference voltage. Note that there is a "–" (minus) sign in Eq. (18); hence, feedback is inherently negative and the sign of the output signal from Sam(s) shall be positive.

In this study, the proportional-integral (PI) controller with mature design theory is used in the system. Set C_i=47 μF, C_o=100 μF, L=2 mH, K=2, I_s=1.9 A, U_{ref}=48 V (R_o=U_{ref}/I_s=25.3 Ω). Set the proportional coefficient K_p=15 and integral coefficient K_i=500. It is also assumed that the sampling part is a constant gain equal to 5/48. The Bode diagram of the open-loop transfer function after PI compensation is shown in Fig. 10. The crossover frequency is 4.5 kHz; the phase margin is 90.7° with an infinite gain margin.

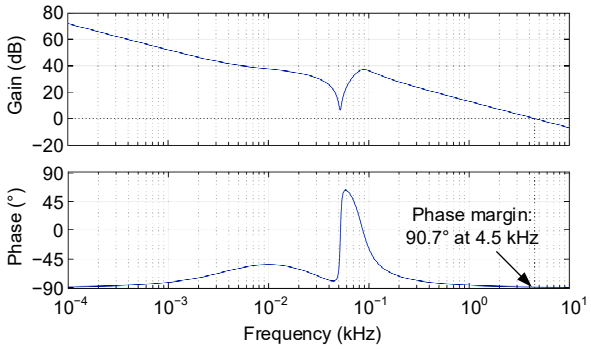

Fig. 10 Stability margin of the system

The inner loop control strategy ensures fast response of the system and makes the system have a sufficient stability margin. As long as the instantaneous increment of load power does not exceed the power margin, there will be no stability problem that may occur in the normal regulation method due to its negative impedance characteristics and the long submarine cable scale. This is also one of the advantages of the ASPR mode.

4 Experimental results

4.1 Setup of the experiment

The setup of the experiment is shown in Fig. 11, which consists of a CC power source, an oscilloscope, an electronic load, and other components mentioned in Section 2. The output current I_s of the open-loop DC/DC module is measured as 1.82 A. The closed-loop DC/DC module has a rated output of 24 V with a wide input voltage range from 14 V to 70 V. To ensure its safety and reliability, the output range of U_o is set between 20 V and 60 V. The electronic load simulates the load of the CC/CV module. Considering the simplicity of the experiment, we set the electronic load working in the current model. Given that the heat loss of the system is different at different time, the measured power corresponding to the same current value may be slightly different. Note that there is a certain conversion loss in the closed-loop DC/DC module, the actual measured power value is greater than the product of the current value and the output voltage of 24 V. In addition, due to the inevitable existence of certain resistive load in the system (such as the unloading resistors in parallel at the end of the open-loop DC/DC module), the actual load power is higher than the external load power. To better illustrate the main idea of this study, the load power is the actual measured power consumed by the load minus the power of the resistive load, that is, the input power of the closed-loop DC/DC module.

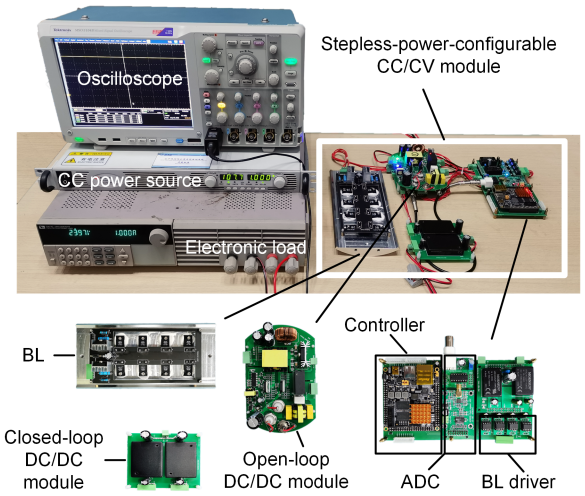

Fig. 11 Setup of the experiment

4.2 Load starting up

The experimental results under different load are shown in Fig. 12. We set the load as 0.75, 1.50, 2.25, and 3.00 A, and the corresponding input power of the closed-loop DC/DC module is 17.6, 37.3, 61.2, and 83.5 W, respectively. According to the strategy analyzed above, first, operators need to turn on MSPR mode and set an appropriate output voltage value. Here, we select the maximum voltage, i.e., 60 V, as the voltage before load starts. The theoretical power margin is 109.2 W. Considering the internal consumption mentioned above, the measured power margin is about 101 W. At the moment of 0.5 s, the start-up of each load leads to the stepping up of load power. Because the steady-state power of each load is less than the power margin at this time, the CC/CV module is able to supply power to the load normally. Since the load is stable after starting, the CC/CV module is switched to ASPR mode at 2.5 s with a preset target power margin of 25 W. Except for the load of 3.00 A, the power of BL, namely, the power margin of the load of 0.75, 1.50, and 2.25 A begins to decline slowly, and all converges to 25.3 W. The efficiency increases from 0.23, 0.40, and 0.64 to 0.41,

0.60, and 0.71, respectively (i.e., increased by 78%, 50%, and 11%, respectively). However, it can be seen from Fig. 12 that for the load of 3.00 A, the power margin of the system is 17.5 W after the load starting up, which is less than the target power margin of 25 W. In other words, the voltage must be increased to ensure the target power margin, while the voltage is already the maximum regulated voltage of 60 V. Therefore, even if ASPR mode is turned on, the power margin will not be further adjusted. Because the power margin of the system cannot be fully guaranteed, it naturally has a higher efficiency (0.84). Nonetheless, the fluctuation of load power is easy to cause stability problems due to the lack of power margin, which should be avoided in practical applications.

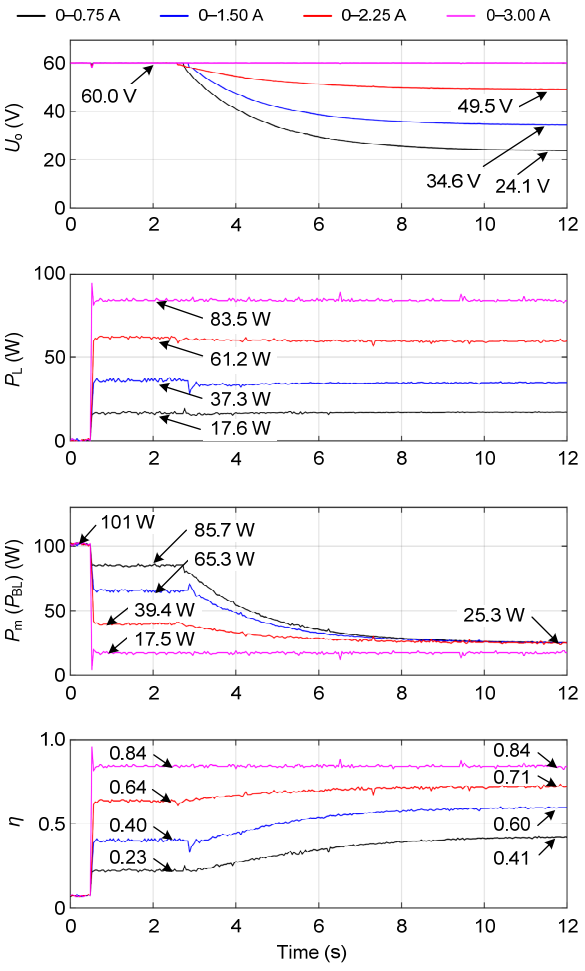

Fig. 12 Experimental results under the strategy with load starting up (References to color refer to the online version of this figure)

4.3 Relatively slowly changing load over a wide range

4.3.1 Load in stepped variation

We take 0.75 A as the initial state, and 0.75 A as a step every 10 s of the load as shown in Fig. 13. Then we let the load step down from the last condition after load stepping up. This kind of load has the characteristics of a wide changing range within a long-time range but a small changing range within a short-time range. Note that to avoid an insufficient power margin under the load of 3.00 A, the upper limit current of the electronic load is set at 2.80 A. As can be seen from Fig. 13a, the initial power consumption value of BL is 25 W, and the corresponding initial voltage is 23.9 V. With the load power stepping up, it is the BL that first gives up its power consumption, resulting in a rapid reduction of the power margin. Then, under the effect of ASPR mode, the power margin slowly rises to the target power margin. The average steady-state power margin is 25.0, 25.0, 25.0, and 24.9 W, and the corresponding output voltage is 23.9, 34.3, 49.2, and 60.0 V, respectively. In theory, the efficiency curve without ASPR applied is shown as the red line in Fig. 13, which is directly obtained from the test data according to Eq. (12). It can be seen that with ASPR applied, the efficiency is increased from 0.17, 0.34, and 0.59 to 0.42, 0.60, and 0.72, respectively, after the system is stable (i.e., increased by 147%, 76%, and 22%, respectively). Similarly, as shown in Fig. 13b, when the load power decreases, the reduced part of the load power is first consumed by the BL, which makes the power margin increase temporally. After the load is stable, the average power consumption of BL is 24.9, 25.0, 25.0, and 25.1 W, respectively, and the efficiency is the same as the circumstance of load stepping down. The steady-state power margin is around the target power margin of 25.0 W with the error of ±0.1 W, which effectively solves the problem of high heat dissipation of the CC/CV module, and correspondingly improves the conversion efficiency. Note that the load of 2.80 A already leads to a maximum voltage of 60 V with a sufficient power margin of 24.9 W; hence, its efficiency is constantly 0.77.

4.3.2 Load in continuous variation

To imitate a load in continuous and slow variation, we set the minimum value of the electronic load

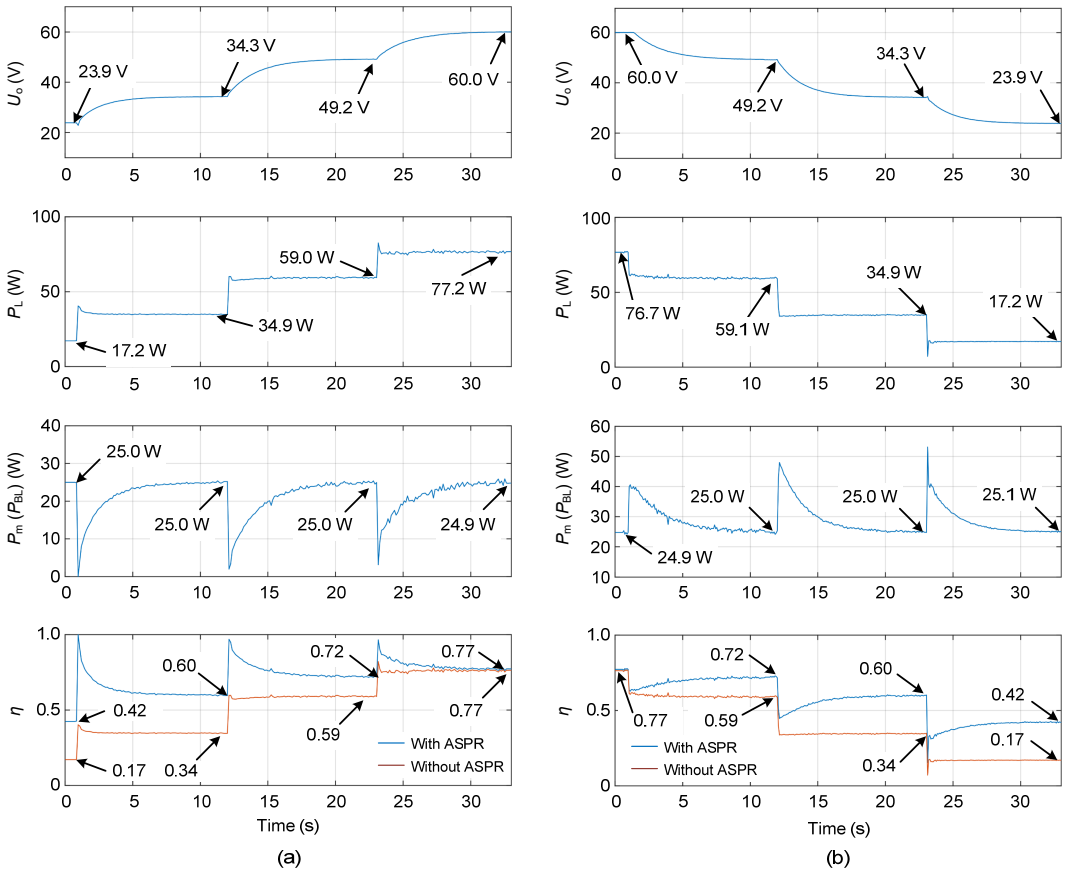

Fig. 13 Experimental results with load in stepped variation: (a) load steps up; (b) load steps down

References to color refer to the online version of this figure

as 0.75 A and the maximum value as 2.25 A which changes periodically in a triangular waveform. The results are shown in Fig. 14. The maximum power and minimum power are 59.8 and 17.1 W, respectively. The corresponding voltage is 48.0 V and 24.7 V, respectively, and the corresponding power margin is 21.4 and 27.3 W, respectively. However, the power margin does not converge to the target power margin while changing periodically between 21.4 and 29.2 W. The lowest and highest points of efficiency are increased from 0.18 and 0.60 to 0.40 and 0.75, respectively (i.e., increased by 122% and 25%, respectively). Nonetheless, the power margin is still in a relatively reliable range, which can also effectively guarantee that the heat dissipation of BL is not too high.

4.4 Efficiency validation

To validate the efficiency of the shunt regulator, we set the target power margin as 5, 15, and, 25 W to obtain the corresponding efficiency under different load power, and also obtain the corresponding ideal efficiency curve through Eq. (12), as shown in Fig. 15. The efficiency in SLLS and IS is significantly improved compared with the one without SPR (i.e., the traditional shunt regulator). The calculation results are highly consistent with the experimental results, which effectively validates the analysis above.

5 Conclusions

The concept of SPR has been introduced in this paper, which is a novel active shunt regulation method that can be used in the CC/CV converter, of which the key technologies are shown in Fig. 16. Focusing on the circumstances mentioned in Section 1, two effective and practical methods named MSPR and ASPR have been discussed. They can steplessly reconfigure the system power manually and automatically, respectively, so as to reduce the unnecessary

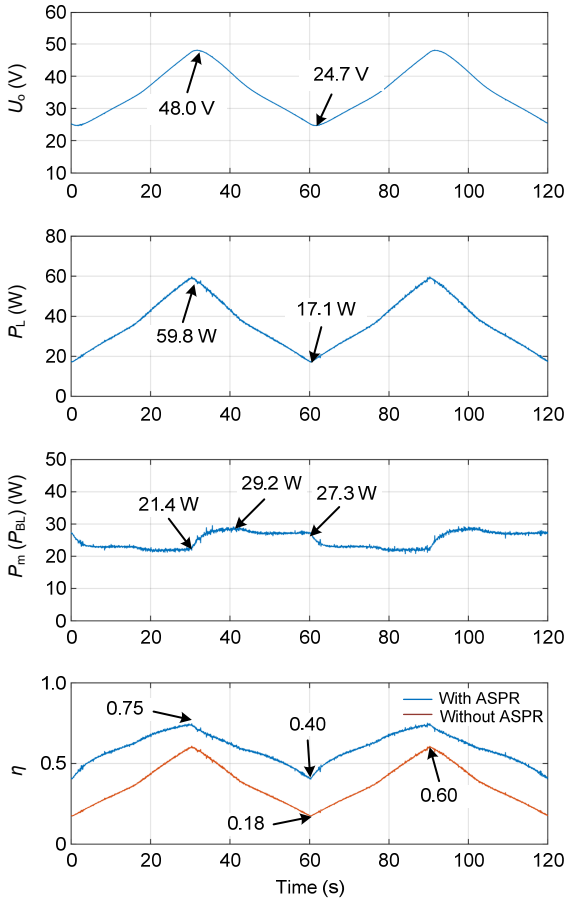

Fig. 14 Experimental results with load in continuous variation

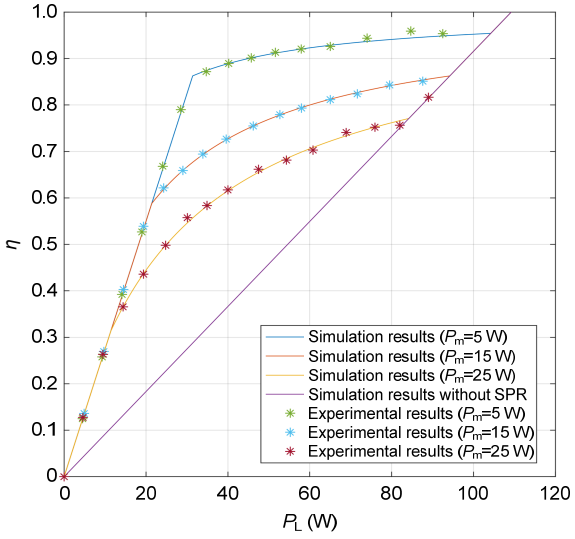

Fig. 15 Experimental results of the efficiency of the shunt regulator with SPR (References to color refer to the online version of this figure)

dissipation of the system and greatly improve the efficiency compared with the traditional shunt regulation method, while ensuring the stability of the system. The experimental results showed that the steady-state efficiency of stepless power reconfiguration can be increased up to 1.47 times that of a typical shunt regulator.

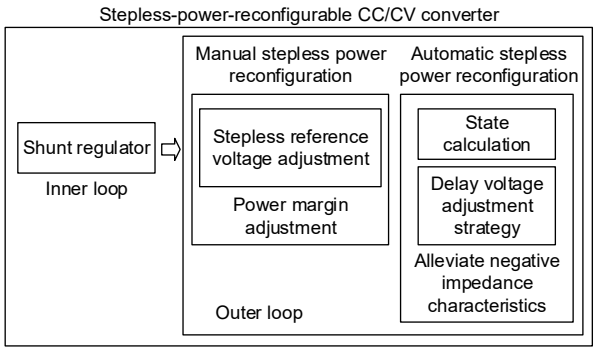

Fig. 16 Key technologies of the stepless-power-reconfigurable converter

Contributors

Yujia ZANG and Yanhu CHEN designed the research. Haoyu ZHANG and Zhiyong DUAN processed the data. Yujia ZANG and Gul MUHAMMAD drafted the paper. Canjun YANG helped organize the paper. Yanhu CHEN and Canjun YANG revised and finalized the paper.

Compliance with ethics guidelines

Yujia ZANG, Yanhu CHEN, Canjun YANG, Haoyu ZHANG, Zhiyong DUAN, and Gul MUHAMMAD declare that they have no conflict of interest.

References

Asakawa K, Kojima J, Muramatsu J, et al., 2003. Novel current to current converter for mesh-like scientific underwater cable network—concept and preliminary test result. OCEANS, p.1868-1873. https://doi.org/10.1109/OCEANS.2003.178172

Asakawa K, Kojima J, Muramatsu J, et al., 2007. Current-to-current converter for scientific underwater cable networks. *IEEE J Ocean Eng*, 32(3):584-592. https://doi.org/10.1109/JOE.2007.905024

Asakawa K, Yokobiki T, Goto TN, et al., 2009. New scientific underwater cable system Tokai-SCANNER for underwater geophysical monitoring utilizing a decommissioned optical underwater telecommunication cable. *IEEE J Ocean Eng*, 34(4):539-547. https://doi.org/10.1109/JOE.2009.2026987

Butler R, 2003. The Hawaii-2 Observatory: observation of

nanoearthquakes. *Seismol Res Lett*, 74(3):290-297. https://doi.org/10.1785/GSSRL.74.3.290

Chave AD, Waterworth G, Maffei AR, et al., 2004. Cabled ocean observatory systems. *Mar Technol Soc J*, 38(2): 30-43. https://doi.org/10.4031/002533204787522785

Chen YH, Yang CJ, Li DJ, et al., 2012. Design and application of a junction box for cabled ocean observatories. *Mar Technol Soc J*, 46(3):50-63. https://doi.org/10.4031/MTSJ.46.3.4

Chen YH, Howe BM, Yang CJ, 2015. Actively controllable switching for tree topology seafloor observation networks. *IEEE J Ocean Eng*, 40(4):993-1002. https://doi.org/10.1109/JOE.2014.2362830

Chen YH, Zang YJ, Yao JJ, et al., 2019a. Optimal communication frequency for switching cabled ocean networks with commands carried over the power line. *Front Inform Technol Electron Eng*, 20(10):1331-1343. https://doi.org/10.1631/FITEE.1900125

Chen YH, Xiao S, Li DJ, 2019b. Power system design for constant current subsea observatories. *Front Inform Technol Electron Eng*, 20(11):1505-1515. https://doi.org/10.1631/FITEE.1800362

Chen YH, Zang YJ, Yang CJ, et al., 2020. Reconfigurable power converter for constant current underwater observatory. *Electronics*, 9(2):307. https://doi.org/10.3390/ELECTRONICS9020307

Choi JK, Nishida S, Yokobiki T, et al., 2013. Development of an automated cable-laying system for DONET construction. IEEE Int Underwater Technology Symp, p.1-6. https://doi.org/10.1109/UT.2013.6519810

Harris DW, Duennebier FK, 2002. Powering cabled ocean-bottom observatories. *IEEE J Ocean Eng*, 27(2):202-211. https://doi.org/10.1109/JOE.2002.1002474

Howe BM, Kirkham H, Vorpérian V, 2002. Power system considerations for undersea observatories. *IEEE J Ocean Eng*, 27(2):267-274. https://doi.org/10.1109/JOE.2002.1002481

Howe BM, Lukas R, Duennebier F, et al., 2011. ALOHA Cabled Observatory installation. OCEANS, p.1-11. https://doi.org/10.23919/OCEANS.2011.6107301

Howe BM, Duennebier FK, Lukas R, 2015. The ALOHA Cabled Observatory. In: Favali P, Beranzoli L, de Santis A (Eds.), Seafloor Observatories. Springer, Berlin, Germany, p.439-463. https://doi.org/10.1007/978-3-642-11374-1_17

Kanazawa T, Shinohara M, Sakai S, et al., 2008. A new compact ocean bottom cabled seismometers system for spatially dense observation on sea floor. OCEANS, p.1-5. https://doi.org/10.1109/OCEANS.2008.5152062

Kanazawa T, Shinohara M, Sakai S, et al., 2011. New innovative ocean bottom cabled seismometer system and observation in the Sea of Japan. IEEE Symp on Underwater Technology and Workshop on Scientific Use of Submarine Cables and Related Technologies, p.1-3. https://doi.org/10.1109/UT.2011.5774112

Kawaguchi K, Kaneda Y, Araki E, 2008. The DONET: a real-time seafloor research infrastructure for the precise earthquake and tsunami monitoring. OCEANS MTS/ IEEE Kobe Techno-Ocean, p.1-4. https://doi.org/10.1109/OCEANSKOBE.2008.4530918

Kawaguchi K, Araki E, Kogure Y, et al., 2013. Development of DONET2—off Kii chanel observatory network. IEEE Int Underwater Technology Symp, p.1-5. https://doi.org/10.1109/UT.2013.6519844

Khan AB, Pham VL, Nguyen TT, et al., 2016. Multistage constant-current charging method for Li-ion batteries. IEEE Transportation Electrification Conf and Expo, p.381-385. https://doi.org/10.1109/ITEC-AP.2016.7512982

Kojima J, Howe BM, Asakawa K, et al., 2005. Power systems for ocean regional cabled observatories. OCEANS, p.2176-2181. https://doi.org/10.1109/OCEANS.2004.1406484

Lin R, Li DJ, Zhang T, et al., 2019. A non-contact docking system for charging and recovering autonomous underwater vehicle. *J Mar Sci Technol*, 24(3):902-916. https://doi.org/10.1007/s00773-018-0595-6.

Petitt RA, Harris DW, Wooding B, et al., 2002. The Hawaii-2 Observatory. *IEEE J Ocean Eng*, 27(2):245-253. https://doi.org/10.1109/JOE.2002.1002479

Qu FZ, Wang ZD, Song H, et al., 2015. A study on a cabled seafloor observatory. *IEEE Intell Syst*, 30(1):66-69. https://doi.org/10.1109/MIS.2015.9

Saha T, Wang HJ, Riar B, et al., 2018a. Analysis and design of a parallel resonant converter for constant current input to constant voltage output DC-DC converter over wide load range. Int Power Electronics Conf, p.4074-4079. https://doi.org/10.23919/IPEC.2018.8507404

Saha T, Bagchi AC, Wang HJ, et al., 2018b. Analysis and design of wide range output voltage regulated power supply for underwater constant input current DC distribution system. IEEE 19th Workshop on Control and Modeling for Power Electronics, p.1-7. https://doi.org/10.1109/COMPEL.2018.8459939

Saha T, Bagchi AC, Zane RA, 2021. Analysis and design of an LCL-T resonant DC-DC converter for underwater power supply. *IEEE Trans Power Electron*, 36(6):6725-6737. https://doi.org/10.1109/TPEL.2020.3034298

Wang HJ, Saha T, Zane R, 2017. Impedance-based stability analysis and design considerations for DC current distribution with long transmission cable. IEEE 18th Workshop on Control and Modeling for Power Electronics, p.1-8. https://doi.org/10.1109/COMPEL.2017.8013355

Wang HJ, Saha T, Riar B, et al., 2019. Design considerations for current-regulated series-resonant converters with a constant input current. *IEEE Trans Power Electron*, 34(1): 141-150. https://doi.org/10.1109/TPEL.2018.2819887

Wang J, Li DJ, Yang CJ, et al., 2015. Developing a power monitoring and protection system for the junction boxes of an experimental seafloor observatory network. *Front Inform Technol Electron Eng*, 16(12):1034-1045.

https://doi.org/10.1631/FITEE.1500099

Yong SO, Rahim NA, 2013. Development of on-off duty cycle control with zero computational algorithm for CC-CV Li ion battery charger. IEEE Conf on Clean Energy and Technology, p.422-426. https://doi.org/10.1109/CEAT.2013.6775668

Zang YJ, Chen YH, Yang CJ, et al., 2020. A new approach for analyzing the effect of non-ideal power supply on a constant current underwater cabled system. *Front Inform Technol Electron Eng*, 21(4):604-614. https://doi.org/10.1631/FITEE.1800737

Zapolskiy SA, Osipov AV, Zhuravlev IM, et al., 2018. Single-cycle LCL-T resonant converter for solar battery. XIV Int Scientific-Technical Conf on Actual Problems of Electronics Instrument Engineering, p.90-93. https://doi.org/10.1109/APEIE.2018.8545079

Zhang ZF, Chen YH, Li DJ, et al., 2018. Use of a coded voltage signal for cable switching and fault isolation in cabled seafloor observatories. *Front Inform Technol Electron Eng*, 19(11):1328-1339. https://doi.org/10.1631/FITEE.1601843