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A creative concept for designing and simulating quaternary logic gates in quantum-dot cellular automata

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Abstract: New technologies such as quantum-dot cellular automata (QCA) have been showing some remarkable characteristics that standard complementary-metal-oxide semiconductor (CMOS) in deep sub-micron cannot afford. Modeling systems and designing multiple-valued logic gates with QCA have advantages that facilitate the design of complicated logic circuits. In this paper, we propose a novel creative concept for quaternary QCA (QQCA). The concept has been set in QCASim, the new simulator developed by our team exclusively for QCAs' quaternary mode. Proposed basic quaternary logic gates such as MIN, MAX, and different types of inverters (SQI, PQI, NQI, and IQI) have been designed and verified by QCASim. This study will exemplify how fast and accurately QCASim works by its handy set of CAD tools. A 1×4 decoder is presented using our proposed main gates. Preference points such as the minimum delay, area, and complexity have been achieved in this work. QQCA main logic gates are compared with quaternary gates based on carbon nanotube field-effect transistor (CNFET). The results show that the proposed design is more efficient in terms of latency and energy consumption.

Key words: Quantum-dot cellular automata (QCA); Quaternary logic; QCASim; Quaternary QCA (QQCA); Quaternary decoder; Quaternary gates

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1 Introduction

Proceeding to implement transistors to attain higher performances and locating them in smaller chips have been the main issues for every logic circuit designer from the past to present years (Wang and Xie, 2020). The challenge of scaling down the feature size of the metal-oxide semiconductor (MOS) has become more complicated in recent years because of its non-ideal and non-scalable characteristics like high leakage currents, high power density, and large parametric variations (Arulkarthick et al., 2020; Shalamzari et al., 2020). These issues have encouraged logic designers to focus on a replacement for the standard complementary MOS (CMOS). With the advent of advanced technologies such as quantum-dot cellular automata (QCA), many of these problems have been solved (Das and De, 2017; Debnath et al., 2019).

The use of more than two authorized logic levels in digital designs has attracted the attention of many logic designers over recent decades (Yasuda et al., 1986). Multiple-valued logic (MVL) is a promising way to conquer many design limitations. By merging two bits into a single quaternary digit, quaternary logic memories may store twice as much information as binary systems do (Daraei and Hosseini, 2019). Using quaternary systems helps reduce the number of inputs and outputs in a system's architecture. This issue assumes even greater importance in complicated

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circuits (Shahrom and Hosseini, 2018). Quaternary gates can be used in binary systems as well. Sharifi et al. (2016) used both quaternary-to-binary and binary-to-quaternary converters in a circuit. Note that each part of a circuit designed in binary or quaternary must obey its specific logic truth table.

QCA is a technology that can be modified to upper logic values. Increasing the number of quantum dots and altering the cell structure will engender a new MVL model (ternary QCA) (Mohaghegh et al., 2018b). Designing basic MVL gates and even intricate concepts such as adder, decoder, multiplier, and multiplexer can be neatly accomplished with QCA technology (Mohaghegh et al., 2018a, 2019). Binary and ternary models were proposed previously. Their superiority in energy consumption and area usage to standard CMOS has been documented.

In this study, a quaternary QCA (QQCA) is presented, and its specific simulator capable of simulating complex quaternary QCA circuits is introduced and exemplified. This tool uses an ultra-fast simulation engine that allows computation to be performed in a short time. QQCA's basics are clarified, and primary quaternary logic gates are described.

2 Basic principles of QCA technology

In this section, brief descriptions of QCA realization, implementation, and clocking are given.

2.1 QCA realization

Realization of the MVL QCA is analogous to that of binary QCA (Lent et al., 1993). These models of QCA have common points like implementation, clocking, and energy computation (Mohaghegh et al., 2018b). Each QCA cell is a square nano-structure with a definite number of quantum dots with differing positions based on the type of logic value; e.g., binary QCA (BQCA) has four quantum dots that have been placed at the corners. QCA was designed with two mobile electrons (Lent et al., 1994). According to the existing repulsion between electrons, these two tend to settle at their largest distance apart. Therefore, the way that these two electrons reside in those dots creates a specific stance. The number of situations is relevant to the QCA model, representing a polarization state known as a logic value.

2.2 QCA implementation

There are four methods for implementing QCA distinguished by the material used: metal island (Orlov et al., 1997), semiconductor (Perez-Martinez et al., 2007), magnetic (Cowburn and Welland, 2000), and molecular (Lent et al., 2003).

The first implementation method, metal island, has some limitations that make it improper for CMOS replacement. In this method, quantum dots are constructed by aluminum islands (Amlani et al., 2000) that are as big as one micron. Non-scalability is the main constraint of this method. Islands should be large so that the operation of electron switching becomes observable. The operating temperature is another major limitation; metal island QCA operates at a temperature of 70 mK (Orlov et al., 2001).

In the semiconductor method, quantum dots are created from a standard semiconductor material such as InAs/GaAs or GaAs/AlGaAs. The benefit of this method is that it is based on sufficiently well-known materials. Nevertheless, the cost of lithography for fabrication at a smaller feature size of 20 nm is untenable.

Magnetic implementation of QCA (MQCA) is based on the interaction between magnetic nanoparticles. Unlike in other types of QCA, there is no electron tunneling phenomenon. MQCA uses a magnetization vector instead of a polarization vector for presenting logic values (Bernstein et al., 2005).

The molecular method is considered an alternative implementation approach for avoiding the limitations of all other types. It can operate rapidly (in the order of THz) at room temperature with high device density (Lu and Lent, 2005). It is the most favorable method, especially for the MVL concept. MVL QCA models have more than four quantum dots. Although MVL QCA is currently in its infancy, strides are being made to introduce and represent new concepts (Arjmand et al., 2013; Mohaghegh et al., 2018b).

2.3 QCA clocking

The primary role of clocking in QCA is to control data flow. Each cell needs the power to fix its electrons in a stable position at a specific time and transfer the data to its neighbors (Kim et al., 2007). QCA's clocking contains four clock signals, each consisting of four phases: switch, hold, release, and relax. The frequencies of all clock signals are the

same, but they are shifted 90° from each other. Fig. 1 shows these four phases.

In the switch phase, barriers are raised, and electrons move to their positions. In the hold phase, barriers remain high, so each cell has a definite polarization. During the release phase, barriers are lowered, and electrons are freed. In the relax phase, cells are unpolarized (Vankamamidi et al., 2006). The clocking scheme is the same in BQCA and MVL QCA (Mohaghegh et al., 2018b).

3 Proposed concept

In this section, a novel QQCA concept is introduced. The configuration of cells, possible states expressing logic values, and energy calculation are discussed to clearly describe the concept and method used to structure the QCASim algorithm.

3.1 Configuration

Fig. 2 shows the four stable states representing a specific logic value. There are eight embedded quantum dots with a pair of mobile electrons in each cell. The activities of these electrons are based on Coulombic interaction. In this concept, each polarization state is defined with a letter. "*A*" has the highest logic value (absolutely high), "*C*" has the next highest (intermediately high) value, "*D*" has the intermediately low value, and "*B*" has the lowest logic value (absolutely low). Due to the quaternary logic, *A*, *C*, *D*, and *B* have values of 3, 2, 1, and 0, respectively.

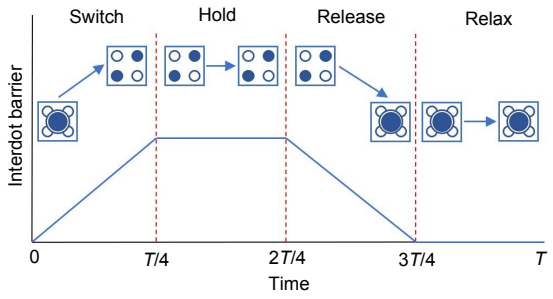

Fig. 1 QCA clocking phases

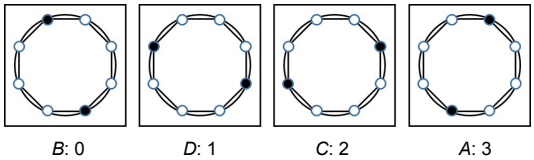

Fig. 2 Four possible states of QQCA cells

3.2 Cell dimension

The schematic of QQCA cells is based on a regular octagon. All eight quantum dots are placed at the corners of the octagon, which is surrounded by a square. Fig. 3 shows the inner and outer distances between these quantum dots. Two adjacent cells are placed horizontally. Cells can be placed either vertically or diagonally, and the cell's polarization will be distinct. The polarization of adjacent cells is then computed by energy calculation.

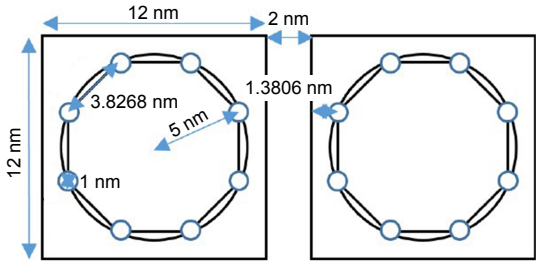

Fig. 3 QQCA cell's dimension

3.3 Energy calculation

Energy calculations are used to determine the status of cells' electrons. Energy is divided chiefly into two types, i.e., intracellular and extracellular. The intracellular energy comprises internal electrostatic energy, ground-state energy (non-clocking circuit), tunneling energy, and kinetic energy. Extracellular energy is external electrostatic energy. Examining all kinds of energy is not required for demonstrating our proposed concept, because external electrostatic energy has a major function in determining the adjacent cell's polarization. On the other hand, energy consumption is directly related to internal electrostatic energy. Information about the other kinds of energy can be found in Bahar et al. (2017).

One method for calculating the total energy consumption is to sum the internal energy E_{internal} of the individual cells and the total external energy E_{external} of the entire circuit (external energy between adjacent cells), as shown in Eq. (1):

$$\begin{aligned}&\text{Total energy consumption}\\&=E_{\text{internal}}\times\text{cell number}+E_{\text{external}}.\end{aligned}\tag{1}$$

Internal electrostatic energy is calculated for each cell individually. Each QQCA cell has a pair of electrons. The internal electrostatic energy is the

repulsive interaction between these two electrons, which can be obtained from Eq. (2):

$$E_{\text{internal}}=\frac{1}{4\pi\varepsilon_0\varepsilon_{\text{r}}}\sum_{i=1}^{m}\sum_{j=1}^{n}\frac{q_iq_j}{d_{ij}}, \tag{2}$$

where ε_0 and ε_{r} are the vacuum and substance relative permittivity coefficients respectively, q_i and q_j are the i^{th} and j^{th} charges of dots in a cell respectively, d_{ij} is the distance between these two charges, and n and m are both limited by the number of quantum dots (In BQCA, n and m are equal to 4, and in QQCA, n and m are equal to 8). The proposed QQCA quantum dots are placed on the circumference of a circle (Fig. 4). In other words, the octagon is surrounded by a circle. Therefore, the internal electrostatic energy for all four polarizations is expressed as

$$d_{a_1b_1}=10\text{ nm}\Rightarrow E_{\text{internal}}=2.304\times10^{-20}\text{ J}. \tag{3}$$

The external electrostatic energy is the repulsion interaction between two electrons from different cells. The obtainable value for this energy could also be obtained from Eq. (2); however, it should be calculated for two electrons that are not in a unit cell.

3.4 Simulation tool

Our QCA team has developed the only tool that is capable of simulating complex quaternary QCA circuits (https://bit.ly/3nFqdTj). QCASim's simulation engine is based on calculating the external electrostatic energy between each pair of adjacent cells. To achieve this goal, QCASim computes the distance between the electrons using geometric equations. It is explicit that two cells could be adjacent in horizontal, vertical, or diagonal direction with or without an interspace across.

The procedure of QCASim determines the adjacent cell's polarization by calculating each cell's effect on its neighbors (Navidi et al., 2021). For better realization, Fig. 4 exemplifies the process with two horizontally non-interspaced cells. Assume that the left cell is input with the highest logic value A, and that the right cell is output or a non-polarized cell. In this case, the simulator considers the output in four different polarizations and computes the external electrostatic energy in all four situations. Then, it compares the results and sets the proper polarization, based on the lowest energy value for the desired cell. QCASim uses the superposition principle in cases where several cells are located beside each other.

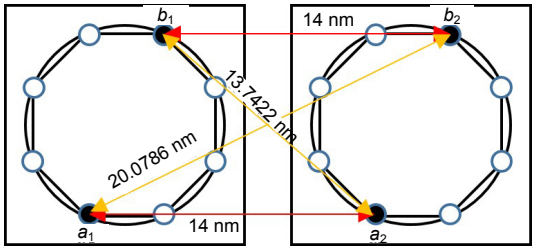

Fig. 4 Two cells next to each other (It is assumed that state *A* is adopted for the cell on the right)

The external electrostatic energy calculation for each distance between the electrons of two adjacent cells in Fig. 4 is as follows:

$$\begin{cases}E_{e_1}=E_{a_1a_2}=1.6457\times10^{-20}\text{ J},\\ E_{e_2}=E_{b_1b_2}=1.6457\times10^{-20}\text{ J},\\ E_{e_3}=E_{a_1b_2}=1.1474\times10^{-20}\text{ J},\\ E_{e_4}=E_{b_1a_2}=1.6765\times10^{-20}\text{ J}.\end{cases} \tag{4}$$

The ultimate energy quantity is obtained by subtracting the sum of energy with similar names from the sum of that with dissimilar names. In cases where this value is negative, the absolute value is desired. Eq. (5) shows the final energy value for two cells that are held in state A:

$$E_t=(E_{e_1}+E_{e_2})-(E_{e_3}+E_{e_4})=0.4675\times10^{-20}\text{ J}. \tag{5}$$

Fig. 5 demonstrates the simulation results for an input cell with three adjacent output cells which are set horizontally, vertically, and diagonally.

4 Proposed QQCA logic gates

In this section, the rudiments of QQCA logic are discussed. In the first step, the quaternary truth table is given (Jahangir et al., 2012; Ebrahimi et al., 2016). The behavior of adjacent cells was verified in the previous section. The designed primary quaternary logic gates are described which include wire, different

types of inverters, and MIN/MAX gates. At the end of this section, a 1×4 decoder is proposed and simulated.

The truth table of NOT, MIN, and MAX gates is shown in Table 1 by covering all possible combinations of inputs and their corresponding outputs. In the quaternary system, the AND and MIN gates are similar but not the same. The only difference is in the truth table. In the quaternary truth table, AND ("2," "1") is "0," but MIN ("2," "1") is "1." OR ("2," "1") is "3," but MAX ("2," "1") is "2," whereas in the binary truth table, the OR gate is exactly the MAX gate and the AND gate is exactly the MIN gate.

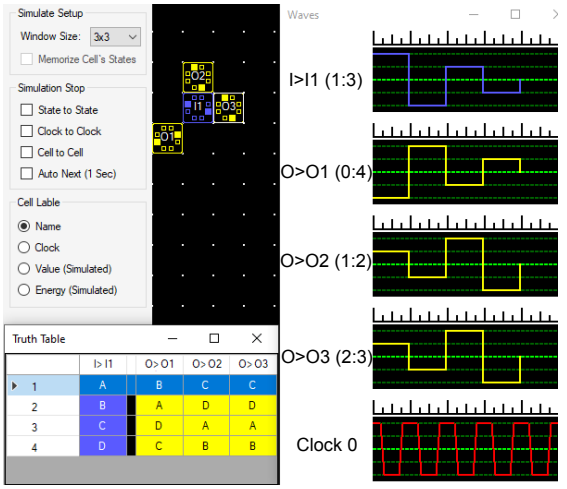

Fig. 5 Simulation for an input cell with three adjacent output cells (Output 1 is set diagonally, output 2 vertically, and output 3 horizontally)

Table 1 Truth table of quaternary logic

Input		NOT SQI	NOT NQI	NOT PQI	NOT IQI	MIN	MAX
In1	In2	In1	In1	In1	In1	In1 In2	In1 In2
0	0	3	3	3	3	0	0
0	1	3	3	3	3	0	1
0	2	3	3	3	3	0	2
0	3	3	3	3	3	0	3
1	0	2	0	3	3	0	1
1	1	2	0	3	3	1	1
1	2	2	0	3	3	1	2
1	3	2	0	3	3	1	3
2	0	1	0	3	0	0	2
2	1	1	0	3	0	1	2
2	2	1	0	3	0	2	2
2	3	1	0	3	0	2	3
3	0	0	0	0	0	0	3
3	1	0	0	0	0	1	3
3	2	0	0	0	0	2	3
3	3	0	0	0	0	3	3

According to the results shown in Fig. 5, the laterally horizontal/vertical cell beside an input cell with state *A* has a state *C*, and vice versa. The same is true for *B* and *D* states. *B* and *D* have low logic values, while *A* and *C* have high logic values (as mentioned in the previous section).

To form a wire in QQCA, an odd number of cells must be used. Fig. 6 shows the simulation results for both horizontal and vertical wires. I1 and O1 are input 1 and output 1, respectively (the horizontal wire). I2 and O2 are the corresponding input 2 and output 2 for the vertical wire, respectively.

It is necessary to place two cells diagonally to construct a standard quaternary inverter (SQI) (Fig. 7). Other types of inverters, like the positive quaternary inverter (PQI), negative quaternary inverter (NQI), and intermediate quaternary inverter (IQI) (also known as an outward inverter), are shown in Figs. 8, 9, and 10, respectively.

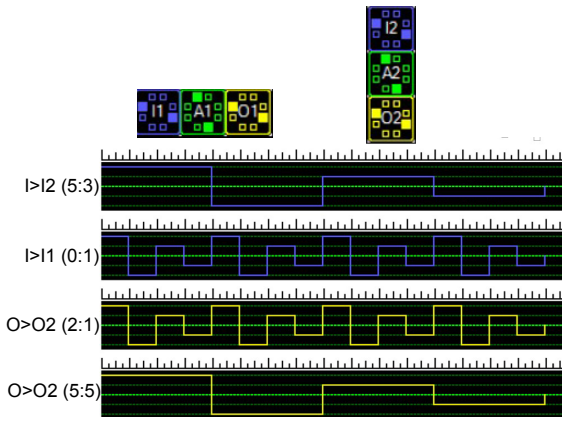

Fig. 6 Simulation of two separate wires (horizontally and vertically)

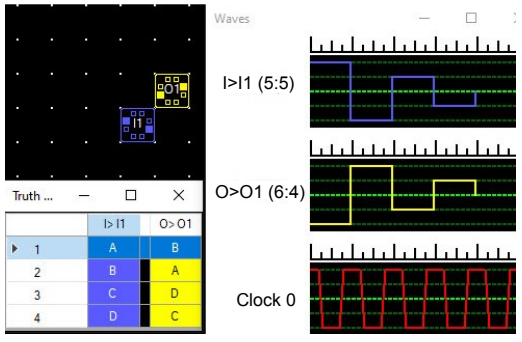

Fig. 7 Simulation of the standard quaternary inverter (SQI) (References to color refer to the online version of this figure)

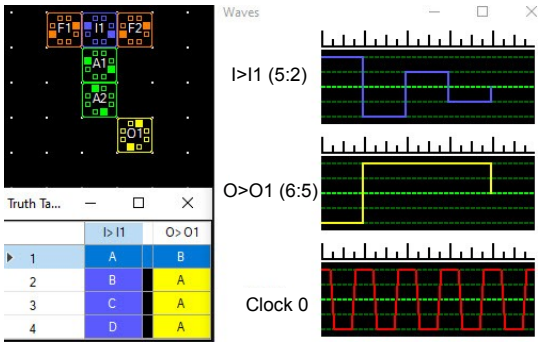

Fig. 8 Simulation of the positive quaternary inverter (PQI) (References to color refer to the online version of this figure)

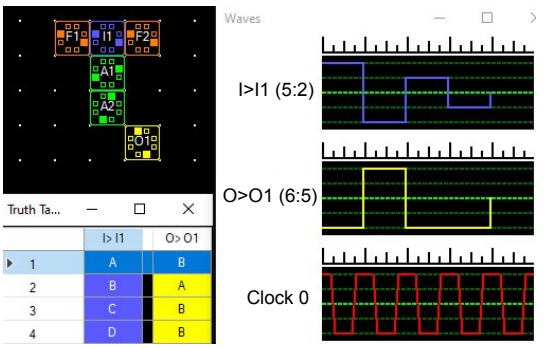

Fig. 9 Simulation of the negative quaternary inverter (NQI) (References to color refer to the online version of this figure)

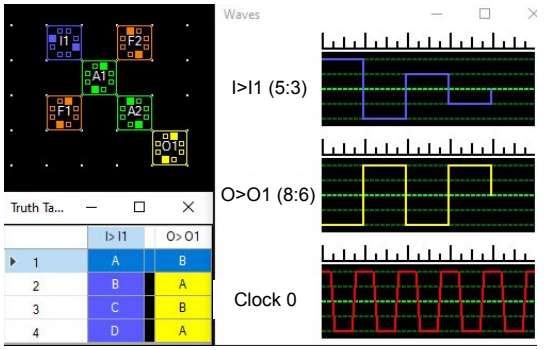

Fig. 10 Simulation of the intermediate quaternary inverter (IQI) (References to color refer to the online version of this figure)

Input, output, and fixed polarization cells are shown in blue, yellow, and orange, respectively. Nonpolarized cells (normal cells) vary in color depending on their clock signals; the four clock signals, switch, hold, release, and relax, are shown in green, purple, cyan, and white, respectively. The QCASim team attempted to develop a user interface similar to QCADesigner so that designers who had previously worked in the binary field would feel comfortable when working with this software (Walus et al., 2004).

To make MAX and MIN gates, it is necessary to use three input-majority gates with a fixed polarization input. In the MIN circuit, the polarization of orange cells (fixed-polarization cells) should be fixed at state *B* polarization, while in the MAX gate it should be at state *A* polarization. The quaternary majority gate has an odd number of inputs with an output that shows the most applied inputs' state (majority state among applied inputs). In quaternary logic, there are four different values. If two out of three or all the applied inputs have the same polarization state, the output will be in that polarization state. If all three inputs have different states, the output would be one of two values that construct a wire together (which depends on the location of the inputs and the output). The MAX and MIN gates are shown in Figs. 11 and 12, respectively. All of the combinations of inputs are considered for evaluating each gate. In Figs. 11 and 12, the numbers inside the cells and the colors of the cells both indicate the cells' clock zones.

By attaching a NOT gate (SQI) to the outputs of the MIN and MAX gates, the NMIN and NMAX gates will be obtained. Thus, the NMIN and NMAX gates have one more cell in comparison with MIN and MAX gates.

A quaternary decoder is a combinational logic circuit that takes *n*-quaternary digit code as an input and decodes it into 4^n values as an output. The quaternary decoder function is as follows: for each of the input quantities, only one of the outputs is activated. Table 2 shows the truth table of the 1×4 quaternary decoder (Haghparast and Monfared, 2017). The decoder is one of the main circuits used in complex designs. Even a 4:1 multiplexer can be designed by a 1:4 decoder. Therefore, every complicated combinational logic circuit can be designed with the multiplexer. The proposed decoder is shown in Fig. 13. In this design, D1–D4 is equivalent to D0–D3.

Table 2 Truth table of the 1×4 quaternary decoder

In1	D0	D1	D2	D3
B=0	3	0	0	0
D=1	0	3	0	0
C=2	0	0	3	0
A=3	0	0	0	3

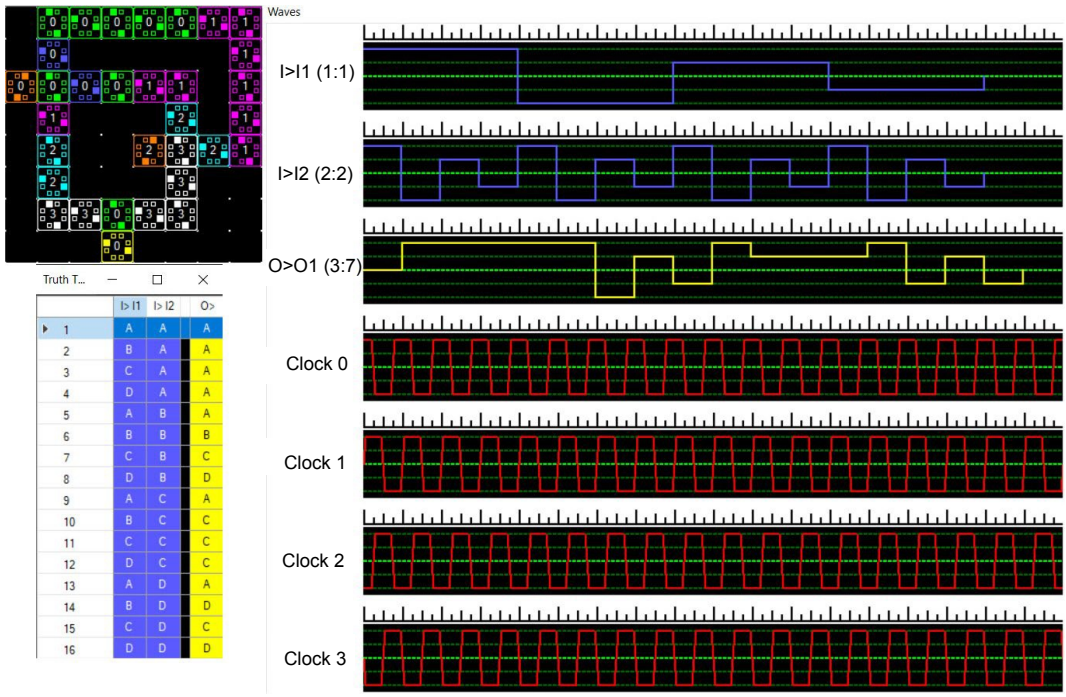

Fig. 11 Simulation of the MAX gate

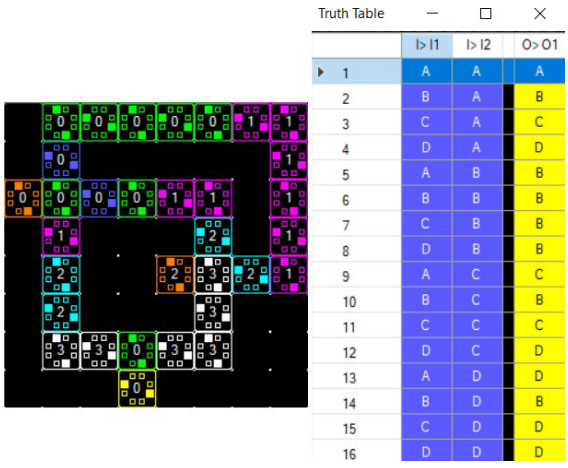

Fig. 12 Simulation of the MIN gate

The outputs have a one-clock cycle delay from their inputs (Figs. 11–13). QCASim's semi-ruler at the top of waveforms helps easily count the number of clock cycles for calculating the latency, which is especially useful in complicated designs.

5 Performance evaluation

5.1 Performance benchmark

In this subsection, a benchmark for evaluating QCASim's performance is presented. In this benchmark, four quaternary circuits, NOT (SQI), MIN, MAX, 1×4 decoder, were simulated 10 times in a row at a specified runtime (10 simulations took about 40 s). QCASim required only 565 KB of free space on a drive. Table 3 shows the benchmark results.

5.2 Simulation results

Although researchers have developed their quaternary designs using a range of new advanced technologies, most have used CNFET. However, a few studies using standard CMOS have been conducted (Yasuda et al., 1986; da Silva et al., 2006).

To evaluate the QCA design performance, an index named "Cost" has been designed, including area, delay, and the complexity (number of cells used) (Liu et al., 2014). Simulation results for all of the proposed QQCA designs are presented in Table 4. Eq. (6) shows the index definition (Oklobdzija, 2001):

$$\text{Cost}=\text{Area}\times\text{Delay}\times\text{Complexity}. \tag{6}$$

Table 5 shows a comparison between the proposed QQCA and some CNFET designs. Each of these technologies has its specific advantages. QCA is superior to CNFET in that it is much more flexible in

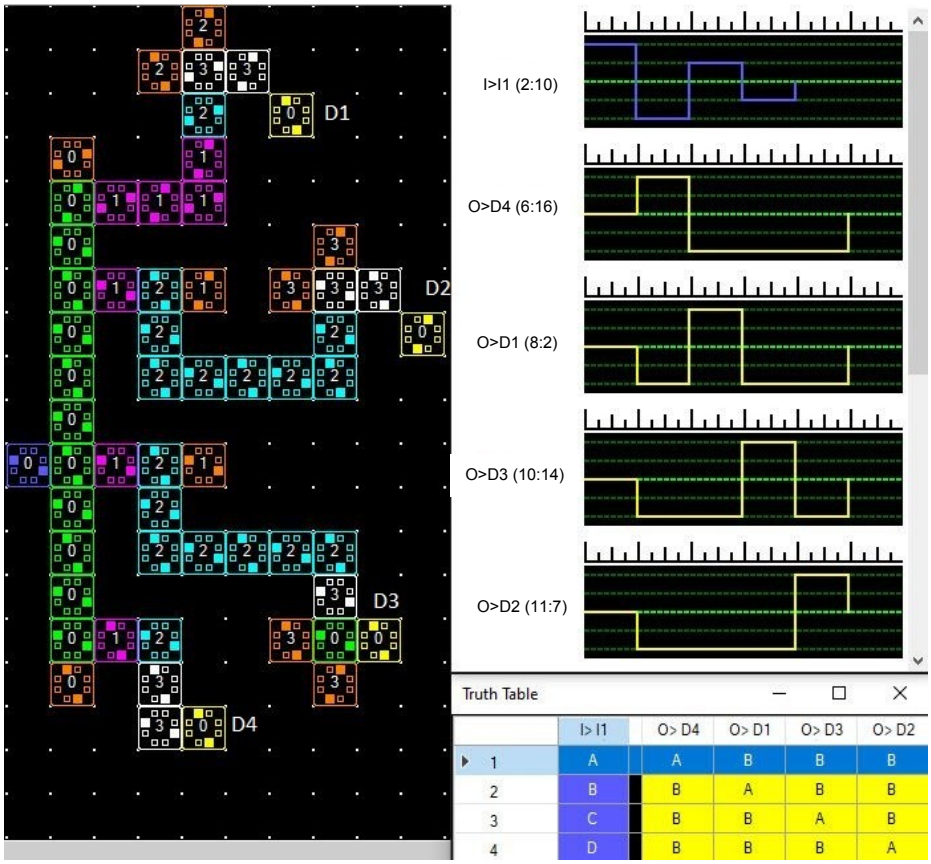

Fig. 13 Simulation of the 1×4 decoder

Table 3 Benchmark results for four quaternary circuits

Operating system	Number of active CPU threads	CPU average (%)*	Private memory** (KB)	Proposed design
Processor: Intel® Core™ i7-9750H@2.6 GHz	8	1.32	98 072	NOT (SQI)
Installed memory: 32.00 GB	16	1.56	266 468	MIN/MAX
Operating system: Windows 10	17	2.76	377 208	1×4 decoder

* Average percentage of CPU consumption by the process of 60 s; ** amount of physical memory in use by the process that cannot be used by other processes

Table 4 Simulation results of the proposed design

Design	Complexity*	Delay**	Area (μm^2)	Cost	Energy consumption (×10^{-20} J)
NOT (SQI)	2	0.25	0.0006	0.0003	4.6675
NOT (PQI)	6	0.25	0.0021	0.0031	15.9020
NOT (NQI)	6	0.25	0.0021	0.0031	15.9020
NOT (IQI)	6	0.25	0.0029	0.0043	14.8428
Majority	5	0.25	0.0016	0.0020	14.0341
MIN	32	1.25	0.0121	0.4840	80.8285
NMIN	33	1.25	0.0136	0.5610	83.1920
MAX	32	1.25	0.0121	0.4840	80.8285
NMAX	33	1.25	0.0136	0.5610	83.1920
1×4 decoder	58	1.25	0.0325	2.3562	145.8464

* Number of cells used; ** number of clock cycles

Table 5 Comparison between QQCA and CNFET designs

Method	Delay (ps)			Energy consumption (J)		
	NOT (SQI)	NMIN	NMAX	NOT (SQI)	NMIN	NMAX
Proposed	0.2	2.0	2.0	4.668×10^{-20}	83.192×10^{-20}	83.192×10^{-20}
Sharifi et al. (2015)'s	71.0	62.5	63.8	3.675×10^{-16}	3.960×10^{-16}	4.078×10^{-16}
Ebrahimi et al. (2016)'s	57.2	61.1	62.0	2.706×10^{-16}	3.172×10^{-16}	3.207×10^{-16}
Abiri et al. (2018)'s	36.9	36.3	35.5	1.263×10^{-16}	1.329×10^{-16}	1.320×10^{-16}

scalability and consumes less energy, as inferred from Table 5. In this comparison, the three main quaternary logic gates (NOT, NMIN, and NMAX) were compared.

Our proposed QQCA logic gates were more efficient in terms of delay and energy consumption in comparison with CNFET quaternary gates (Table 5). The energy consumption for our design was in the order of 10^{-20} J, compared with that in the order of 10^{-16} J for CNFET designs.

6 Conclusions

Designing multiple-valued logic (MVL) systems is a promising way to model and solve problems more conveniently than using binary logic. The capability of storing more information in a single bit is another advantage of these designs compared with standard binary designs. In this paper, a novel quaternary concept for quantum-dot cellular automata (QCA) is proposed. The energy relations governing this concept are based on Coulombic interactions, so electrostatic energies define the polarization of adjacent cells. Eight quantum dots with two agile electrons exist in the QQCA cell. There are four possible states at which the electrons can reside in those dots, which can be considered as logic values. All of the basic quaternary gates, including different types of inverters, MIN, and MAX, are simulated and evaluated by the accurate quaternary QCA simulator (QCASim). QCASim was created by our team, and it is available free of charge. This simulator can show results in both graphical formats and truth tables. A combinational logic circuit (1×4 decoder) is also proposed and simulated. Finally, the proposed quaternary main gates are compared with CNFET-based quaternary gates. The results show that QQCA designs are superior in terms of energy consumption and latency.

Contributors

Alireza NAVIDI and Reza SABBAGHI-NADOOSHAN designed the research. Alireza NAVIDI processed the data and drafted the manuscript. Reza SABBAGHI-NADOOSHAN helped organize the manuscript. Reza SABBAGHI-NADOOSHAN and Massoud DOUSTI revised and finalized the paper.

Compliance with ethics guidelines

Alireza NAVIDI, Reza SABBAGHI-NADOOSHAN, and Massoud DOUSTI declare that they have no conflict of interest.

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