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Review:

Analysis and design of transformer-based CMOS ultra-wideband millimeter-wave circuits for wireless applications: a review*

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Abstract: With a lot of millimeter-wave (mm-Wave) applications being issued, wideband circuits and systems have attracted much attention because of their strong applicability and versatility. In this paper, four transformer-based ultra-wideband mm-Wave circuits demonstrated in CMOS technologies are reviewed from theoretical analysis, implementation, to performance. First, we introduce a mm-Wave low-noise amplifier with transformer-based Gm-boosting and pole-tuning techniques. It achieves wide operating bandwidth, low noise figure, and good gain performance. Second, we review an injection-current-boosting technique which can significantly increase the locking range of mm-Wave injection-locked frequency triplers. Based on the injection-locked principle, we also discuss an ultra-wideband mm-Wave divider with the transformer-based high-order resonator. Finally, an E-band up-conversion mixer is presented; using the two-path transconductance stage and transformer-based load, it obtains good linearity and a large operating band.

Key words: CMOS; Millimeter-wave (mm-Wave); Ultra-wideband; Transformer; Low-noise amplifier; Injection-locked frequency tripler; Injection-locked frequency divider; Mixer

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1 Introduction

With the continuous rapid development of silicon semiconductor technologies, advanced complementary metal-oxide-semiconductor (CMOS) transistors have downscaled into the deep nanometer, whose characteristic and maximum oscillation frequencies are up to 300 GHz (Reynaert et al., 2017). They can implement millimeter-wave (mm-Wave) circuits and systems. Compared to III-V compound semiconductors, CMOS technologies have notable advantages of low cost, high reliability, and high integration. However, silicon-based mm-Wave circuits encounter several serious technical challenges to meet the requirement of commercial application, e.g., high noise figure (NF), low gain, low output power, and narrow operating bandwidth (Yao et al., 2007; Chen et al., 2013; Guo et al., 2016).

In recent years, several spectra in the mm-Wave regime have been issued sequentially for various wireless applications, including V band (57–65 GHz) for in-door high-speed wireless data transmission, 77 GHz for automotive radar, and 28 and 39 GHz for fifth generation (5G) mm-Wave wireless communication. All possess huge market potential. Therefore, mm-Wave wideband circuits have attracted tremendous attention in industrial and academic fields (Shahramian et al., 2013; Vigilante and Reynaert, 2018), especially those covering two or more frequency bands. They will greatly reduce the number and cost of wireless devices.

As a feature of high-order networks at the mm-Wave frequency, transformers have shown significant

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potential in the implementation of wideband circuits. In this paper, we review four transformer-based ultra-wideband CMOS circuits for several wireless applications: a 54.4-to-90 GHz low-noise amplifier (LNA) (Yu et al., 2017), a 22.8-to-43.2 GHz tuningless injection-locked frequency tripler (ILFT) (Zhang et al., 2019), a 32.3-to-61.9 GHz injection-locked frequency divider (ILFD) (Zhang et al., 2018), and an E-band up-conversion mixer (Chen ZN et al., 2019). Their working mechanism, implementation, and performance are described. We also briefly discuss some directions of research in ultra-wideband mm-Wave CMOS circuits and systems.

2 Ultra-wideband mm-Wave LNA

As the first active building block in a receiver, the LNA plays a significant role in guaranteeing the overall performance, particularly the sensitivity of wireless systems. To achieve a wide bandwidth, several techniques and topologies, such as magnetic coupling (Yeh et al., 2012), pole converging (Feng et al., 2017), the transformer-based fourth-order matching network (Vigilante and Reynaert, 2016b), and the T-type network (Liu and Schumacher, 2013), are proposed for mm-Wave LNAs design. However, these wideband LNAs suffer from high power dissipation, large chip area, or are at the cost of reduced radio frequency (RF) performances of linearity and NF.

Yu et al. (2017) proposed a novel transformer-based Gm-boosting method to obtain comparable power gain and NF for the wideband mm-Wave LNA. As shown in Fig. 1, a transformer is used between adjacent stages to replace the drain inductor of the former stage and the source-degeneration inductor of the following stage. A pole-tuning technique realized by a gate-series inductor is also applied to adjust the main pole of the inter-stage matching network. For multi-stage amplifiers, the peak gains of each stage can be separated with the pole-tuning technique, and the bandwidth of the circuit is therefore effectively increased.

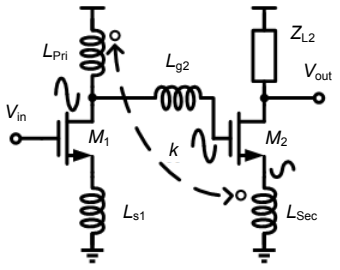

Fig. 1 Transformer-based topology for mm-Wave LNA design

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2.1 Analysis of the transformer-based topology

2.1.1 Gain

Based on Fig. 1, the effective transconductance of the second stage M_2 (G_{m2}) can be calculated by

$$G_{m2}=\left(1+\frac{M}{L'_{Pri}}\right)g_{m2}, \tag{1}$$

where L'_{Pri} means the equivalent inductance of the primary winding of the transformer considering the coupling effect, $M=k\sqrt{L_{Pri}L_{Sec}}$, M and k denote the mutual inductance and coupling coefficient of the transformer, respectively, and g_{m2} is the transconductance of M_2. It can be seen from Eq. (1) that the effective transconductance of M_2 is enlarged by a factor of $(1+M/L'_{Pri})$, compared with the one without the transformer. As a result, the total gain of the two-stage topology (A_{VF}) is increased:

$$A_{VF}(s)\approx\frac{G_{m2}\dfrac{\omega_{T1}}{s}}{2\sqrt{R_S(r_{g1}+\omega_{T1}L_{s1})}}\frac{(Z_{L2}\parallel r_{o2})\dfrac{L_{Pri}}{L_{Sec}}}{\dfrac{\omega_{T2}}{s}+1+\dfrac{sL_{g2}+\dfrac{1}{sC_{gs2}}}{sL_{Sec}}}, \tag{2}$$

where R_S, $\omega_{Ti}=g_{mi}/C_{gsi}$, r_{gi}, C_{gsi}, and r_{oi} represent the source resistance, angular cutoff frequency, gate parasitic resistance, gate-to-source parasitic capacitance, and channel modulation resistance of M_i, respectively.

As presented in Fig. 2, the simulated maximum stable power gain (G_{msg}) of the topology with the transformer is larger than that of the typical two-stage common-source (CS) topology with the source inductors (k=0 in Fig. 2). Also, with the increase of k of the transformer, G_{msg} will be further improved.

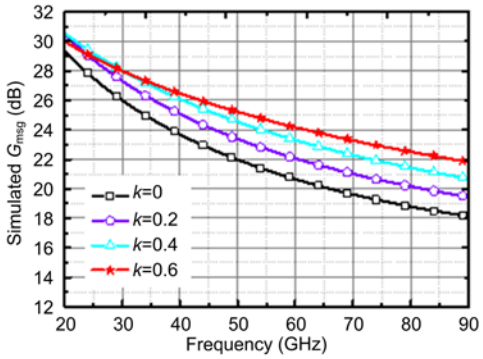

Fig. 2 Simulated maximum stable power gain (G_{msg}) of the proposed topology versus the coupling coefficient k of the transformer

2.1.2 Noise figure

Ignoring the noise contribution from the passive devices, the NF of the topology (NF_T) can be expressed as

$$NF_T \approx 10\lg(1+F_{g1}+F_{d1}+F_{g2}+F_{d2}), \tag{3}$$

where F_{g1}, F_{d1}, F_{g2}, and F_{d2} mean the noise factors contributed by the gate resistances and the channel currents of M_1 and M_2, respectively. Assuming that the input terminal matches well with R_S, the noise factors of M_1 (Fig. 3) are calculated as follows:

$$F_{g1}=r_{g1}/R_S, \tag{4}$$

$$F_{d1}=\frac{(2r_{g1}+\omega_{T1}L_{s1})^2}{r_{g1}+\omega_{T1}L_{s1}}\frac{s}{\omega_{T1}}\frac{\gamma_1}{\alpha_1}g_{m1}, \tag{5}$$

where $\alpha_i=g_{mi}/g_{d0i}$, and g_{d0i} and γ_i denote the zero-bias drain conductance and the coefficient of the channel thermal noise of M_i, respectively. According to Fig. 3, the output noise currents of M_2 can be deduced by

$$i_{g2}^{out}=\frac{i_{g2,n}r_{g2}\omega_{T2}/s}{\omega_{T2}L_{Sec}+sZI+(2s+\omega_{T2})M}, \tag{6}$$

$$i_{d2}^{out}=\frac{i_{d2,n}}{1+\frac{\omega_{T2}}{s}\frac{L_{Sec}+M}{ZI+2M}}, \tag{7}$$

$$ZI=L_{Pri}+L_{Sec}+L_{g2}+\frac{1}{s^2}C_{gs2}. \tag{8}$$

In this design, $ZI>2L_{Sec}$. Based on Eqs. (2), (6), and (7), F_{g2} and F_{d2} can be calculated as follows:

$$F_{g2}=\frac{\overline{(i_{g2}^{out})^2}(Z_L\|r_{o2})^2}{A_{VF}^2 4KTR_S}=\frac{(Z_L\|r_{o2})^2 r_{g2}(\omega_{T2}/s)^2}{A_{VF}^2[\omega_{T2}L_{Sec}+sZI+(2s+\omega_{T2})M]^2R_S}, \tag{9}$$

$$F_{d2}=\frac{\overline{(i_{d2}^{out})^2}(Z_L\|r_{o2})^2}{A_{VF}^2 4KTR_S}=\frac{\alpha_2 g_{m2}(Z_L\|r_{o2})^2}{\gamma_2 A_{VF}^2\left[1+\frac{\omega_{T2}}{s}\left(\frac{L_{Sec}+M}{ZI+2M}\right)\right]^2R_S}, \tag{10}$$

where K is Boltzmann's constant and T the temperature.

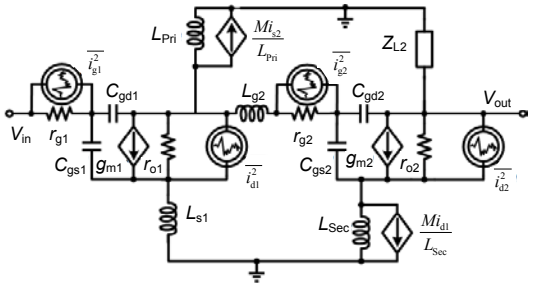

Fig. 3 Equivalent noise model of the proposed topology with channel thermal noise and gate resistance noise of MOS transistors

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From Eqs. (9) and (10), it can be inferred that both F_{g2} and F_{d2} are further reduced when M is positive, besides the improved A_{VF}. Thus, the transformer-based Gm-boosting technique can greatly decrease the noise power contributed by the second stage. The minimum NF (NF_{min}) of the topology is also simulated to verify the above analysis (Fig. 4). Compared to the typical one (k=0), the introduced topology's NF_{min} decreases. Also, it is further improved as k increases.

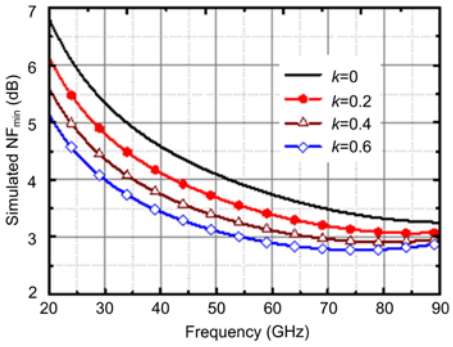

Fig. 4 Simulated minimum NF (NF_{min}) of the proposed topology with different k

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2.1.3 Bandwidth

As shown in Fig. 1, the inter-stage matching network of the topology is realized by the transformer and gate series inductor L_{g2}, whose main poles can be approximately derived by

$$s_{1,2} \approx \pm \mathrm{j}\sqrt{\frac{1}{(L'_{\mathrm{Sec}} + L_{g2})C_{gs2}}}, \tag{11}$$

where L'_{Sec} is the equivalent of the secondary winding of the transformer. According to Eq. (11), it can be inferred that $s_{1,2}$ relies on L_{g2}. The simulated transfer impedance (Z_{21}) with different L_{g2} is shown in Fig. 5. With the increase in L_{g2}, the peak moves to lower frequencies. For multi-stage amplifiers, the main pole of each inter-stage matching network can be separated at different frequencies by adjusting the gate series inductors. Therefore, the operating bandwidth will be extended.

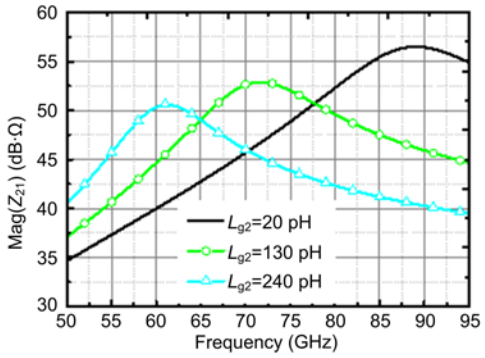

Fig. 5 Simulated Z_{21} of the inter-stage matching network with different L_{g2}
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2.2 Implementation of ultra-wideband LNA

As shown in Fig. 6. The LNA is composed of four common-source stages. The bias voltage of the transistors is optimized by SPECTRE simulation software for both a good NF and a low power consumption. The transistors' current density is about 250 μA/μm.

The rectangular shape is chosen to design the transformers to obtain a compact chip size (Figs. 7a and 7b). However, it comes at a cost of reduction in the quality factor (Q-factor) and coupling coefficient of the transformer (Gao et al., 2015). According to the analysis, the performances of gain and NF are strongly related to the coupling coefficient. Thus, a coupling-enhancement technique is used to alleviate this problem. The idea is to add a parallel coil with a larger physical size to the secondary winding (Fig. 7b). With the parallel coil, the overlapping area between the primary and secondary windings is increased compared with the typical transformer (Fig. 7a). Therefore, the magnetic flux between the two windings is enhanced, and k is enlarged (Fig. 7c).

To extend the gain bandwidth of the proposed LNA, the gate series inductors (L_{G1}, L_{G2}, and L_{G3}) are independently adjusted to separate the resonating frequencies of the three inter-stage matching networks. In this design, L_{G1}, L_{G2}, and L_{G3} are set at 116, 240, and 49 pH, respectively. As a result, the simulated main poles of the first, second, and third inter-stage matching networks are separated, located at 87, 66, and 107 GHz, respectively (Fig. 8).

2.3 Measurement results of ultra-wideband LNA

The LNA has been designed and fabricated with commercial 65 nm CMOS technology. It consumes

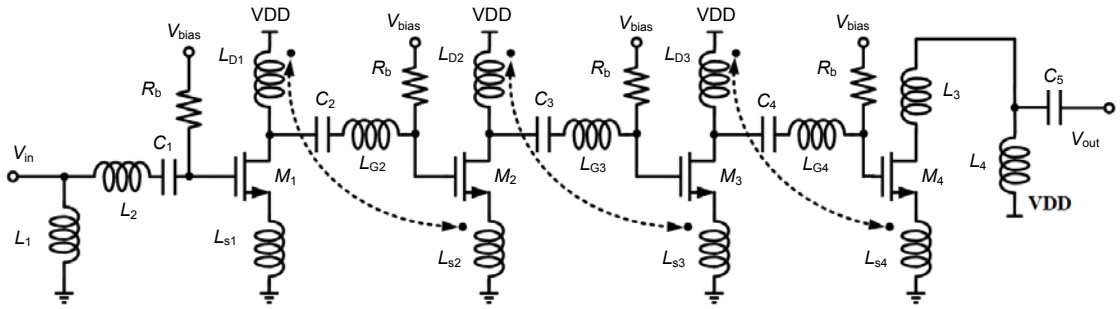

Fig. 6 Schematic of the proposed LNA
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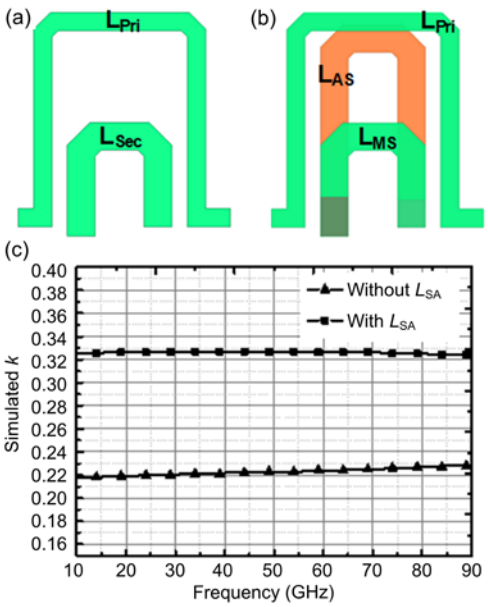

Fig. 7 Physical layout of the typical transformer (a), physical layout of the proposed transformer with a parallel coil in the secondary winding (b), and simulated coupling coefficients of the transformers with and without the parallel coil (c)

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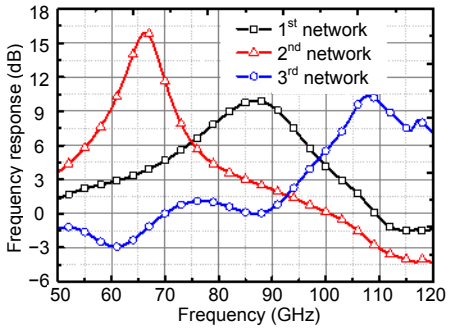

Fig. 8 Simulated frequency responses of the three interstage networks

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19-mA DC current under the voltage supply of 1 V. The die micrograph is shown in Fig. 9. With all the testing pads, its chip size is only 0.37 μm^2.

The measured *s* parameters are presented in Fig. 10. The tested maximum gain is 17.7 dB at 67 GHz. The 3-dB gain bandwidth is 35.6 GHz (from 54.4 to 90 GHz). The fractional bandwidth of the LNA is up to 49.3%. The measured NF is 5.4–7.4 dB from 54 to 67 GHz and agrees well with the simulation results, as shown in Fig. 11. The 1-dB input compression point (IP_{1dB}) of the LNA is also tested. This is between −15.4 and −11.7 dBm in the 3-dB gain frequency band. The chip performance is summarized and compared with the state-of-the-art mm-Wave LNAs in Table 1. A remarkable bandwidth and better or comparable NF and linearity with the lowest DC power dissipation are achieved, compared to the other works.

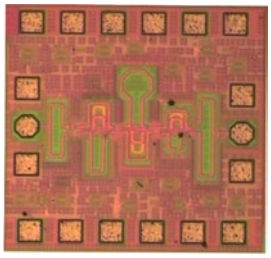

Fig. 9 Die photo of the wideband LNA

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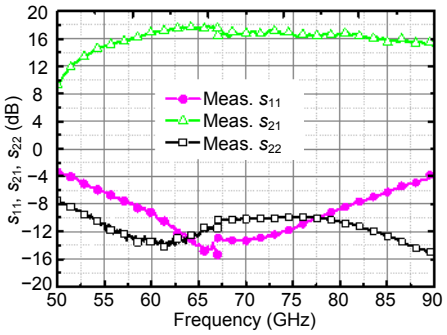

Fig. 10 Measured *s* parameters of the LNA

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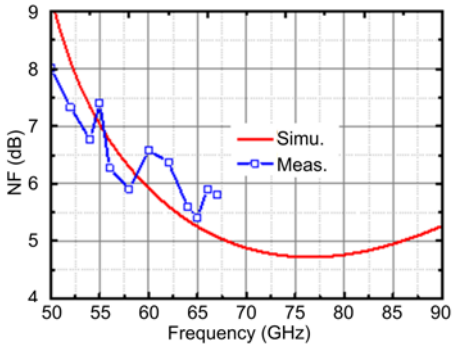

Fig. 11 Measured and simulated noise figure (NF)

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Table 1 Performance summary and comparison of the LNA

Reference	Process	Peak gain (dB)	BW (GHz)	FBW	NF (dB)	IP_{1dB} (dBm)	P_{DC} (mW) (VDD)	Chip area (mm^2)
Vigilante and Reynaert, 2016b	28 nm CMOS	29.6	28.3 (68.1–96.4)	34.4%	6.4–8.2	−28.1	31.3 (0.9 V)	0.254*
Liu and Schumacher, 2013	0.25 μm BiCMOS	22.5	30 (47–77)	48.4%	6.0–7.2	−17	52.0 (2.5 V)	0.5
Feng et al., 2017	65 nm CMOS	18.5	30 (62.5–92.5)	38.7%	5.5–7.9	−15@80 GHz	27.0 (1.8 V)	0.24
Yeh et al., 2012	90 nm CMOS	17.0	17 (46–63)	31.1%	4.4	−16	19.2 (1.2 V)	0.59
Fritsche et al., 2015	28 nm CMOS	13.8	18 (54.5–72.5)	28.3%	4.0	−12.5	24.0 (2 V)	0.38
Chen et al., 2012	0.18 μm BiCMOS	25.0	27 (86–113)	20.8%	8.3	NA	52.5 (1.8 V)	0.114*
Yu et al., 2017	**65 nm CMOS**	**17.7**	**35.6 (54.4–90)**	**>49.3%**	**5.4–7.4**	**−15.4–−11.7**	**19.0 (1 V)**	**0.37**

* Core area. BW: bandwidth; FBW: fractional bandwidth; NF: noise figure. NA: not available

3 Ultra-wideband injection-locked frequency tripler

For wideband mm-Wave transceiver front ends, the local oscillator (LO) is the one of the most serious challenges. A higher data rate usually requires a wider bandwidth and more complex modulation schemes, which will lead to more stringent requirements of the phase noise and a larger frequency range for LOs (Khanzadi et al., 2014; Zong et al., 2016). Besides these, phased-array transceivers and multiple input multiple output (MIMO) systems create new needs for LOs, e.g., low power consumption and high efficiency.

mm-Wave oscillators usually encounter a lot of technical problems, including poor phase noise, limited tuning range, and high power consumption in CMOS processes (Sadhu et al., 2015; Yanay and Socher, 2015; Vigilante and Reynaert, 2016a). Frequency multiplications, which need only low-frequency oscillators, may be a good solution for mm-Wave LO generations. Meanwhile, by allocating the frequency multiplier close to the mixer of each channel, it is easier to distribute the LO signal to multiple front-end channels. The key requirements going to frequency multipliers are large operating bandwidth and low power consumption with sufficient output power and harmonic rejections. The injection-locked frequency multiplier (ILFM) is popularly chosen to implement such frequency multiplications, because of its potential of high efficiency and low power dissipation. Several efforts have been made to increase the frequency range of mm-Wave multipliers. Low quality factor resonator (Chan and Long, 2008), varactors or digital capacitor arrays (Deng et al., 2013; Shin and Koh, 2018), and coupled-LC resonators (Li et al., 2014; Mangraviti et al., 2015) are proposed to extend the locking range. However, they still face several problems, such as high power consumption and complex tuning (calibration) circuit.

An injection-current-boosting (ICB) technique was introduced to increase the locking range of ILFT in Zhang et al. (2019). It is realized by a transformer-based sixth-order injection-coupling network. The parasitic capacitances of injection devices are resonated out over a wide frequency band with the network, and the injection current is boosted greatly. Therefore, the locking range of the tripler is significantly increased.

3.1 Analysis of the ICB technique

3.1.1 Locking range of the injection-locked oscillator

The injection-locked oscillators have been modeled by a linear model given by Razavi (2004), as shown in Fig. 12a. The tank current I_T of the resonator is formed by the injection current I_{inj} and oscillation current I_{osc}. Fig. 12c depicts the phasor diagram of I_{inj}, I_{osc}, and I_T. According to the analysis in Razavi (2004) (Chen ZN et al., 2019), the maximum phase difference φ_{max} between I_{osc} and I_T is given by

$$\varphi_{\max}=\pm\arcsin\left(\left\|\boldsymbol{I}_{\mathrm{inj},\omega}\right\|/\left\|\boldsymbol{I}_{\mathrm{osc},\omega}\right\|\right). \tag{12}$$

From Eq. (12), it can be inferred that the ILFT can be locked by the injection signal, when the phase shift generated from the load resonator is less than $\varphi_{\max}$. According to Eq. (12), $\varphi_{\max}$ can be increased by the following methods: (1) Reduce the oscillation current I_{osc}. However, this may degrade the output power of the oscillator. (2) Enlarge the injection current I_{inj}. This can be a much more reasonable way to extend the locking range (Fig. 12d).

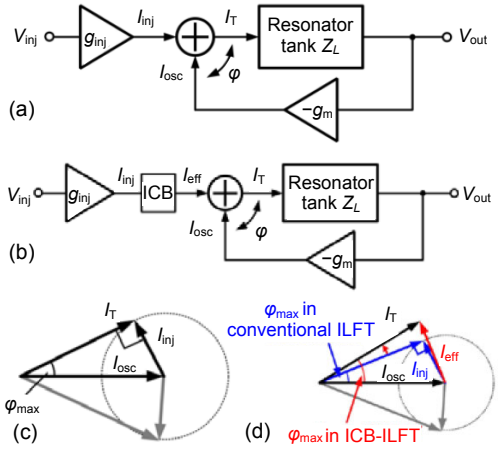

Fig. 12 Behavior model of the conventional ILFT (a), behavior model of ICB-ILFT (b), phasor diagram of ILFT and limitations on injection locking (c), and comparison between the conventional and ICB-ILFT in the phasor diagram (d)

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3.1.2 Injection current of ICB-ILFT

To analyze and compare the injection currents of the conventional ILFT and ICB technique based ILFT, we give their simplified half circuit models in Figs. 13 and 14, respectively. According to Fig. 13b, the ratio between I_{inj} and the ideal current source I_{i}, which represents the current of the injection transistor M_{inj}, can be deduced by

$$G_{\mathrm{conv}}=\frac{I_{\mathrm{inj}}}{I_{\mathrm{i}}}=\frac{s^2L_{\mathrm{T}}C_{\mathrm{T}}-s\left(C_{\mathrm{i}}r_{\mathrm{T}}+\dfrac{L_{\mathrm{T}}}{R_{\mathrm{i}}}\right)+1-\dfrac{C_{\mathrm{tot}}r_{\mathrm{T}}^2}{L_{\mathrm{T}}}-\dfrac{r_{\mathrm{T}}}{R_{\mathrm{i}}}}{s^2L_{\mathrm{T}}C_{\mathrm{tot}}-\dfrac{C_{\mathrm{tot}}r_{\mathrm{T}}^2}{L_{\mathrm{T}}}+1}, \tag{13}$$

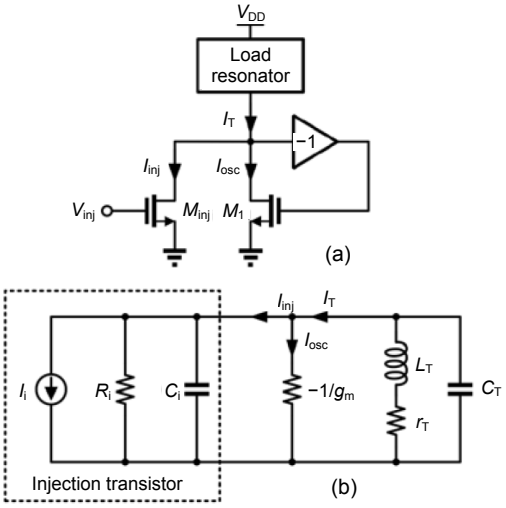

Fig. 13 Conventional ILFT: (a) simplified half-circuit model; (b) equivalent small-signal model

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where $C_{\mathrm{tot}}=C_{\mathrm{i}}+C_{\mathrm{T}}$. From the small signal model of the ICB-ILFT shown in Fig. 14b, it can be seen that the parasitic capacitance C_{i} generated by the injection transistor will be resonated by the transformer. The resonating frequency is strongly related to the physical size of the transformer. Thus, the resonating frequency can be shifted to a slightly higher value than the oscillating frequency by adjusting the transformer, and the current-boosting gain $G_{\mathrm{ICB}}=I_{\mathrm{eff}}/I_{\mathrm{i}}$ can attain a wider frequency band, which is acquired by

$$G_{\mathrm{ICB}}=sk\sqrt{L_{\mathrm{p}}L_{\mathrm{s}}}R_{\mathrm{i}}\left[s^3(1-k^2)L_{\mathrm{p}}L_{\mathrm{s}}C_{\mathrm{i}}R_{\mathrm{i}}+s^2(1-k^2)L_{\mathrm{p}}L_{\mathrm{s}}+sL_{\mathrm{s}}R_{\mathrm{i}}+(Z_L-1/g_{\mathrm{m}})(s^2L_{\mathrm{p}}C_{\mathrm{i}}R_{\mathrm{i}}+sL_{\mathrm{p}}+R_{\mathrm{i}})\right]^{-1}. \tag{14}$$

Based on Eqs. (13) and (14), the G_{conv} and G_{ICB} varying with the different frequencies are plotted in Fig. 15. It can be seen that G_{ICB} has two peaks. One is located at the oscillation frequency, and the other is at a higher frequency caused by the resonance of C_{i} and the transformer. Compared with the conventional one, as shown in Fig. 15, G_{ICB} and its bandwidth are much increased. As a result, the injection current is remarkably boosted by the ICB technique. Thanks to the application of the ICB transformer, the impedance in ICB-ILFT is much larger than that in the conventional ILFT. Thus, the required negative impedance ($-1/g_{\mathrm{m}}$) of ICB-ILFT is smaller. It may consume less power than the conventional ones.

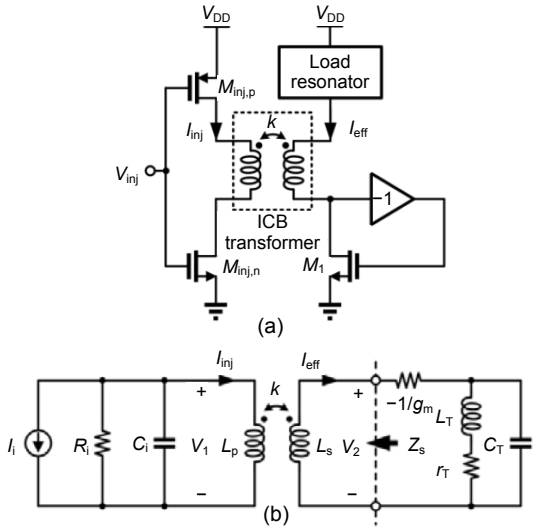

Fig. 14 ICB-ILFT: (a) simplified half-circuit model; (b) small-signal model

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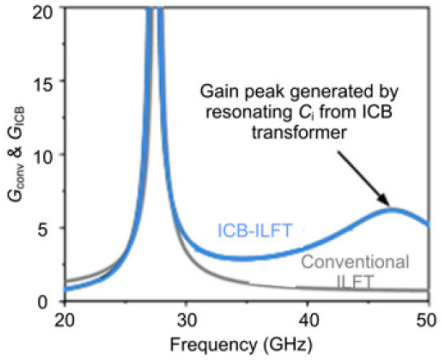

Fig. 15 Simulated G_{ICB} and G_{conv}

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3.1.3 Comparison between conventional ILFTs and ICB-ILFT

As shown in Fig. 16, the conventional ILFTs with the *LC*-tank and fourth-order transformer-based resonator (Li et al., 2014; Mangraviti et al., 2015; Zhang et al., 2019) are used to evaluate the advantages of the proposed ICB technique. The parasitic capacitance (C_c) imported by the cross-coupled pairs is considered. This has an impact on the resonating frequencies. To obtain a fair comparison, the oscillation frequencies and the quality factor of the loads are tuned to the same value separately in the three ILFTs. The simulated load impedances of the three topologies are presented in Fig. 16. It can be seen that both of ILFTs with the conventional fourth-order resonator and the ICB transformer, with two peaks, show flattened phase responses around zero degree. It follows that these two ILFTs can achieve a wider locking range.

To further compare ICB-ILFT with the conventional ILFTs, the effective current-boosting gain is defined as

$$G_{\text{eff}} = \frac{G_{\text{ICB}}}{G_{\text{conv}}}. \tag{15}$$

Based on Eq. (15), two effective current-boosting gains, $G_{\text{ICB}}/G_{\text{LC-tank}}$ and $G_{\text{ICB}}/G_{\text{4th-order}}$, are calculated (Fig. 17a). It can be seen that the two effective current-boosting gains are larger than 0 dB. It indicates that the injection current is significantly enlarged with the ICB technique. The locking ranges are also simulated (Fig. 17b). Compared to the two

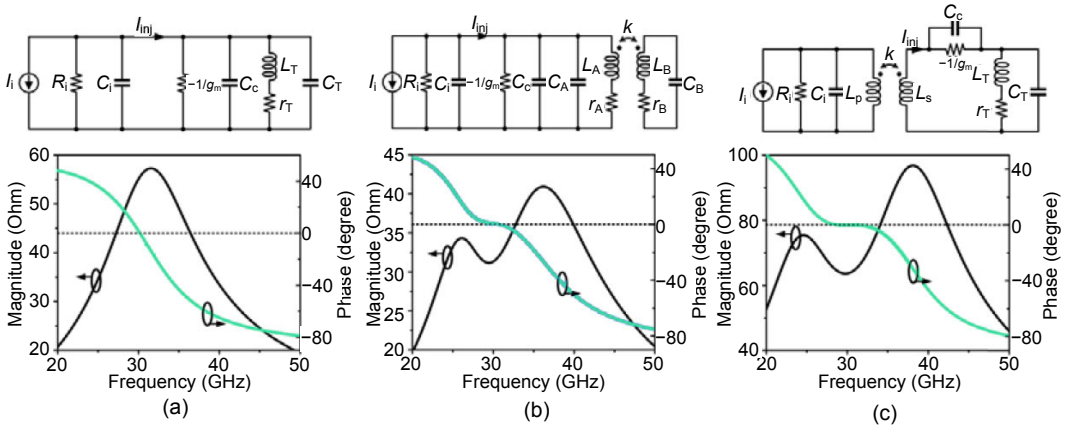

Fig. 16 Simplified equivalent models of three resonators and their simulated impedances seen from the cross-coupled pairs: (a) conventional *LC*-tank resonator; (b) conventional fourth-order-tank resonator; (c) proposed ICB transformer

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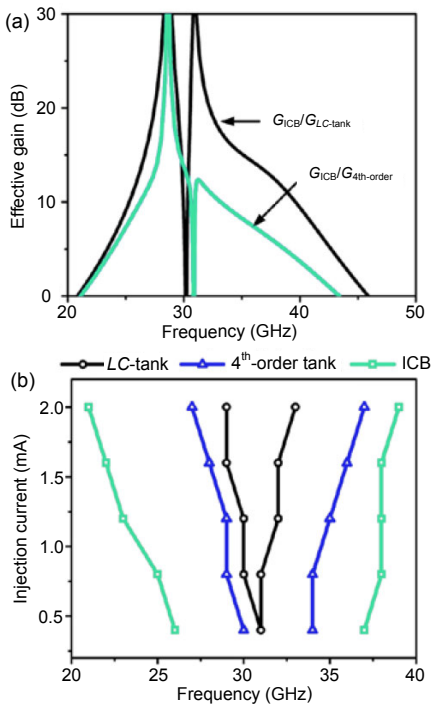

Fig. 17 Simulated effective current-boosting gains (a) and simulated locking ranges of the three topologies (b)
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conventional topologies, ICB-ILFT achieves the largest bandwidth.

3.2 Circuit implementation of ICB-ILFT

3.2.1 Transformer-based sixth-order resonator

A three-winding transformer and three tuning capacitors are applied to implement a sixth-order resonator to reduce the phase variation of ILFT with the frequency. The design procedure can be divided mainly into four steps. First, build up a simplified equivalent circuit model for the resonator; second, simulate the impedance seen from the cross-coupled pair and determine the available negative impedance ($-1/g_m$) from the real and imaginary parts of the impedance; third, tune the parameters or size of the resonator to obtain a flattened phase response for an optimum locking range; finally, calculate the current-boosting gain to estimate the bandwidth.

3.2.2 ICB-ILFT

As shown in Fig. 18a, ICB-ILFT is implemented with differential output terminals. Two negative channel metal oxide semiconductor (NMOS) transistors are used to form the cross-coupled pair to generate the required negative resistance. The sixth-order transformer realized by a staked structure functions as a load of the tripler. The top two metals are applied to design the transformer for a good quality factor. To increase the injection current, complementary topology is used to realize the injection circuit. Compared to the conventional injection circuit formed by an NMOS transistor, the complementary topology has better injection efficiency. This is because it works as a push–pull structure, which will create more injection current under the same injection power. The coupling coefficient of the transformer-based resonator is set relatively low for a wide frequency response. The capacitance C_s at the secondary coil and C_t at the tertiary coil are designed to tune the impedance of the resonator. The signal is output at the drain nodes of the cross-coupled pair.

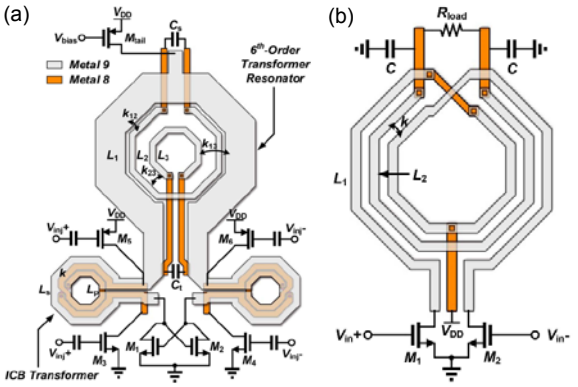

Fig. 18 Implementations with its layout view: (a) ICB-ILFT; (b) output buffer
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3.2.3 Output buffer

An output buffer is applied in this circuit to achieve a sufficient output power and drive the 50-Ω load of the measurement equipment. However, the output buffer faces the same challenge of wide bandwidth. As shown in Fig. 18b, a transformer-based load, which can function as a fourth-order resonator, is adopted in the buffer. It can increase the operating bandwidth excellently.

3.3 Measurement results of ICB-ILFT

ICB-ILFT is demonstrated by a 65-nm CMOS process. The chip micrograph is presented in Fig. 19. The chip size is 670 μm×700 μm, whereas the core circuit occupies only 270 μm×330 μm. The total

power consumption is 14.8 mW under 1-V voltage supply, of which the core injection-locked oscillator consumes 5 mW.

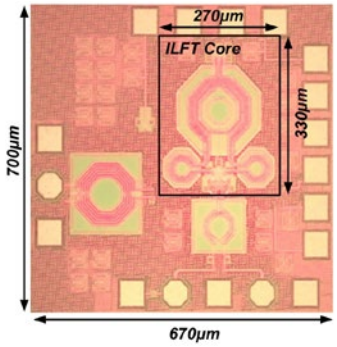

Fig. 19 Chip micrograph of ICB-ILFT
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As shown in Fig. 20a, with 0-dBm injection power, the locking range is from 22.8 to 51 GHz, and the fractional bandwidth is 76.4% of the center frequency. While for ICB-ILFT there is an in-band locking loss with the injection power lower than −1.5 dBm, it still covers all of the bands for 5G mm-Wave wireless communication. The simulation results (Fig. 20a) match well with the measurement results. The tested phase noise from 22.8 to 45.6 GHz is presented in Fig. 20b. It degrades around 9 dB from 22.8 to 43.2 GHz at both 100 kHz and 1 MHz offset. The tested degradation value of phase noise is close to the theoretical one, whereas it deteriorates severely above 43.2 GHz. One of the possible reasons is that the output power is low above the frequencies of 43.2 GHz, so that the phase noise at a low level is submerged by the white noise of measurement equipment. The fundamental rejection is also considered for the frequency tripler. Fig. 20c shows the measured output power and fundamental rejection. The output power is about −20 dBm, except the one above 41 GHz. The fundamental power is less than −50 dBm. At high frequencies, the fundamental rejection becomes poor, because of the bad performance of the output buffer above 40 GHz. The second harmonic rejection is also better than 40 dBc (Fig. 20d). At 39 GHz, the second harmonic rejection is smaller than 20 dBc (Fig. 20d). The reason for this is that ILFT is tested by single-ended equipment. In fact, the second harmonic can be suppressed by the differential structure. The performance of ICB-ILFT is summarized and compared with those of state-of-the-art frequency synthesizers in Table 2. ICB-ILFT achieves the largest locking range and good noise performance.

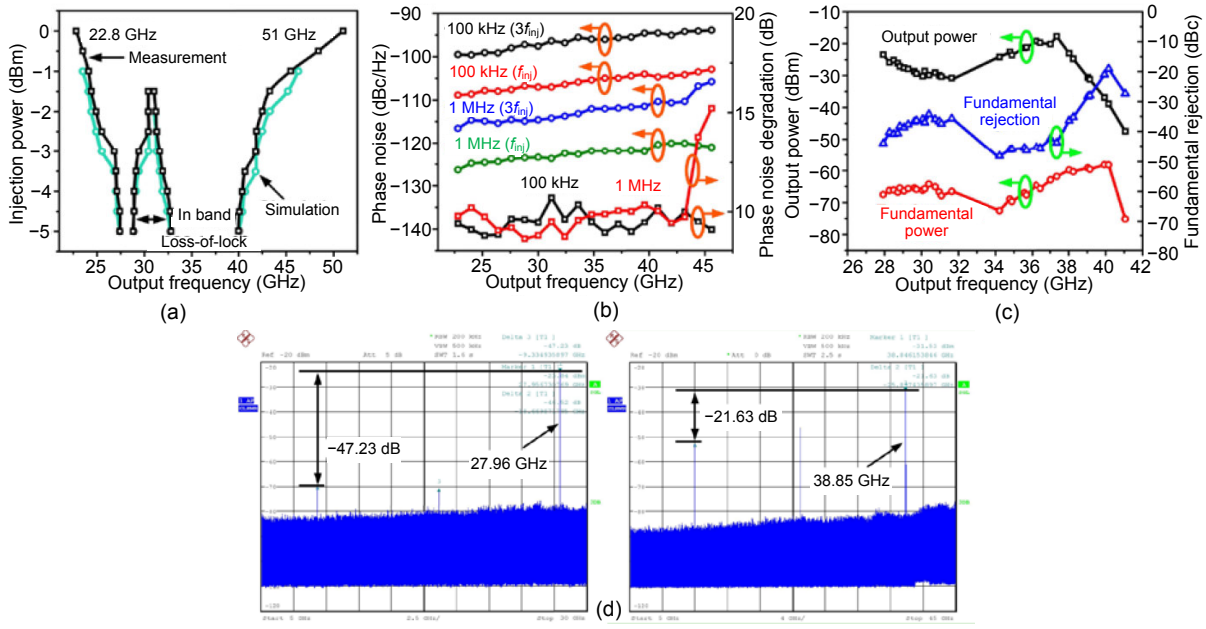

Fig. 20 Tested and simulated locking ranges of ICB-ILFT (a), measured phase noise and phase-noise degradation (b), tested output power and fundamental rejection (c), and measured output spectra at 28 and 39 GHz (d)
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Table 2 Performance summary and comparison of ILFT

Reference	Process	Phase	Output frequency (GHz)	Bandwidth (%)	PN at 1 MHz (dBc/Hz)	Power (mW)	Chip area (mm^2)
Wu et al., 2013	130 nm SiGe BiCMOS	Diff.	27.9–37.8	30.1	−104.0	10 (VCO only)	1.93
Kim et al., 2018	28 nm CMOS	Quad.	25.8–28.0	8.2	−108.5	NA	7.3/1.67
Shin and Koh, 2018	130 nm CMOS	Quad.	26.5–29.7	11.4	−106.7	49.7/23.2	1/0.08
Yoo et al., 2018	65 nm CMOS	Quad.	27.4–30.8	11.7	−115.6	24.3 (ILFM only)	0.72/0.11
Li et al., 2014	65 nm CMOS	Diff.	20.6–35.2	53.2	−113.9	148.3/[21.8/16.8]	2.1
Zhang et al., 2019	**65 nm CMOS**	**Diff.**	**22.8–43.2**	**61.8**	**−114.0**	**14.8/5.0**	**0.47/0.09**

PN: phase noise. NA: not available

4 Ultra-wideband injection-locked frequency divider

In mm-Wave frequency synthesizers, the first-stage frequency dividers always place restrictions on their operating bandwidth. Current-mode-logic dividers (Ghilioni et al., 2013; Hussein and Paramesh, 2017), regenerative dividers (Rong and Luong, 2010; Lin and Wang, 2016), and injection-locked frequency dividers (ILFD) (Jang et al., 2011; Lin and Liu, 2011; Imani and Hashemi, 2017) are potential solutions for mm-Wave applications.

To achieve ultra-wideband mm-Wave dividers, an injection-locked frequency structure with transformer-based high-order resonators is reported (Zhang et al., 2018). Similar to the ILFT introduced in the above section, high-order resonators can achieve a flat phase response within a wide frequency band, and lead to a wide locking range. Moreover, the inductive gain peaking technique was used for low power considerations in Zhang et al. (2018).

4.1 Analysis of the transformer-based high-order resonator

4.1.1 Locking range limitations

As shown in Fig. 21a, the conventional ILFD consists mainly of a cross-coupled pair, a resonator, and an injection circuit. A simplified behavior model is adopted to analyze the locking range of ILFD (Fig. 21b). The injection device M_{inj} is modeled by a mixer together with an adder. A g_{m} gain cell, a feedback network, and the LC-tank $Z_{L,\omega}$ are used to form the oscillator. The injection signal $V_{\text{inj},2\omega}$ at the gate of M_{inj} will be mixed with the output signal $V_{\text{out},\omega}$ at the drain (source) of M_{inj} and generate the mixed current $I_{\text{mix},\omega}$. The total current in the LC tank is equal to

$$I_{\text{T},\omega}=I_{\text{mix},\omega}+I_{\text{out},\omega}, \tag{16}$$

where

$$I_{\text{mix},\omega}=g_{\text{mix}}V_{\text{inj},2\omega}, \tag{17}$$

$$I_{\text{out},\omega}=g_{\text{m}}V_{\text{out},\omega}, \tag{18}$$

$$V_{\text{out},\omega}=I_{\text{T},\omega}Z_{L,\omega}. \tag{19}$$

$I_{\text{out},\omega}$ means the current generated by the cross-coupled pair at node A. g_{m} and $Z_{L,\omega}$ represent the transconductance of the cross-coupled pair and load impedance, respectively. g_{mix} is the transconductance of the mixer, regarded as a constant. As shown in Fig. 21c, the maximum phase difference ($\varphi_{\max}$) between $I_{\text{T},\omega}$ and $I_{\text{out},\omega}$, which indicates the locking range of ILFDs, can be calculated by (Razavi, 2004)

$$\sin\varphi_{\max}=\pm\left|I_{\text{mix},\omega}\right|/\left|I_{\text{out},\omega}\right|. \tag{20}$$

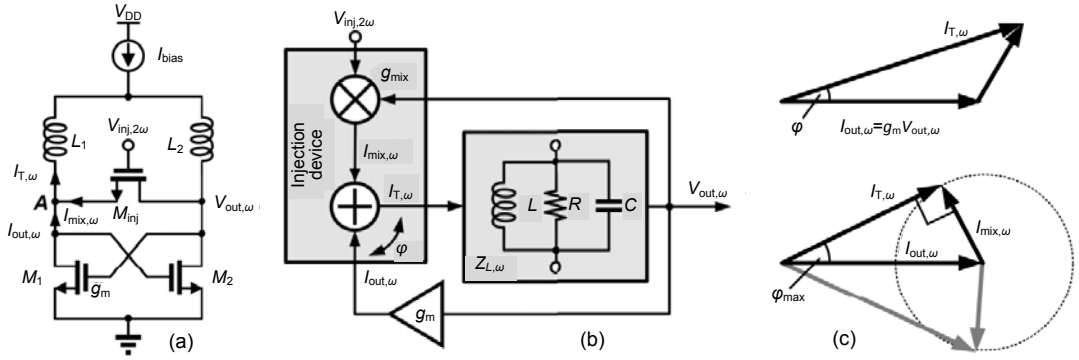

Fig. 21 Conventional ILFD (a), simplified model of ILFD with the *LC*-tank (b), and phasor diagram of the currents (c)
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Based on Eqs. (17)–(20), the maximum phase shift of the resonator under the locking state is derived by

$$\angle Z_{L,\omega(\max)} = \pm \arcsin\left(\frac{\left|g_{\mathrm{mix}} V_{\mathrm{inj},2\omega}\right|}{\left|g_{\mathrm{m}} V_{\mathrm{out},\omega}\right|}\right). \tag{21}$$

When the phase of $Z_{L,\omega}$ is larger than $\angle Z_{L,\omega(\max)}$, ILFD will lose locking (Fig. 22a). From Eq. (21), it can also be inferred that the locking range can be enhanced by the following methods:

1. Enlarge the transconductance of the injection device (Fig. 22b).

2. Decrease the transconductance of the cross-coupled pair or output voltage.

3. Flatten the phase response of the resonator around zero degree (Fig. 22c).

The first method, which has been discussed in Chao and Luong (2013), is not easy to realize in mm-Wave frequencies because of the parasitic capacitances of transistors. The second one encounters a risk of failure of oscillation and low output power. The third one seems a reasonable solution for wideband mm-Wave ILFD design.

4.1.2 Transformer-based high-order resonator

As shown in Fig. 23, the resonator is composed of a transformer and two capacitors. A SPECTRE simulation is performed to compare the transformer-based fourth-order and the *LC*-tank-based resonators. As shown in Fig. 24a, compared to the *LC*-tank one, the impedance's phase of the transformer-based resonator achieves a much larger frequency range within $\angle Z_{L,\omega(\max)}$. This is because a phase ripple is created. From Fig. 24b, it is obvious that a ripple in amplitude response will also appear with the transformer. Its bandwidth will be enlarged when the coupling coefficient of the transformer (k) is increased. This means a larger k can achieve a larger locking range. The ripple may move beyond $\angle Z_{L,\omega(\max)}$ with a large k (Fig. 24a). This may lead to an in-band loss of locking. Therefore, k should be set at an appropriate value.

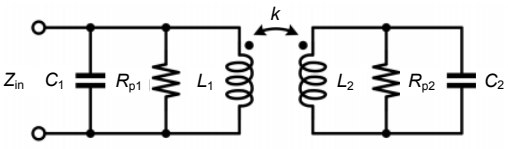

Fig. 23 Schematic of the transformer-based fourth-order resonator

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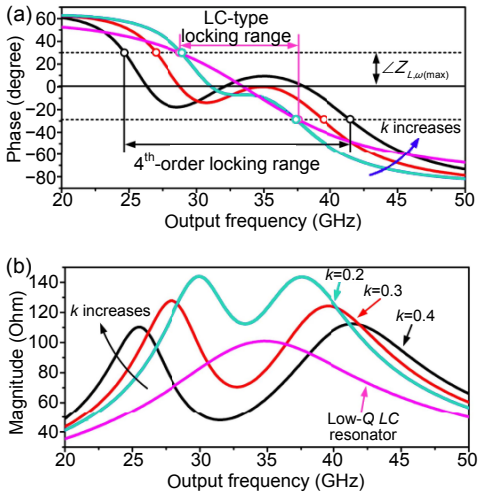

Fig. 24 Simulation results of the impedance of the resonator vs. k: (a) phase response; (b) magnitude response

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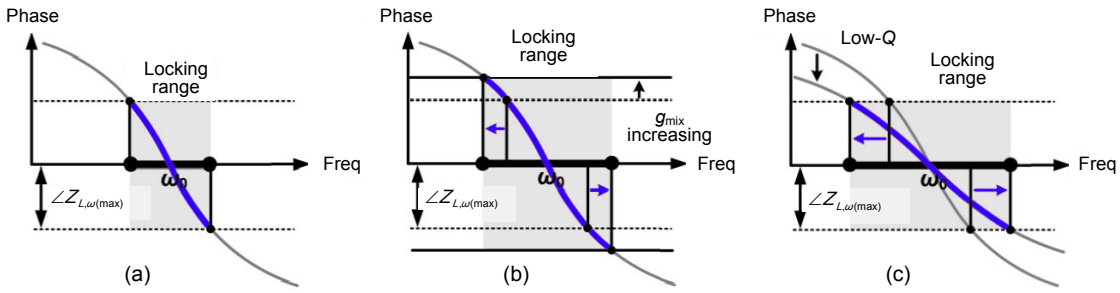

Fig. 22 Locking range of the conventional ILFD (a), increasing the locking range by enlarging g_{mix} (b), and increasing the locking range using a low-*Q* *LC*-tank (c)

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4.2 Implementation of ultra-wideband ILFD

Fig. 25 shows the schematic of ILFD. Two gain-peaking inductors L_p are inserted between the cross-coupled pair and the high-order resonator to increase the impedance of the differential load. It will strengthen the condition of oscillation and reduce the DC power consumption. The simulated impedances with and without the peaking inductor are presented in Fig. 26. It can be seen that the impedance amplitude increases with L_p at low frequencies, while the phase response variation is enlarged. However, the phase response variation can be rebuilt easily by adjusting the capacitors in the resonator. The wideband output buffers are also adopted to improve the output power and increase the isolation between the core and external load, which are connected to the secondary coil of the transformer. As shown in Fig. 27, the primary winding of the transformer is implemented by a two-turn octagonal inductor to reduce the chip size.

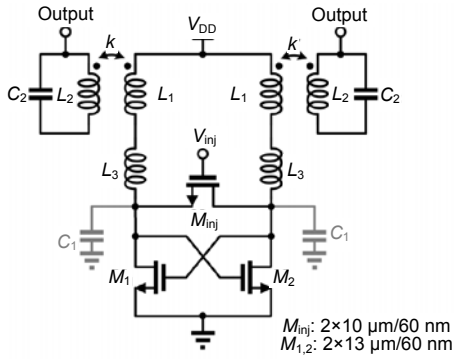

Fig. 25 Schematic of ILFD

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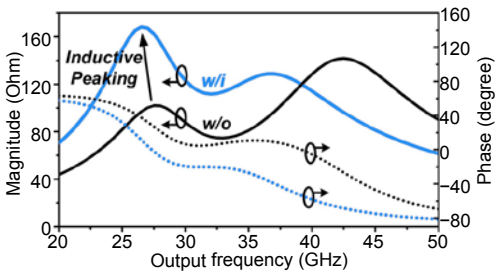

Fig. 26 Simulated impedances of the load with and without the gain peaking inductor

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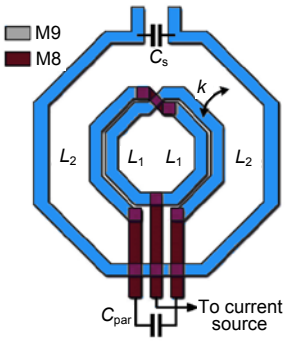

Fig. 27 Layout view of the transformer

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4.3 Measurement results of ultra-wideband ILFD

The circuit is fabricated using a 65-nm CMOS technology, whose die photo is shown in Fig. 28. The core area is only 280 μm×250 μm. Its required supply voltage is only 0.42 V, and the DC power consumption is about 1.2 mW.

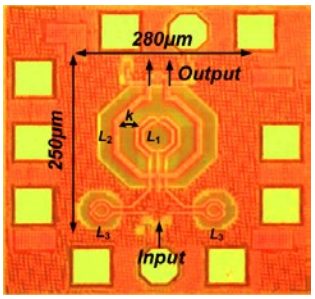

Fig. 28 Chip micrograph of ILFD

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Fig. 29a presents the tested input sensitivity curve of ILFD with the supply voltage of 0.42, 0.45, and 0.48 V. It can be seen that the locking range of the circuit is about 29.6 GHz (from 32.3 to 61.9 GHz), and the fractional bandwidth is 62.7% of the center frequency. As shown in Fig. 29b, the phase noise performance is tested across the entire operating frequency band. The phase difference between the input signal and output signal is around 6 dB, which agrees well with the theoretical value. The performance of ILFD is summarized and compared with those of the published mm-Wave ILFDs in Table 3. It can be found that the transformer-based ILFD achieves a much larger locking range.

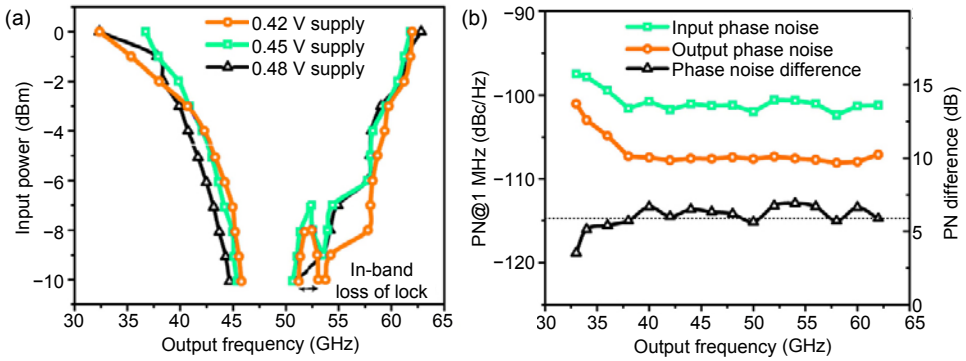

Fig. 29 Measured input sensitivity (a) and tested phase noise performance (b) of ILFD
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Table 3 Performance summary and comparison of ILFD

Reference	Process	Supply voltage (V)	Operation frequency (GHz)	Locking range (GHz)*	PN diff. (dBc/Hz)		Power (mW)	Core area (mm^2)
					100 kHz	1 MHz		
Ghilioni et al., 2013	32 nm CMOS	1	14.0–70.0	32.0 (60.0%)	12	12	48	0.001
Lin and Wang, 2016	65 nm CMOS	0.4	36.8–59.2	22.4 (46.7%)	6	NA	1.6	0.046
Chen et al., 2013	65 nm CMOS	1	25.0–53.6	28.6 (72.8%)	6	10	12.1	0.105
Luo and Chen, 2008	90 nm CMOS	0.8	38.8–51.2	12.4 (27.6%)	NA	NA	0.8	0.192
Chao and Luong, 2013	65 nm CMOS	0.8	53.4–79.4	26.0 (39.2%)	6	6	2.9	0.126
Takatsu et al., 2010	65 nm CMOS	1.2	48.5–62.9	14.4 (25.9%)	NA	NA	1.65	0.125
Imani and Hashemi, 2017	130 nm SiGe	1.15	35.0–59.5	18.5 (36.8%)	6	0	3.8	0.046
Zhang et al., 2018	**65 nm CMOS**	**0.42**	**32.3–61.9**	**29.6 (62.7%)**	**6**	**6**	**1.2**	**0.070**

* The percentage in the brackets refers to the fractional locking range. PN diff.: phase noise difference. NA: not available

5 Ultra-wideband high linearity mm-Wave up-conversion mixer

Mixers are also necessary blocks in transceivers for wireless applications. With the phased-array technique being widely considered as the most likely solution for mm-Wave applications, the wideband mm-Wave mixers need a high linearity to ensure a large dynamic range. Several improvement techniques, such as the complementary derivative superposition technique (Byeon et al., 2015), adaptive biasing schemes (Won et al., 2015), and the resistive feedback network (Lee et al., 2017), are reported to achieve high linearity for mm-Wave up-conversion mixers. Nevertheless, these techniques find it hard to achieve high linearity and wide intermediate frequency (IF) and RF bandwidth simultaneously.

Chen ZN et al. (2019) proposed an advanced mm-Wave up-conversion mixer topology with a transformer-based high-order network and two-path transconductance stage to achieve both wide bandwidth and high linearity. The high-order load realized by a transformer is used as an output impedance matching network to improve the RF bandwidth, and occupies a more compact layout than the inductor-based high-order structures. The two-path transconductance stage is helpful in suppressing the high-order distortion of transistors and reducing the impedance variation with frequency. Thus, this stage is adopted to enhance the linearity of the mixer and the IF matching bandwidth.

5.1 Analysis of the two-path transconductance stage

5.1.1 Linearity

For an active up-conversion mixer, the linearity and IF bandwidth are dominated mainly by the transconductance stage. A two-path transconductance stage involving a CS path and a cross-coupled common-gate (CCCG) path is used to improve both linearity and IF bandwidth. As shown in Fig. 30, the CS path consists of transistors M_1 and M_2 with source-degeneration inductors L_1 and L_2, while the CCCG path is made up of transistors M_3 and M_4 with source-degeneration inductors L_3 and L_4. The drain currents of M_1 and M_4 can be obtained as follows:

$$i_1 = g_{m1}^1 V_{if} + g_{m1}^2 V_{if}^2 + g_{m1}^3 V_{if}^3 + \cdots, \quad (22)$$

$$i_4 = g_{m4}^1 \beta V_{if} + g_{m4}^2 \beta^2 V_{if}^2 + g_{m4}^3 \beta^3 V_{if}^3 + \cdots, \quad (23)$$

where g_{m1}^n and g_{m4}^n denote the n^{th}-order transconductances of M_1 and M_4, respectively, V_{if} is the input voltage at node x (Fig. 30), and β means the boosting factor of g_m, which is affected mainly by the gate-source and coupling capacitors (Li et al., 2005). Since $C_{c1} >> C_{gs4}$ (C_{gs4} represents the gate-source parasitic capacitance of M_4), $\beta \approx 2$. At the drain node of M_1 (node O), the total current is derived from

$$\begin{aligned} i_0 &= i_1 + i_4 \\ &= (g_{m1}^1 + g_{m4}^1 \beta) V_{if} + (g_{m1}^2 + g_{m4}^2 \beta^2) V_{if}^2 \\ &\quad + (g_{m1}^3 + g_{m4}^3 \beta^3) V_{if}^3. \end{aligned} \quad (24)$$

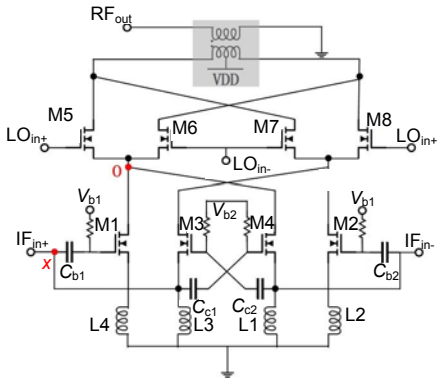

Fig. 30 Schematic of the proposed up-conversion mixer
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The third-order distortion has serious influence on the linearity of devices, and is strongly relevant to the gate bias voltage (Razavi, 2011). Therefore, M_1 is biased in the weak inversion region, while M_4 is working in the saturation region. This leads to the third-order transconductance coefficients of M_1 and M_4 (g_{m1}^3 and g_{m4}^3) having opposite polarity (Liu et al., 2018). By optimizing the bias voltage and size of M_1 and M_4, the summed third-order coefficient ($g_{m1}^3 + g_{m4}^3 \beta^3$) can be largely eliminated. The linearity will be improved accordingly. Meanwhile, the gain is increased at the two-path transconductance stage, because the first-order transconductance coefficients (g_{m1}^1 and g_{m4}^1) of the transistors of the two paths have the same polarity. Fig. 31 plots the improvement of IP_{1dB} and gain, compared with the state of turning off the CS path. It can be observed that the IP_{1dB} is increased and the gain is degraded when the gate bias voltage V_{GS} decreases from the strong inversion region to the weak inversion region. Fig. 31 is used to guide the design of the up-conversion mixer. To alleviate the process-voltage-temperature (PVT) influence, a diode is connected to the current mirror as the bias circuits to compensate for the PVT variations (Fig. 32a). The post-layout simulation results (Fig. 32b) show that IP_{1dB} changes slightly with the temperature changing from −45 °C to 125 °C, and IP_{1dB} varies by 0.9 dB with the process changing.

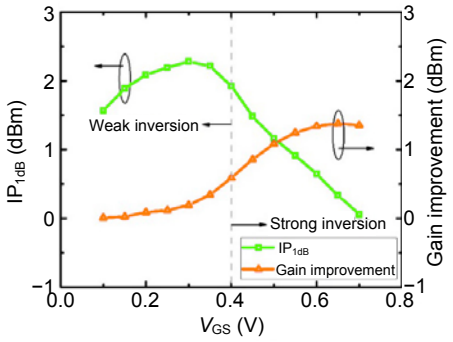

Fig. 31 Simulated IP_{1dB} and gain improvement versus V_{GS} of the CS path
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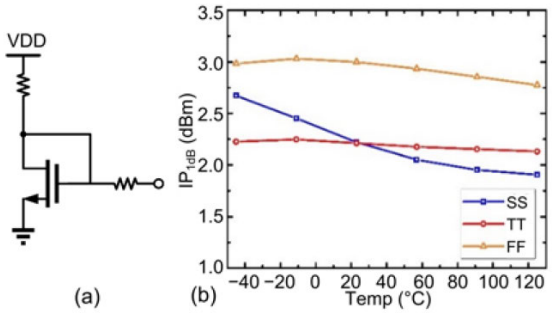

Fig. 32 Bias circuits (a) and simulated IP_{1dB} vs. temperature and the process deviation (b)

5.1.2 Bandwidth

In a conventional CS stage, the input impedance Z_{in} has a huge imaginary-part variation with the frequency. When the transistor size is set at 12 μm/60 nm, the simulated imaginary part of Z_{in} of the conventional CS path (Fig. 33) ranges from −580 to −200 Ω

in the band of 10–30 GHz. It is difficult to design an input matching network with such a wide frequency range. Owing to the two-path transconductance stage, the imaginary part of Z_{in} attains a small variation of 11–17 Ω over 10–30 GHz (Fig. 33). This means that in the two-path transconductance stage it is much easier to achieve a wideband IF operation than the conventional structure.

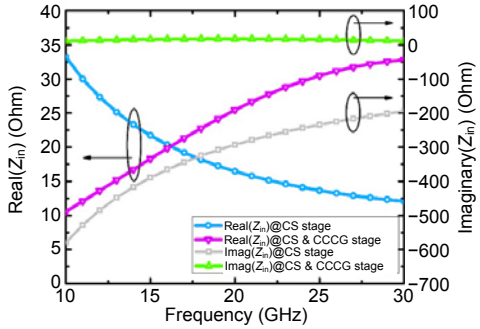

Fig. 33 Simulated Z_{in} of the proposed CS & CCCG stage and the conventional CS stage

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5.2 Implementation of the ultra-wideband mm-Wave up-conversion mixer

Fig. 34 shows the schematic of the up-conversion mixer, which is composed of a two-path transconductance stage, a double-balanced switching stage, and a transformer-based load stage. NMOS transistors M_5–M_8 function as the switching stage. To obtain a wideband output matching, a transformer is applied to realize the load stage, whose physical view is shown in Fig. 34a. Compared with the conventional inductive load, this transformer-based load does not require additional devices achieve output impedance matching. Thus, the chip size can be reduced. According to the full-wave electromagnetic (EM) simulation, the transformer with a symmetrical layout provides low insertion loss and excellent balance performance (Fig. 34b).

5.3 Measurement results of the ultra-wideband up-conversion mixer

The up-conversion mixer is demonstrated in a commercial 65 nm CMOS process. It consumes a DC power of 10.8 mW. Fig. 35 shows the photo of the chip, whose size is 0.75 mm×0.51 mm.

The measured return losses of IF, LO, and RF ports are shown in Fig. 36a. Thanks to the output transformer and two-path transconductance stage, both IF and RF ports achieve ultra-wideband impedance matching. The measured conversion gains with different LOs (48, 55, and 62 GHz) are shown in Fig. 36b. A 3-dB IF bandwidth of 18 GHz is captured by measurement, from 12 to 30 GHz. From Fig. 36b, it can also be observed that the maximum conversion gain is −4.3 dB at 77 GHz. The measured 3-dB RF bandwidth is 23 GHz (from 62 to 85 GHz). The IP_{1dB} is 2.14 dBm at 77 GHz (Fig. 37). The LO-to-IF and LO-to-RF isolations are better than 30 dB. The chip performances are summarized and compared in Table 4. The mixer with the two-path transconductance stage and transformer-based load stage demonstrates the best IP_{1dB} and widest RF and IF bandwidth.

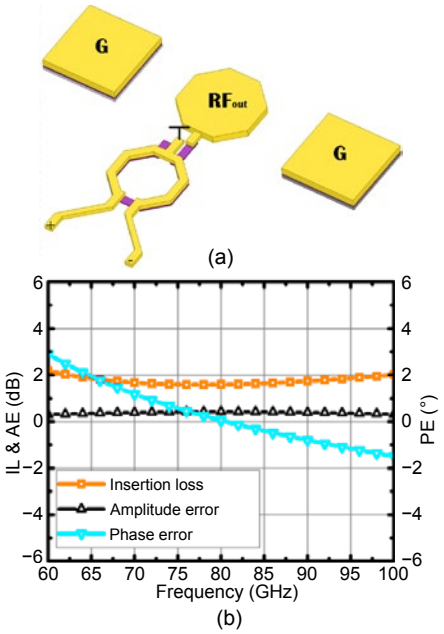

Fig. 34 Layout of the output transformer (a) and electromagnetic simulation results of the output transformer (b)

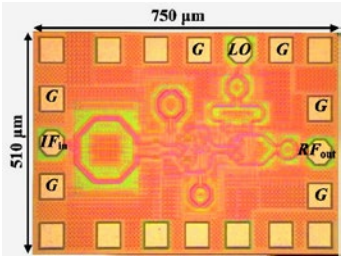

Fig. 35 Chip micrograph of the mixer

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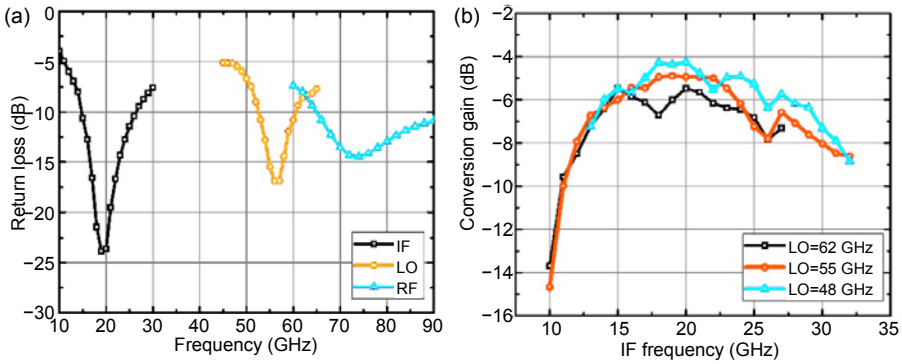

Fig. 36 Measured performance of the up-conversion mixer: (a) return losses of IF, LO, and RF ports; (b) conversion gain versus IF frequencies

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Table 4 Summary and comparison with state-of-the-art mixers

Parameter	Value or description			
	Lee et al., 2017	Lin et al., 2014	Levinger et al., 2014	Chen et al., 2019
Process	65 nm CMOS	90 nm CMOS	0.13 μm SiGe	**65 nm CMOS**
RF frequency (GHz)	60	71–81	71–86	**62–85**
IF bandwidth (GHz)	7.5	–	–	**18**
Conversion gain (dB)	6.2@57 GHz	2.1@78.1 GHz	3.9@76 GHz	**−4.3@77 GHz**
IP_{1dB} (dBm)	−12.5@57 GHz	−10@78.1 GHz	−1.9@76 GHz	**2.14@77 GHz**
Isolation (dB)	35	35.9	30	**30**
Chip area (mm^2)	0.66×0.63	0.72×0.83	1.5×1.2	**0.75×0.51**
DC power (mW)	17.8	13.6	80	**10.8**

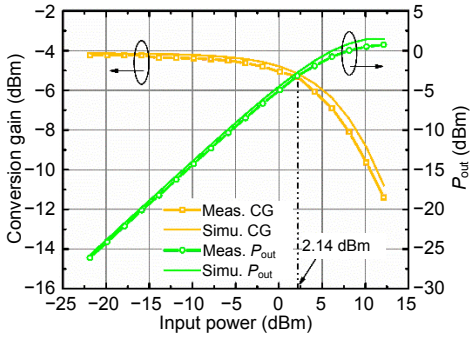

Fig. 37 Measured and simulated conversion gain and output power

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6 Conclusions and discussion

With the rapid development of mm-Wave wireless applications, a new requirement of wide bandwidth for circuits and systems has emerged to serve multi-band operations and multiple applications. In this paper, several transformer-based techniques are reported to realize a wide operating bandwidth for the widely used mm-Wave circuits in commercial CMOS processes. For the mm-Wave amplifier design, the transformer-based Gm-boosting technique is beneficial to noise and gain performance, and the pole-tuning method can effectively extend the gain bandwidth. The injection-locked architecture has revealed excellent advantages in mm-Wave multiplier and divider design. The introduced injection-current-boosting technique can greatly increase the injection current for the injection-locked oscillators, and further enlarge the locking range of the circuits. The transformer-based high-order resonator is also a workable way to significantly enhance the operating bandwidth of ILFDs and ILFMs. The two-path transconductance stage is discussed as implementing the up-conversion mixer with high linearity. The presented structure possesses a low variation of input impedance. Thus, it is easy to achieve a wide IF bandwidth for the mm-Wave mixer. A transformer-based load at the RF port is also introduced to increase the bandwidth of the output impedance matching of mixers.

In recent years, phased-array transceivers have become the most attractive candidate for mm-Wave

wireless applications. Besides the wide bandwidth, they put forward new requirements for their key building blocks, including small chip size, low power consumption, scalability, and high PVT robustness.

Contributors

Yi-ming YU wrote the first draft of the manuscript. Kai KANG helped organize the manuscript. Yi-ming YU and Kai KANG revised and edited the final version.

Compliance with ethics guidelines

Yi-ming YU and Kai KANG declare that they have no conflict of interest.

References

Byeon CW, Lee JH, Lee DY, et al., 2015. A high linearity, image/LO-rejection I/Q up-conversion mixer for 5G cellular communications. European Microwave Conf, p.345-348. https://doi.org/10.1109/EuMC.2015.7345983

Chan WL, Long JR, 2008. A 56-65 GHz injection-locked frequency tripler with quadrature outputs in 90-nm CMOS. *IEEE J Sol-State Circ*, 43(12):2739-2746. https://doi.org/10.1109/JSSC.2008.2004869

Chao Y, Luong HC, 2013. Analysis and design of a 2.9-mW 53.4-79.4-GHz frequency-tracking injection-locked frequency divider in 65-nm CMOS. *IEEE J Sol-State Circ*, 48(10):2403-2418. https://doi.org/10.1109/JSSC.2013.2272371

Chen WL, Shiao YSJ, Yen HD, et al., 2013. A 53.6 GHz direct injection-locked frequency divider with a 72% locking range in 65 nm CMOS technology. IEEE MTT-S Int Microwave Symp Digest, p.1-3. https://doi.org/10.1109/MWSYM.2013.6697536

Chen ZL, Liu HH, Liu ZQ, et al., 2019. A 62-85-GHz high linearity upconversion mixer with 18-GHz IF bandwidth. *IEEE Microw Wirel Compon Lett*, 29(3):219-221. https://doi.org/10.1109/LMWC.2019.2894979

Chen ZM, Wang CC, Yao HC, et al., 2012. A BiCMOS W-band 2×2 focal-plane array with on-chip antenna. *IEEE J Sol-State Circ*, 47(10):2355-2371. https://doi.org/10.1109/JSSC.2012.2209775

Deng W, Siriburanon T, Musa A, et al., 2013. A sub-harmonic injection-locked quadrature frequency synthesizer with frequency calibration scheme for millimeter-wave TDD transceivers. *IEEE J Sol-State Circ*, 48(7):1710-1720. https://doi.org/10.1109/JSSC.2013.2253396

Feng GY, Boon CC, Meng FY, et al., 2017. Pole-converging intrastage bandwidth extension technique for wideband amplifiers. *IEEE J Sol-State Circ*, 52(3):769-780. https://doi.org/10.1109/JSSC.2016.2641459

Fritsche D, Tretter G, Carta C, et al., 2015. Millimeter-wave low-noise amplifier design in 28-nm low-power digital CMOS. *IEEE Trans Microw Theory Techn*, 63(6):1910-1922. https://doi.org/10.1109/TMTT.2015.2427794

Gao ZZ, Kang K, Zhao CX, et al., 2015. A broadband and equivalent-circuit model for millimeter-wave on-chip *M*:*N* six-port transformers and baluns. *IEEE Trans Microw Theory Techn*, 63(10):3109-3121. https://doi.org/10.1109/TMTT.2015.2466549

Ghilioni A, Mazzanti A, Svelto F, 2013. Analysis and design of mm-Wave frequency dividers based on dynamic latches with load modulation. *IEEE J Sol-State Circ*, 48(8):1842-1850. https://doi.org/10.1109/JSSC.2013.2258793

Guo ST, Xi TZ, Gui P, et al., 2016. A transformer feedback G_m-boosting technique for gain improvement and noise reduction in mm-Wave cascode LNAs. *IEEE Trans Microw Theory Techn*, 64(7):2080-2090. https://doi.org/10.1109/TMTT.2016.2564398

Hussein AI, Paramesh J, 2017. Design and self-calibration techniques for inductor-less millimeter-wave frequency dividers. *IEEE J Sol-State Circ*, 52(6):1521-1541. https://doi.org/10.1109/JSSC.2017.2681801

Imani A, Hashemi H, 2017. Distributed injection-locked frequency dividers. *IEEE J Sol-State Circ*, 52(8):2083-2093. https://doi.org/10.1109/JSSC.2017.2701325

Jang SL, Chang CW, Wun JY, et al., 2011. Quadrature injection-locked frequency dividers using dual-resonance resonator. *IEEE Microw Wirel Compon Lett*, 21(1):37-39. https://doi.org/10.1109/LMWC.2010.2091264

Khanzadi MR, Kuylenstierna D, Panahi A, et al., 2014. Calculation of the performance of communication systems from measured oscillator phase noise. *IEEE Trans Circ Syst I*, 61(5):1553-1565. https://doi.org/10.1109/TCSI.2013.2285698

Kim HT, Park BS, Song SS, et al., 2018. A 28-GHz CMOS direct conversion transceiver with packaged 2×4 antenna array for 5G cellular system. *IEEE J Sol-State Circ*, 53(5):1245-1259. https://doi.org/10.1109/JSSC.2018.2817606

Lee JG, Lee HJ, Kim SH, et al., 2017. 60GHz direct up-conversion mixer with wide IF bandwidth and high linearity in 65nm CMOS. IEEE Int Symp on Radio-Frequency Integration Technology, p.74-76. https://doi.org/10.1109/RFIT.2017.8048294

Levinger R, Sheinman B, Katz O, et al., 2014. A 71-86GHz multi-tanh up-conversion mixer achieving +1dBm OP1dB in 0.13 μm SiGe technology. IEEE MTT-S Int Microwave Symp, p.1-4. https://doi.org/10.1109/MWSYM.2014.6848282

Li A, Zheng SY, Yin J, et al., 2014. A 21-48 GHz subharmonic injection-locked fractional-*N* frequency synthesizer for multiband point-to-point backhaul communications. *IEEE J Sol-State Circ*, 49(8):1785-1799. https://doi.org/10.1109/JSSC.2014.2320952

Li XY, Shekhar S, Allstot DJ, 2005. G_m-boosted common-gate LNA and differential colpitts VCO/QVCO in 0.18-μm CMOS. *IEEE J Sol-State Circ*, 40(12):2609-2619. https://doi.org/10.1109/JSSC.2005.857426

Lin BL, Liu SI, 2011. Analysis and design of D-band injection-locked frequency dividers. *IEEE J Sol-State Circ*, 45(6):1250-1264. https://doi.org/10.1109/JSSC.2011.2131750

Lin YH, Wang H, 2016. A 35.7-64.2 GHz low power Miller divider with weak inversion mixer in 65 nm CMOS. *IEEE*

Microw Wirel Compon Lett, 26(11):948-950. https://doi.org/10.1109/LMWC.2016.2615013

Lin YS, Wen WC, Wang CC, 2014. 13.6 mW 79 GHz CMOS up-conversion mixer with 2.1 dB gain and 35.9 dB LO-RF isolation. *IEEE Microw Wirel Compon Lett*, 24(2): 126-128. https://doi.org/10.1109/LMWC.2013.2291204

Liu G, Schumacher H, 2013. Broadband millimeter-wave LNAs (47-77 GHz and 70-140 GHz) using a T-type matching topology. *IEEE J Sol-State Circ*, 48(9):2022-2029. https://doi.org/10.1109/JSSC.2013.2265500

Liu ZQ, Dong JY, Chen ZL, et al., 2018. A 62-90 GHz high linearity and low noise CMOS mixer using transformer-coupling cascode topology. *IEEE Access*, 6:19338-19344. https://doi.org/10.1109/ACCESS.2018.2814062

Luo TN, Chen YJE, 2008. A 0.8-mW 55-GHz dual-injection-locked CMOS frequency divider. *IEEE Trans Microw Theory Techn*, 56(3):620-625. https://doi.org/10.1109/TMTT.2008.916868

Mangraviti G, Khalaf K, Parvais B, et al., 2015. Design and tuning of coupled-LC mm-wave subharmonically injection-locked oscillators. *IEEE Trans Microw Theory Techn*, 63(7):2301-2312. https://doi.org/10.1109/TMTT.2015.2439259

Razavi B, 2004. A study of injection locking and pulling in oscillators. *IEEE J Sol-State Circ*, 39(9):1415-1424. https://doi.org/10.1109/JSSC.2004.831608

Razavi B, 2011. RF Microelectronics (2nd Ed.). Prentice-Hall, Englewood Cliffs, NJ, USA.

Reynaert P, Steyaert W, Standaert A, et al., 2017. mm-Wave and THz circuit design in standard CMOS technologies: challenges and opportunities. IEEE Asia Pacific Microwave Conf, p.85-88. https://doi.org/10.1109/APMC.2017.8251383

Rong S, Luong HC, 2010. A 0.8 V 57 GHz-to-72 GHz differential input frequency divider with locking range optimization in 0.13-μm CMOS. Proc IEEE Asian Solid-State Circuits Conf, p.1-4.

Sadhu B, Ferriss M, Valdes-Garcia A, 2015. A 52 GHz frequency synthesizer featuring a 2nd harmonic extraction technique that preserves VCO performance. *IEEE J Sol-State Circ*, 50(5):1214-1223. https://doi.org/10.1109/JSSC.2015.2414921

Shahramian S, Baeyens Y, Kaneda N, et al., 2013. A 70–100 GHz direct-conversion transmitter and receiver phased array chipset demonstrating 10 Gb/s wireless link. *IEEE J Sol-State Circ*, 48(5):1113-1125. https://doi.org/10.1109/JSSC.2013.2254536

Shin D, Koh KJ, 2018. An injection frequency-locked loop—autonomous injection frequency tracking loop with phase noise self-calibration for power-efficient mm-wave signal sources. *IEEE J Sol-State Circ*, 53(3):825-838. https://doi.org/10.1109/JSSC.2017.2782762

Takatsu K, Tamura H, Yamamoto T, et al., 2010. A 60-GHz 1.65mW 25.9% locking range multi-order LC oscillator based injection locked frequency divider in 65 nm CMOS. Proc IEEE Custom Integrated Circuits Conf, p.1-4. https://doi.org/10.1109/CICC.2010.5617390

Vigilante M, Reynaert P, 2016a. Analysis and design of an E-band transformer-coupled low-noise quadrature VCO in 28-nm CMOS. *IEEE Trans Microw Theory Techn*, 64(4):1122-1132. https://doi.org/10.1109/TMTT.2016.2530703

Vigilante M, Reynaert P, 2016b. 20.10 A 68.1-to-96.4 GHz variable-gain low-noise amplifier in 28nm CMOS. IEEE Int Solid-State Circuits Conf, p.360-361. https://doi.org/10.1109/ISSCC.2016.7418056

Vigilante M, Reynaert P, 2018. A wideband class-AB power amplifier with 29-57-GHz AM–PM compensation in 0.9-V 28-nm bulk CMOS. *IEEE J Sol-State Circ*, 53(5): 1288-1301. https://doi.org/10.1109/JSSC.2017.2778275

Won YS, Kim CH, Lee SC, 2015. A 24 GHz highly linear up-conversion mixer in CMOS 0.13 μm technology. *IEEE Microw Wirel Compon Lett*, 25(6):400-402. https://doi.org/10.1109/LMWC.2015.2421293

Wu QY, Quach T, Mattamana A, et al., 2013. A 10mW 37.8GHz current-redistribution BiCMOS VCO with an average FOMT of −193.5dBc/Hz. IEEE Int Solid-State Circuits Conf Digest of Technical Papers, p.150-151. https://doi.org/10.1109/ISSCC.2013.6487677

Yanay N, Socher E, 2015. Wide tuning-range mm-wave voltage-controlled oscillator employing an artificial magnetic transmission line. *IEEE Trans Microw Theory Techn*, 63(4):1342-1352. https://doi.org/10.1109/TMTT.2015.2403366

Yao T, Gordon MQ, Tang KKW, et al., 2007. Algorithmic design of CMOS LNAs and PAs for 60-GHz radio. *IEEE J Sol-State Circ*, 42(5):1044-1057. https://doi.org/10.1109/JSSC.2007.894325

Yeh HC, Chiong CC, Aloui S, et al., 2012. Analysis and design of millimeter-wave low-voltage CMOS cascode LNA with magnetic coupled technique. *IEEE Trans Microw Theory Techn*, 60(12):4066-4079. https://doi.org/10.1109/TMTT.2012.2224365

Yoo S, Choi S, Kim J, et al., 2018. A low-integrated-phase-noise 27-30-GHz injection-locked frequency multiplier with an ultra-low-power frequency-tracking loop for mm-wave-band 5G transceivers. *IEEE J Sol-State Circ*, 53(2): 375-388. https://doi.org/10.1109/JSSC.2017.2749420

Yu YM, Liu HH, Wu YQ, et al., 2017. A 54.4-90 GHz low-noise amplifier in 65-nm CMOS. *IEEE J Sol-State Circ*, 52(11):2892-2904. https://doi.org/10.1109/JSSC.2017.2727040

Zhang JZ, Cheng YX, Zhao CX, et al., 2018. Analysis and design of ultra-wideband mm-wave injection-locked frequency dividers using transformer-based high-order resonators. *IEEE J Sol-State Circ*, 53(8):2177-2189. https://doi.org/10.1109/JSSC.2018.2822710

Zhang JZ, Liu HH, Wu YQ, et al., 2019. An injection-current-boosting locking-range enhancement technique for ultra-wideband mm-wave injection-locked frequency triplers. *IEEE Trans Microw Theory Techn*, 67(7):3174-3186. https://doi.org/10.1109/TMTT.2019.2907254

Zong ZR, Babaie M, Staszewski RB, 2016. A 60 GHz frequency generator based on a 20 GHz oscillator and an implicit multiplier. *IEEE J Sol-State Circ*, 51(5):1261-1273. https://doi.org/10.1109/JSSC.2016.2528997