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A driving pulse edge modulation technique and its complex programming logic devices implementation*

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Abstract: With the continual increase in switching speed and rating of power semiconductors, the switching voltage spike becomes a serious problem. This paper describes a new technique of driving pulse edge modulation for insulated gate bipolar transistors (IGBTs). By modulating the density and width of the pulse trains, without regulating the hardware circuit, the slope of the gate driving voltage is controlled to change the switching speed. This technique is used in the driving circuit based on complex programmable logic devices (CPLDs), and the switching voltage spike of IGBTs can be restrained through software, which is easier and more flexible to adjust. Experimental results demonstrate the effectiveness and practicability of the proposed method.

Key words: Driving pulse edge modulation, Switching voltage spike, Complex programmable logic device (CPLD), Active gate drive

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1 Introduction

The performance of an insulated gate bipolar transistor (IGBT) gate driver is correlated with the switching behavior of power electronic devices. Both drive capability, including steady and transient states, and protection should be considered carefully. Especially in high power applications, higher $\mathrm{d}i_c/\mathrm{d}t$, in which i_c is the collector current of the IGBT, and larger parasitic inductance may cause more serious switching voltage spikes (Eckel and Sack, 1993; Idir *et al.*, 2006; Kim *et al.*, 2007).

There are two main types of gate drivers in applications: traditional and active (Dulau *et al.*, 2006; Idir *et al.*, 2006; Bryant *et al.*, 2007; Grbovic, 2007; Kim *et al.*, 2007; Kuhn *et al.*, 2008; Schmitt *et al.*, 2008; Bortis *et al.*, 2009; Chen and Peng, 2009a; 2009b; Wang *et al.*, 2013a; 2013b; 2014). Both types can regulate the switching speed.

Changing gate resistance and gate capacitance, based on the traditional drive, leads to different charging and discharging times. However, the switching peak voltage cannot be suppressed significantly through this method. Therefore, to control the gate charging and discharging time, several active gate drivers are proposed. A two-level turn-on and turn-off voltage method limits the peak current and over voltage at the cost of a more complicated circuit and a higher switching loss (Dulau *et al.*, 2006). Multi-level gate resistance methods have also been studied (Blaabjerg and Pedersen, 1992; Eckel and Sack, 1993), but they are affected by detection delay and are not suitable for normal operation. The accuracy of both multi-level voltage and multi-level resistance methods is affected by the level of resistance or voltage. Palmer and Rajamani (2004) proposed a

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method to control IGBT gate voltage using a voltage feedback loop to restrain the voltage spike. However, the method is sensitive to device parameters and may cause instability. The closed-loop gate drive proposed by Chen and Peng (2009a; 2009b) can control voltage and current overshoot. However, the method is realized by complicated hardware and gate voltage oscillation may introduce secondary failure. The dynamic voltage rise control technique (Hornkamp, 2006), which uses a capacitor to monitor and control turn-off speed, is useful in preventing voltage overshoot. However, the relevant parameters need to be designed very carefully and precisely. There are other similar alternative techniques (Bryant *et al*., 2007), but all these methods are based on hardware modification, for which careful parameter design is very important.

With the development of digital drive techniques (Hemmer *et al*., 2010), some new strategies have been employed. A new feed-forward control of the IGBT turn-off dynamics based on the gate voltage shaping method using a 100-MHz field programmable gate array (FPGA) device was introduced by Michel *et al.* (2013). This method overcomes some of the previous limitations, but it uses two FPGAs and the testing was carried out at a very low voltage level.

In this paper, a new technique of driving pulse edge modulation based on a digital circuit is developed. A complex programmable logic device (CPLD) is used for advanced drive and protection. The slope of the driving voltage can be controlled without changing the hardware circuit. Therefore, the turn-on and turn-off speed of the semiconductor devices can be regulated by programming, which is more flexible and easier to control. Results obtained on an H-bridge inverter are presented at the end of this paper to demonstrate the validity of this new IGBT driver, based on the driving pulse edge modulation technique.

2 Influence of IGBT switching behavior on the voltage spike

In high power applications, there is usually a freewheeling diode paralleled with an IGBT. Fig. 1 shows a double pulse test circuit which is usually used for testing parasitic inductance and IGBT performance. The upper IGBT Q_1 remains off, and the IGBT Q_2 is given the turn-on pulse signal twice. When Q_2 is on, the DC-link capacitor charges the inductance L and the inductance current i_L increases linearly. When Q_2 is off, the current freewheels through the freewheeling diode paralleled with Q_1. Neglecting the line loss, the current i_L remains unchanged.

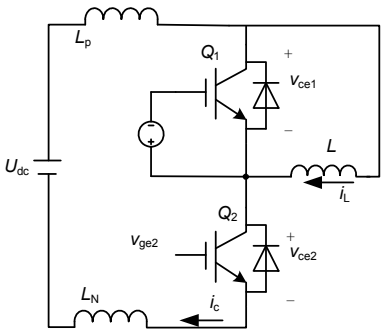

Fig. 1 Double pulse test circuit

The upper part of Fig. 2 shows the voltage and current waveforms of the double pulse test. When amplifying the part in the dashed box to analyze the voltage spike, the waveforms can be simplified as shown in the lower part of Fig. 2. Since t is very short, the current i_c can be considered constant during the period. Once the drive signal v_{ge2} is low, Q_2 turns off immediately, and the output current flows through the freewheeling diode of Q_1. The current i_c decreases sharply. Considering the existence of parasitic inductance L_P and L_N, the collector-emitter peak voltage of Q_2 can be expressed as

$$\begin{aligned} v_{ce2,peak} &= U_{dc} - L_P \frac{di_c}{dt} + V_{F1} - L_N \frac{di_c}{dt} \\ &\approx U_{dc} - (L_P + L_N)\frac{di_c}{dt}, \end{aligned} \tag{1}$$

where V_{F1} is the forward voltage of the freewheeling diode of Q_1.

When Q_2 turns on, the output current path will be changed from the freewheeling diode of Q_1 to IGBT Q_2. The spike of current i_c is produced because of the reverse recovery characteristic of the diode. The collector-emitter peak voltage of Q_1 can be expressed as

$$v_{ce1,peak} = U_{dc} - L_P \frac{di_c}{dt} - V_{ce,sat2} - L_N \frac{di_c}{dt} \approx U_{dc} - (L_P + L_N)\frac{di_c}{dt}, \quad (2)$$

where $V_{ce,sat2}$ refers to the collector-emitter saturation voltage of Q_2.

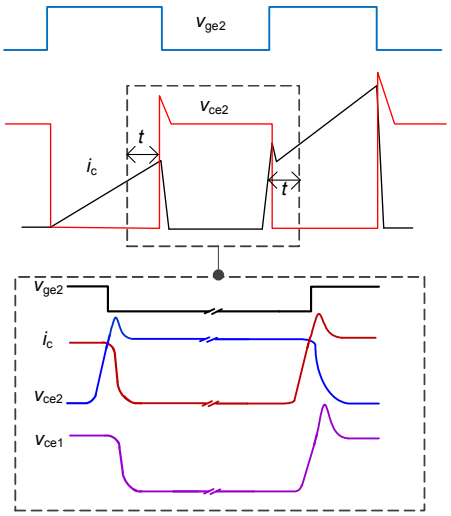

Fig. 2 Voltage and current waveforms when the IGBT Q_2 turns off and on

Through the analysis of the voltage spike in the double pulse test circuit when the IGBT turns on and off, it is known that under the half bridge structure, the turn-off speed of a tube determines its turn-off voltage spike and the turn-on speed determines the current spike and voltage spike of the other tube on the bridge. As a result, when considering the bridge structure, both of the IGBT's turn-on and turn-off speeds have a great influence on the switching voltage spike.

3 Driving pulse edge modulation technique

From the analysis above, it can be seen that reducing the IGBT's turn-on and turn-off speed is effective in restraining the switching voltage spike. With the development of digital drive techniques, new strategies are available to regulate the IGBT gate driving voltage to control the turn-on and turn-off speed.

3.1 Common gate drive circuit

Fig. 3 shows a traditional equivalent IGBT gate drive circuit. To regulate the turn-on and turn-off speed separately, it is common to use two gate resistors with different values. At one time point, one driving power supply is active and the other is cut off from the drive circuit, depending on the drive signals.

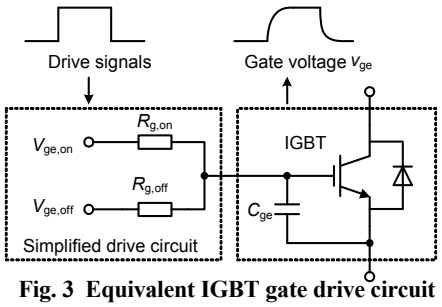

Fig. 3 Equivalent IGBT gate drive circuit

$V_{ge,on}$ and $V_{ge,off}$ refer to the driving power supply positive and negative voltages, respectively, and C_{ge} is the gate capacitance

Regardless of the Miller effect, the behavior of the driving circuit can be treated as the charging and discharging processes of an RC circuit under a square wave power supply. The turn-on and turn-off gate voltages during switching can be approximately expressed as follows (explanations for parameters will be given later):

$$v_{ge,on}(t) = V_{ge,off} + (V_{ge,on} - V_{ge,off})\left(1 - e^{\frac{-t}{R_{g,on}C_{ge}}}\right), \quad (3)$$

$$v_{ge,off}(t) = V_{ge,on} + (V_{ge,off} - V_{ge,on})\left(1 - e^{\frac{-t}{R_{g,off}C_{ge}}}\right). \quad (4)$$

3.2 Driving pulse edge modulation technique

From Eqs. (3) and (4), it can be seen that not only the gate resistance, gate capacitance, and gate power supply voltage values but also the action time of the driving power supply, influence the gate voltage during the switching period. As indicated by Eq. (3), the gate voltage $v_{ge,on}$ cannot rise up to a stable value without enough input high level time of the driving circuit. When the time decreases, the peak value of $v_{ge,on}$ reduces accordingly, and the voltage will start to fall even before it reaches the turn-on threshold $V_{ge,th}$. Nonetheless, the increase in $v_{ge,on}$ in the RC circuit is still influenced by the initial value. As a result, the

gate voltage of an IGBT has a cumulative effect, and Eqs. (3) and (4) can be expressed as Eqs. (5) and (6), respectively, in which t_n is the width of positive pulse signal:

$$v_{ge,on}(t)=v_{ge}(t)|_{t=t_n}+(V_{ge,on}-v_{ge}(t)|_{t=t_n})\left(1-e^{\frac{-t}{R_{g,on}C_{ge}}}\right), \quad (5)$$

$$v_{ge,off}(t)=v_{ge}(t)|_{t=t_n}+(V_{ge,off}-v_{ge}(t)|_{t=t_n})\left(1-e^{\frac{-t}{R_{g,off}C_{ge}}}\right). \quad (6)$$

According to the area equivalence principle, pulses with equivalent area but different shapes have the same effect on inertial elements. Therefore, the gradually rising and falling edges of the gate driving pulse signal can be mapped into pulse trains. Based on digital techniques, we introduce a new method, named driving pulse edge modulation, to regulate the turn-on and turn-off speed of IGBTs. Take the IGBT turn-on process, as an example. This method maps the rising edge of the driving pulse signal into a pulse train (Fig. 4a), and the gate driving voltage turns accordingly into the accumulation of each pulse's response (Fig. 4b).

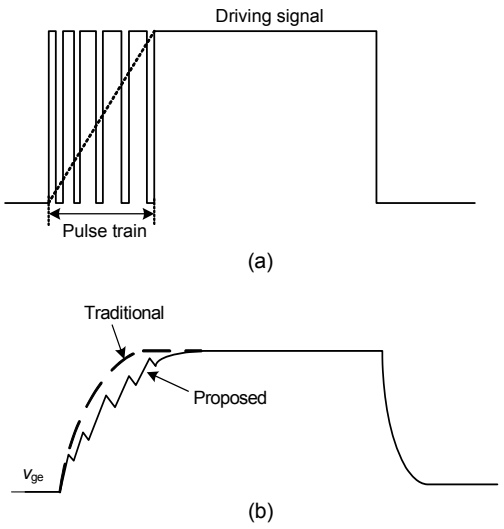

Fig. 4 Pulse train (a) and gate voltage response (b)

Compared with the normal turn-on gate driving voltage curve, though not smooth, the rising slope with this modulation method does decline. That response can also be seen when imposing a pulse train before the traditional gate driving signal. By mapping the driving pulse edge into a pulse train, the modulation of the pulse edge can be changed into the modulation of the width and density of the pulse train. Ideally, the driving pulse edge can be modulated arbitrarily if the pulse train is modulated only with given width and density. It is the same when considering the turn-off process. Driving pulse edge modulation can be realized by using the following two methods of driving power (bidirectional and unidirectional).

3.2.1 Bidirectional pulse train modulation

Fig. 5 shows the basic principle during the turn-on and turn-off switching periods using the driving pulse edge modulation method. The modulated pulse width modulation (MPWM) signal is realized by imposing a series of positive and negative levels. When the signal is positive, the positive driving voltage $V_{ge,on}$ is used, and when the signal is negative, the negative driving voltage $V_{ge,off}$ is used. This method is called bidirectional pulse train modulation (BPTM).

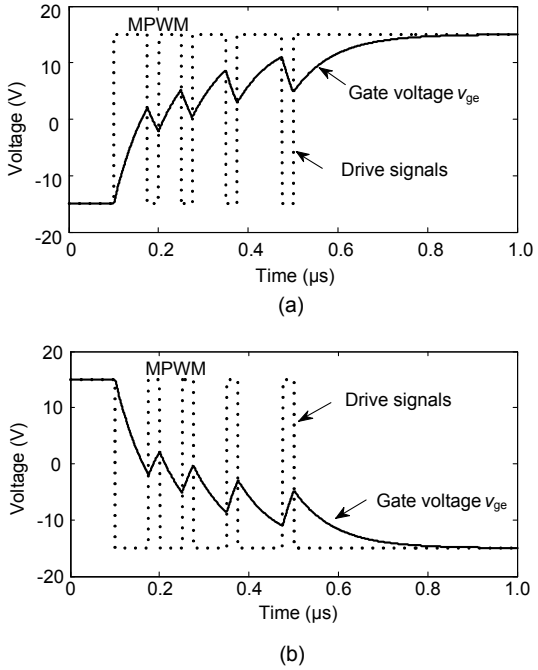

Fig. 5 Waveforms of drive signals and IGBT gate voltage v_{ge} based on pulse edge modulation: (a) turn-on period; (b) turn-off period

The higher the pulse train density, the higher the accuracy that can be achieved by gate voltage regulation. The pulse width and density depend not only on the processing speed of the digital chip that produced the driving signals, but also on the bandwidth of the drive circuit, which is between the chip and IGBT gate and usually plays a role in power amplification. In fact, the pulses are useful only when the gate voltage is around the gate threshold voltage $V_{ge,th}$. So, pulses with proper width and action time are recommended.

During the IGBT's turn-on period, if the response capability of the driving circuit is limited, the edge of the gate driving voltage will appear as an obvious zigzag. As a result, the gate voltage will fluctuate around the turn-on threshold voltage $V_{ge,th}$ (Fig. 6), which will cause the pseudo turn-on of the IGBT. The pseudo turn-on problem will influence the output performance of the main circuit, increase the IGBT switching loss, and decrease the system's reliability.

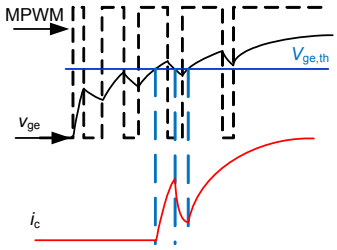

Fig. 6 Pseudo turn-on problem with the BPTM method

3.2.2 Unidirectional pulse train modulation

Considering the serrated gate voltage edge shown in Fig. 6, if the fluctuation can be reduced, or even be kept stable during the original falling segment, the pseudo turn-on problem will be solved. Based on a similar principle, a pulse train is still added before the traditional driving signal to modulate the driving pulse's edge. However, unlike the BPTM method, when modulating the rising edge, the high level signal means connecting to the positive driving voltage $V_{ge,on}$ and the low level signal means connecting to nothing, which will keep the gate voltage stable. When modulating the falling edge, the high level signal means connecting to the negative driving voltage $V_{ge,off}$ and the low level signal means connecting to nothing. We define this method as unidirectional pulse train modulation (UPTM).

Fig. 7 shows the modulation waveforms of UPTM, in which $G_{Vge,on}$ and $G_{Vge,off}$ represent the control signals of the positive and negative driving voltages, respectively. A high level of a control signal means the driving voltage is controlled to connect with the IGBT gate, and a low level means no driving signal connects to the gate. Take the driving circuit shown in Fig. 3 as an example. Considering the turn-on stage of the IGBT, the control signal of the negative driving voltage $G_{Vge,off}$ keeps low and the control signal $G_{Vge,on}$ of the positive driving voltage consists of alternate signals, i.e., with high and low levels. When $G_{Vge,on}$ is high, the gate voltage v_{ge} increases for connecting to positive driving voltage and when $G_{Vge,on}$ is low, the gate voltage v_{ge} remains unchanged for connecting to no driving voltage. As a

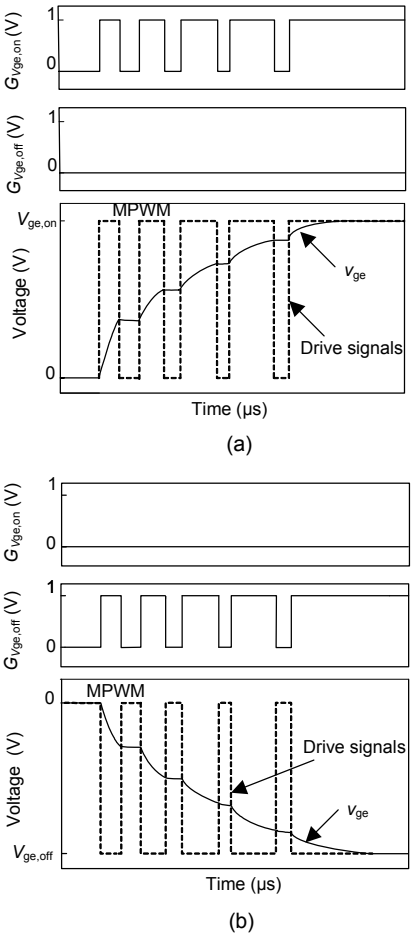

Fig. 7 Waveforms when using the UPTM method: (a) turn-on process; (b) turn-off process

result, when adopting the UPTM method, no falling segment of gate voltage exists, thus solving the IGBT's pseudo turn-on problem. As for the modulation of the falling edge of the gate pulse, the principle is similar.

Both of the pulse edge modulation methods mentioned above can be realized in a digital chip by adding a pulse train before the traditional PWM signal, and the rising and falling speed of the IGBT's gate voltage can be adjusted according to the demands of the circuit. Compared with the BPTM method, the UPTM is more complicated because of its separate control of positive and negative driving voltages, and the range of speed regulation of the gate voltage is smaller. However, being smoother, the UPTM can solve the pseudo turn-on problem, and the requirement of the driving circuit's response speed also diminishes.

3.3 Gate driver with the proposed technique

The structure of the gate driver with the pulse edge modulation technique is given in Fig. 8. Its components are similar to those of other digitalized drivers. The digital chip can be a digital signal processor (DSP), an FPGA, or a CPLD. The driver realizes most of the logic processing, including PWM transformation, fault detection, pulse edge modulation, and dead time management.

The digital chip receives the PWM control signal from the controller and produces the MPWM signal to be changed into the positive and negative levels through a voltage level conversion module. Through the power amplification module, the driving voltage of the IGBT is finally obtained. Unlike the traditional driving circuit, only one gate resistor is required because the turn-on and turn-off speed can be regulated through the pulse edge modulation technique. Normally, the driver can provide the same driving pulse as the traditional driver and the digital chip operates in detecting mode. When the relatively large switching spike of the IGBT is detected, the digital chip uses the pulse edge modulation technique to impose the pulse train signal to restrain the switching spike by lowering the slope of the driving pulse edge.

The concrete driving circuit structure using CPLD is shown in Fig. 9. Under the BPTM operation mode, the metal-oxide-semiconductor field-effect transistors (MOSFETs) M_1 and M_2 switch on and off alternately to modulate the driving pulse edge. Under the UPTM operation mode, only one MOSFET switches on and off to modulate the driving pulse edge, and the other MOSFET's driving signal is blocked. As mentioned above, the smallest bandwidth of the three steps shown in Fig. 8 decides the accuracy of the gate voltage with the driving pulse edge modulation method. Thus, the driver with the proposed method may have a higher requirement for chips and design. When using BPTM, the requirement for the processing speed of the digital chip is high, because the digital chip needs to produce pulse trains with high density to solve the pseudo turn-on and turn-off problem, but the UPTM method decreases the requirement on the processing speed.

When adopting the driving pulse edge modulation method, no extra devices are needed, because its structure is similar to that of the traditional digital IGBT driver. Because of the pure digital implementation, it is very easy to adjust the rising and falling speed of the IGBT gate driving voltage to reduce the switching spikes.

4 Experimental evaluation of the digitalized IGBT gate driver

One purpose of the IGBT gate driver is to minimize the turn-off peak voltage v_{ce} during the

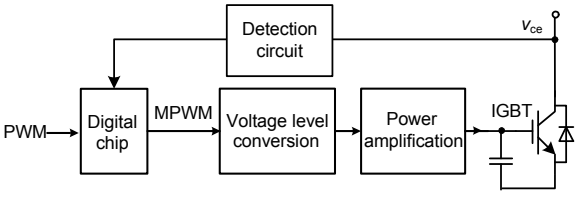

Fig. 8 IGBT driver structure based on the digital technique

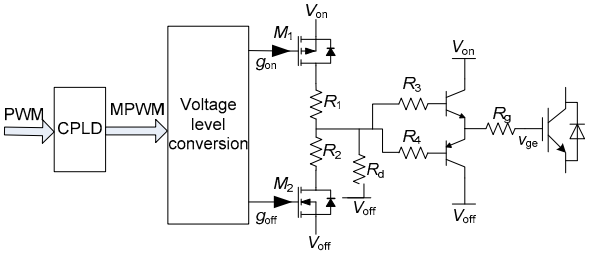

Fig. 9 Concrete driving circuit using CPLD

IGBT turn-off period based on the digital technique. To validate the ability of the digitalized gate driver with the driving pulse edge modulation technique, a gate driver was designed according to Fig. 8. The driver was applied to a full bridge converter (Fig. 10). In practice, the DC voltage was established by a rectifier bridge and DC-link capacitors.

A type of CPLD which can run over 100 MHz was used as the digital chip (Altera MAX II series, model EPM570T100I). It receives PWM signals produced by an advanced controller. The IGBT chosen for the test was the Infineon FF450R12ME4. Table 1 shows some of the main parameters of the system.

Experimental tests revealed that the turn-off voltage was higher during the reverse recovery process. This means that reducing the turn-on speed is more effective in mitigating the turn-off overshoot voltage of the complementary transistor. So, the pulse edge modulation technique was used only during the turn-on period of the drive signals.

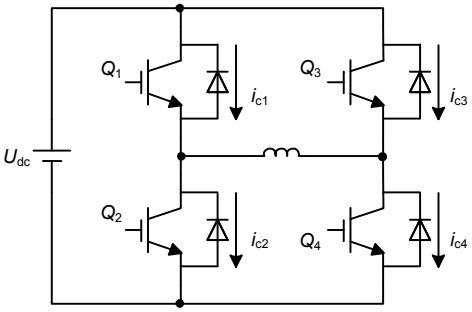

Fig. 10 Topology of the experimental platform

Fig. 11 shows the driving signals with additional pulse trains and the corresponding gate voltage. Fig. 11a shows the waveforms of the driving signal and gate voltage using the BPTM method. Clearly, the gate voltage increases with serration. Fig. 11b shows the waveforms using the UPTM method. In this case, the gate voltage increases without a falling segment.

A comparison of gate voltages before and after adopting the driving pulse edge modulation technique is shown in Fig. 12. Compared with the traditional driving method, the gate voltage using these two methods rises slowly, especially with the UPTM method (Fig. 12b).

The driving pulse edge modulation technique was applied to all the four IGBTs' gate drivers. Taking transistors Q_1 and Q_2 as the test objects, the DC-link voltage was fixed around 200 V. Fig. 13 shows the gate voltage v_{ge2} of Q_2 and the collector-emitter voltage v_{ce1} of Q_1 with and without the proposed driving pulse edge modulation technique. When the IGBT turns on at a high speed (Fig. 13a), the switching voltage spike was about 100 V. After using the two driving pulse edge modulation methods mentioned above, the voltage spike of Q_1 was almost

Table 1 Main parameters of the experimental prototype

Symbol	Parameter	Value
$V_{ge,on}$	Positive drive supply voltage	+15 V
$V_{ge,off}$	Negative drive supply voltage	–15 V
R_g	Gate resistance	3.6 Ω
f_{sw}	IGBT switching frequency	5 kHz
f_{osc}	Operating frequency of CPLD	40 MHz

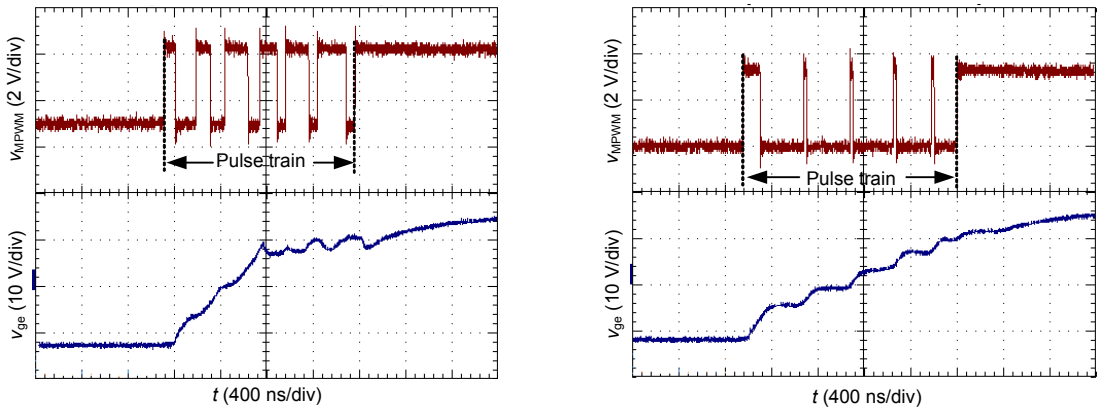

Fig. 11 MPWM signals and IGBT gate voltage with additional pulses during the turn-on period: (a) BPTM; (b) UPTM

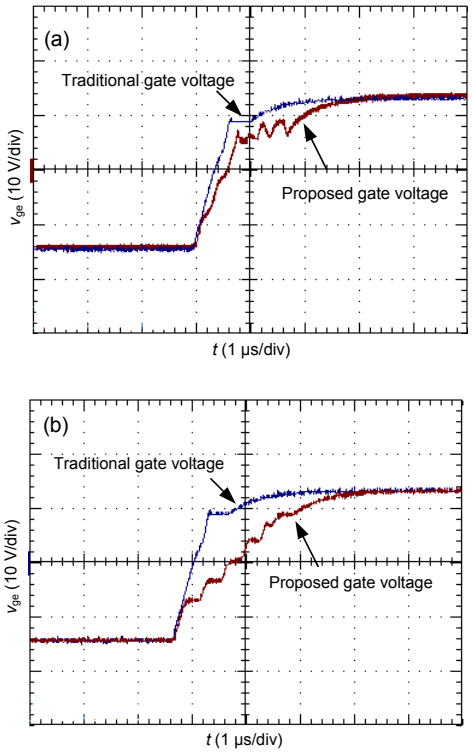

Fig. 12 Waveforms of IGBT gate voltages before and after adopting the pulse edge modulation technique: (a) BPTM; (b) UPTM

zero (Figs. 13b and 13c), confirming a strong suppression effect.

Fig. 14 shows the pseudo turn-on problem of Q_2 when using the BPTM with the gate voltage fluctuating around the turn-on threshold voltage of the IGBT. The voltage of Q_1 (v_{ce1}) between the collector and emitter was distorted during the pseudo turn-on time of Q_2.

Not only is the turn-on speed of one transistor slowed down by adopting the driving pulse edge modulation technique, but also the turn-off speed of its geminate transistor is reduced if its freewheeling diode operates with a reverse recovery process. However, the reduction of switching speed may also lead to higher switching power loss of the IGBTs, which is also unavoidable with traditional methods for reducing switching speed. Therefore, the design of driving pulse edge modulation should take overall consideration of both switching voltage spike and switching power loss.

Fig. 15 shows the waveforms of collector-emitter voltage, collector current, and device power

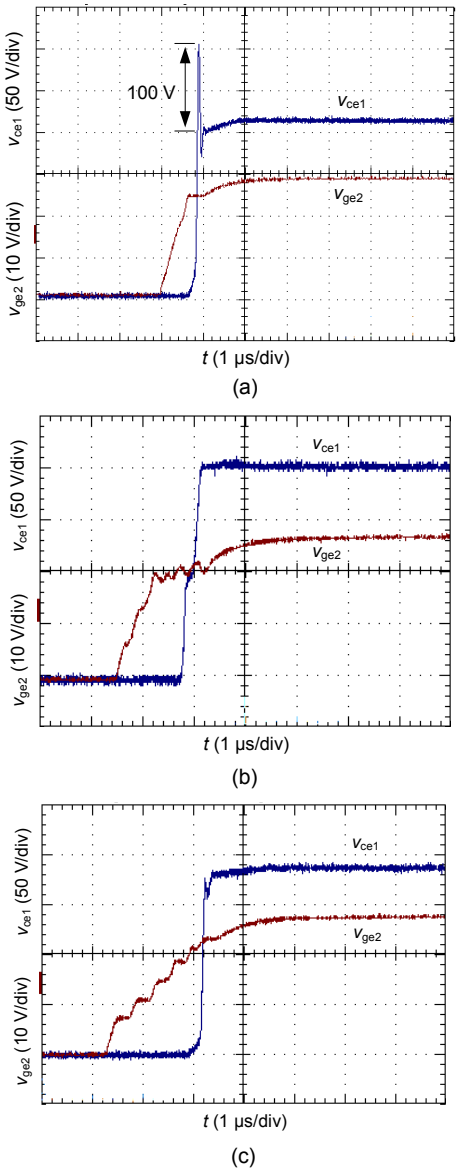

Fig. 13 Waveforms of the IGBT gate voltage of Q_2 and collector-emitter voltage of Q_1: (a) TDS; (b) BPTM; (c) UPTM

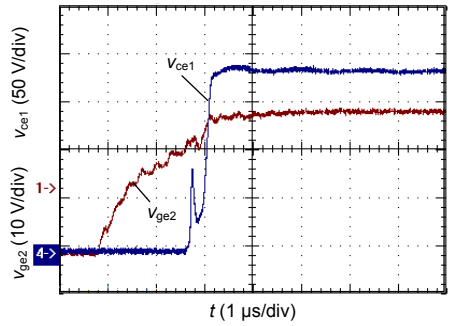

Fig. 14 Pseudo turn-on problem with the BPTM method

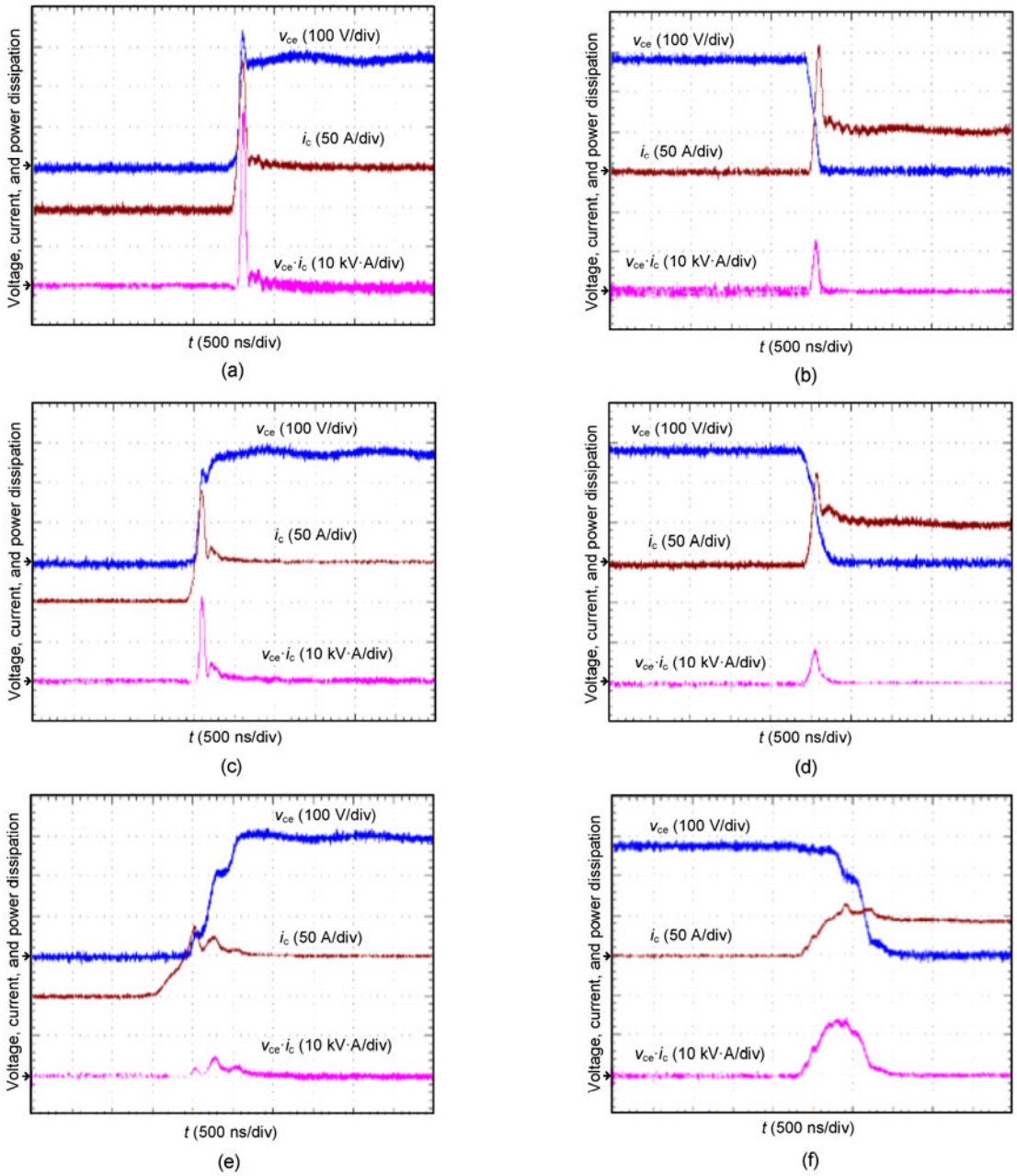

Fig. 15 Waveforms of the IGBT collector-emitter voltage, collector current, and power dissipation during the turn-on period (right column) and turn-off period (left column) using a traditional driver with small gate resistance ((a) and (b)), a traditional driver with large turn-on gate resistance ((c) and (d)), and our proposed pulse edge modulation technique ((e) and (f))

dissipation during IGBT turn-on and turn-off periods with the three different drive conditions, i.e., the traditional drive method with small gate resistance (3.6 Ω), the traditional drive method with larger turn-on gate resistance (10 Ω), and the proposed BPTM method.

When using the traditional drive, both the switching voltage spike and reverse current of the freewheeling diode are the most serious among all three conditions (Figs. 15a and 15b). The power dissipation is very large during the turn-off period due to the simultaneously high voltage and large current.

With a larger gate resistance (Figs. 15c and 15d), the switching voltage spike is suppressed effectively and the reverse current is also smaller. Consequently,

the power dissipation during both the turn-on and turn-off periods is reduced to a certain extent.

Using the proposed BPTM technique, the switching voltage spike totally disappeares and the reverse current is much smaller with regard to the former two cases. Furthermore, the turn-off power dissipation is further reduced (Fig. 15e). However, in spite of the smaller collector current, the total turn-on power loss is larger on account of the slow conduction process (Fig. 15f).

If the conduction process is too slow, there will be a large power loss during the turn-on period. Fortunately, the switching speed can be easily regulated by programming. Taking the BPTM technique as an example, Fig. 16 shows several gate voltages under different pulse assignations. With various gate voltages, the turn-on and turn-off processes are different.

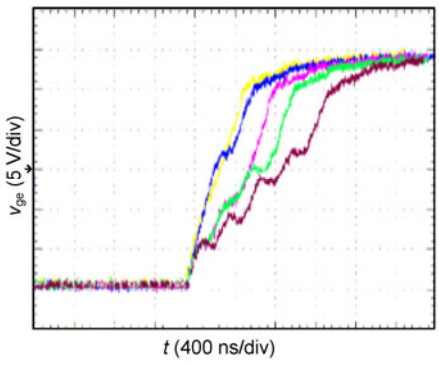

Fig. 16 Waveforms of IGBT gate voltages with different pulse assignations

5 Conclusions

In this paper, a new driving pulse edge modulation technique based on a digital driver for regulating the IGBT turn-on and turn-off speed is introduced. The possibility of realizing a digitalized technique to suppress the switching voltage spike is demonstrated. With the implementation of CPLD, the switching speed can be easily regulated by programming. The effectiveness and validity of the technique are demonstrated by experiments on a full bridge converter. The main features can be summarized as follows:

1. Modulation can be achieved totally by using digital techniques and can be used in different working conditions without changing the structure of drive circuits.

2. Only one CPLD (or FPGA) is used and no specific properties are required.

3. The pseudo turn-on problem can be solved by using the UPTM method, and the low requirement on the response speed of the driving circuit gives it better applicability.

4. The method is flexible in application due to its digitalization.

Future work will address further practical applications of the proposed gate driver, including the detection of the switching voltage spike, intellectualized and automatic setting pulses based on the detection, and achieving a better balance between voltage spike suppression and power loss and other practical problems.

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