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RESEARCH ARTICLE

Huaisheng WANG, Mingxiang WANG, Zhenyu YANG

Finite element analysis of temperature distribution of polycrystalline silicon thin film transistors under self-heating stress

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Abstract The temperature distribution of typical n-type polycrystalline silicon thin film transistors under self-heating (SH) stress is studied by finite element analysis. From both steady-state and transient thermal simulation, the influence of device power density, substrate material, and channel width on device temperature distribution is analyzed. This study is helpful to understand the mechanism of SH degradation, and to effectively alleviate the SH effect in device operation.

Keywords finite element analysis (FEA), temperature distribution, thin film transistors, self-heating, steady-state, transient state

1 Introduction

Low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) are key elements to realize a flat panel display with its pixel array integrated with peripheral driver circuits [1]. Because of low thermal conductivity of the glass substrate in TFTs, the self-heating (SH) effect resulting from current Joule heating is a concern when TFTs are operated in the ON-state [2–6]. On the one hand, similar to silicon on insulator (SOI) devices, the SH effect reduces the device output current [5]. On the other hand, it is a key mechanism for the device degradation of poly-Si TFTs [2–4]. It is known that in the SH effect, the device channel temperature rise is a critical factor to induce variation or degradation of device characteristics. However, precise measurement of actual channel temperature distribution is a major difficulty in SH study [3–6]. Currently available experimental approaches such as infrared pyrometer [3] or Pt thermometer [6] can only offer indirect measurement and a rough estimate of the channel temperature, while information about temperature distribution features cannot be obtained. However, simulation by finite element analysis (FEA) is an effective method to directly obtain the device channel temperature distribution under SH [3–4], only if the boundary conditions and heat transfer model of the device under SH electrical stress can be adequately taken into account. The simulation results are helpful to clarify the mechanism of SH degradation.

In this study, both steady-state and transient temperature distribution of n-type metal-induced laterally crystallized (MILC) poly-Si TFTs [1] under typical SH bias condition are simulated by FEA. Influences of electrical bias, device size and structure on the temperature distribution are also investigated, which provide useful information for the study of the mechanism of SH degradation and optimization of the device geometry to alleviate the SH effect.

2 Device fabrication and SH degradation

TFTs used in this study were in the conventional self-aligned top-gate structure [1,4]. First, a 50 nm amorphous-Si (a-Si) was deposited on an oxidized silicon wafer by low pressure chemical vapor deposition (LPCVD). After patterning active areas, 100 nm low-temperature oxide (LTO) as gate dielectric and 300 nm a-Si layer as gate material were deposited sequentially, and the gate electrode was then etched. A crystallization-inducing window was opened through the LTO and 5 nm Ni was evaporated by electron-beam. Subsequently, channel MILC and gate MIC processes were performed simultaneously through 550°C, 24-hour annealing. After Ni removal, self-aligned phosphorous implantation done twice, with each dose of 2×10^{15} cm^{-2}, was introduced to form the source and drain. Implantation energies were

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Huaisheng WANG, Mingxiang WANG (✉), Zhenyu YANG
Department of Microelectronics, Soochow University, Suzhou 215021, China
E-mail: Mingxiang_wang@suda.edu.cn

90 keV and 120 keV, respectively. Phosphorus ions were then activated at 620°C for 3 hours. Finally, contact holes were opened before aluminum layer sputtering and patterning. A schematic illustration of the cross section of the TFT devices is shown in Fig. 1.

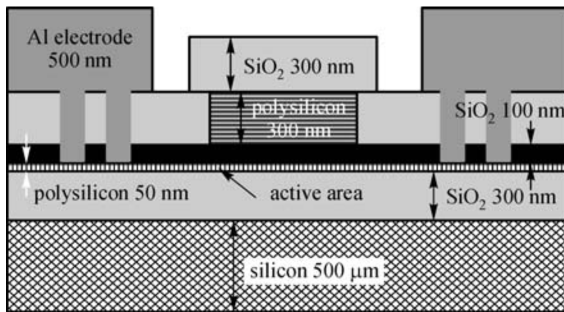

Fig. 1 Schematic illustration of cross section of TFT

Figure 2 is the stress time-dependent degradation of the transfer characteristic (measured at V_{ds}= 0.1 V) of an n-channel MILC TFT (W/L = 10 μm/6 μm) under a typical SH stress condition (V_g= 35 V, V_d= 18 V). Generally, one sees a decrease of ON-state current (I_D), an increase of OFF-state current, an increase of threshold voltage (V_T), and a degradation of subthreshold slope. Previous studies [2–4] show that a large channel temperature rise can result in an increase of interface trap density within the channel region by breaking the weak Si-H bond at Si/SiO_2 interface and/or grain boundaries, which causes the observed SH degradation. Therefore, it is highly desirable for an SH study to precisely obtain the device channel temperature distribution under SH stress. In this study, both steady-state and transient temperature distribution of n-type MILC TFTs were simulated under various stress conditions. Influences of different stress power densities, substrate materials and device widths/lengths (W/L) on the temperature distribution were also analyzed.

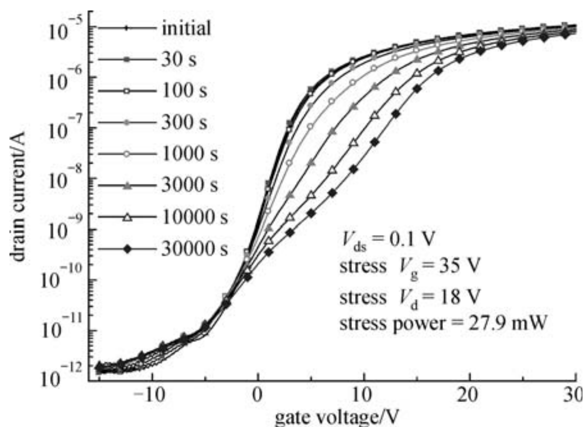

Fig. 2 Transfer characteristic degradation of n-channel MILC TFT under SH stress

3 FEA thermal model

By using a commercial tool ANSYS, a three-dimensional (3D) FEA single device model was built for each device W/L. As shown in Fig. 3, a TFT is located in the center of a 4-inch silicon wafer or Corning glass substrate. SOLID-70 element is used for FEA calculation. It is noted that only a small volume containing the TFT device needs to be fine meshed, although the FEA model includes the entire substrate. To investigate the influence of stress power density, steady-state simulation was performed for TFT on silicon wafer under 11 different electrical stress conditions, while transient simulation was performed only for a selected typical stress condition. For TFT on glass substrate, both steady-state and transient simulations were performed for a typical stress condition. All FEA thermal models and corresponding electrical stress conditions were listed in Table 1. Threshold voltage V_T and ON-state current I_D were listed according to the measured values on device with W/L = 10 μm/6 μm. Thermal properties of all related materials for FEA are shown in Table 2.

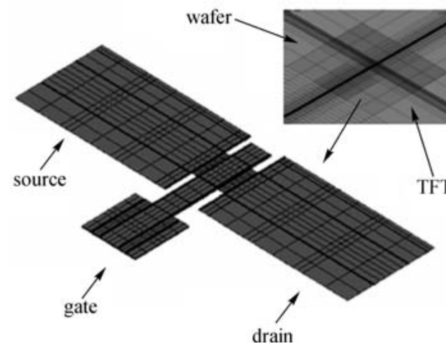

Fig. 3 Single device finite element model used for TFT thermal analysis

Table 1 Electrical stress conditions simulated in thermal analysis models with different W/L and substrate types

substrate	FEA models	self-heating electrical stress conditions				transient simulation
		V_D/V	V_G/V	V_T/V	I_D/mA	
silicon wafer	(W/L)/ (μm/μm) A1:10/6 B1:20/6 C1:40/6 D1:100/6 E1:200/6	18	30	5.1	1.17	—
		16	35	4.7	1.42	—
		20	30	4.6	1.25	—
		18	35	4.8	1.41	—
		18	35	4.55	1.55	yes
		17	35	5.3	1.74	—
		20	35	4.7	1.58	—
		24	30	5.9	1.35	—
		18	35	4.9	1.83	—
		22	30	4.05	1.51	—
	saturation: 10/6	25	30	4.85	1.39	—
Corning 1737	A2–E2 10/6–200/6	8.5	20	4.55	0.485	yes

Table 2 Thermal parameters of different materials used in simulation

materials	density/(kg·m^{-3})	specific thermal capacity/(J·kg^{-1}·K^{-1})		thermal conductivity/(W·m^{-1}·K^{-1})	
Al	2700	900		237	
polysilicon (undoped in Refs. [7,8])	2330	716.2		15	
polysilicon (doped in Refs. [7,8])	2330	716.2		45	
Si in Ref. [9]	2330	700		27°C	156
				127°C	105
				227°C	80
				327°C	64
SiO_2 in Ref. [10]	2200	1000		27.71°C	1.3
				59.7°C	1.35
				93.62°C	1.39
				129.2°C	1.42
				151.3°C	1.47
				177.9°C	1.5
				204.8°C	1.53
Corning 1737 glass in Ref. [11]	2540	23°C	707.6	23°C	0.91
		50°C	736.9	50°C	0.95
		100°C	795.5	100°C	1.03
		200°C	891.8	200°C	1.14
		300°C	971.3	300°C	1.22

Temperature dependence of those properties of Si, SiO_2, and Corning 1737 glass were included in the simulation.

It is known that the SH effect originates from the current Joule heating in the inversion channel when TFT is at ON state. Hence, the inversion layer (typical thickness is set as $d = 5$ nm) is the heat generation source in the FEA thermal model. Local heat generation power dP along the inversion channel at $y \rightarrow y + \mathrm{d}y$ could be expressed as [12]

$$\mathrm{d}P = I_\mathrm{D}^2 \mathrm{d}R = \frac{I_\mathrm{D}^2 \mathrm{d}y}{\mu W C_\mathrm{ox}(V_\mathrm{G} - V_\mathrm{T} - V_y)}, \tag{1}$$

where dR is the channel resistance of $y \rightarrow y + \mathrm{d}y$, μ is the channel carrier mobility, V_y is the voltage drop along the device channel at position y, and C_ox is the gate oxide capacitance per unit area. Since V_y increases from the source electrode ($V_\mathrm{S} = 0$) to the drain electrode V_D, it can be seen from Eq. (1) that channel resistance dR and heat generation dP also increase. In Table 1, the 12 electrical stress conditions listed are all in the linear region of device operation (saturation condition is set at the limit of the linear region and the beginning of saturation). Therefore, V_y varies along the channel gradually. In the FEA thermal model, heat generation along the channel dP could be approximated as a linear increase from the source to the drain. Heat generation power density at the source and drain edge can be deduced as

$$\text{source: } P_\mathrm{S} = \frac{2I_\mathrm{D}V_\mathrm{D}}{WLd} \frac{V_\mathrm{G} - V_\mathrm{D} - V_\mathrm{T}}{2V_\mathrm{G} - V_\mathrm{D} - 2V_\mathrm{T}},$$

$$\text{drain: } P_\mathrm{D} = \frac{2I_\mathrm{D}V_\mathrm{D}}{WLd} \frac{V_\mathrm{G} - V_\mathrm{T}}{2V_\mathrm{G} - V_\mathrm{D} - 2V_\mathrm{T}}.$$

For heat transfer boundary conditions, by considering typical ambient of a stressed device, the bottom plane of the substrate (which is in contact with a wafer chuck) is set at a fixed temperature of 27°C, while all the other surrounding surfaces are set as natural convection by air with a typical convective coefficient $h = 7.5$ W/(m·K) [13].

4 Temperature distribution in device channel

Channel temperature distribution was first investigated with a device on silicon wafer ($W/L = 10$ μm/6 μm) under a typical SH stress condition (as shown in Table 1, stress power = 27.9 mW). In Fig. 4, the temperature rise within the device channel under SH stress is evident. The temperature rise is symmetrically distributed along the

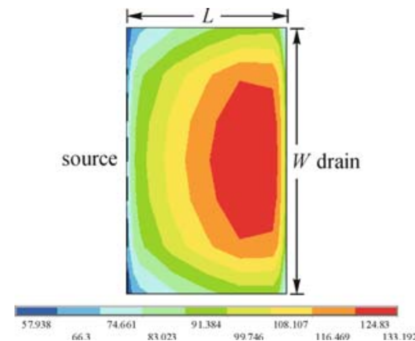

Fig. 4 Channel temperature distribution simulated in $W/L = 10$ μm/6 μm TFT model on Si substrate with stress power = 27.9 mW

channel width direction, while along the channel length the high temperature region is significantly shifted to the drain side. Peak temperature of ~133°C is located in mid-channel width and near the drain edge, due obviously to the higher channel resistance and larger heat generation near the drain side.

Figures 5(a) to 5(c) show the temperature distributions crossing the peak temperature point in the inversion channel along the length, width and thickness directions, respectively. It is seen that channel temperature increases from the source to the drain, where a high temperature region forms. At both source and drain edges, because of lateral heat dissipation from the channel to the outside, temperature decreases dramatically with a high temperature gradient (62 K/μm) at the boundaries between the channel and source/drain. In terms of width, the temperature distribution is precisely symmetrical and the temperature gradient (15 K/μm) at the edges is much smaller than that in the length direction, reflecting that source/drain metallizations are important lateral heat dissipation paths. In the vertical direction, the temperature gradient in the bottom oxide (319 K/μm) is far larger than that in the gate oxide (78 K/μm). It indicates that the device bottom substrate is the key vertical heat dissipation path. Since heat dissipation area in the channel direction WL is far larger than that in the lateral direction $2Wd$, heat conduction through the silicon substrate is the primary dissipation path under SH stress. Compared to that stressed in the linear region, the temperature distribution stressed in the saturation is obviously steeper from the source to the drain, with peak temperature significantly higher and located closer to the drain edge (only ~ 0.5 μm away from the edge). It is noteworthy that higher peak temperature is not only caused by higher stress power density, but also by the more concentrated power density distribution at the drain side in the saturation condition. By extracting the temperature gradient in lateral and vertical directions in saturation condition, it is found that both lateral heat dissipation from the drain edge and vertical heat conduction through the channel top surface increase compared to those in the linear region. However, the heat dissipation through the bottom silicon substrate still dominates.

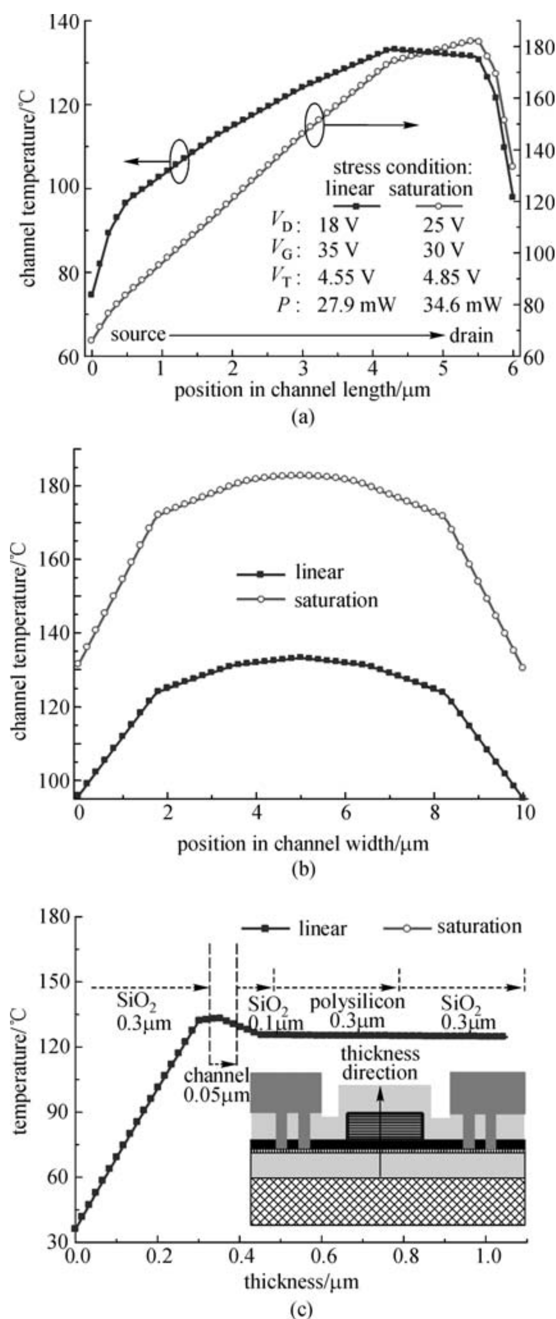

Fig. 5 Channel temperature distribution crossing peak temperature point in linear and saturation regions simulated in $W/L = 10$ μm/6 μm TFT model on Si substrate. (a) Along channel length direction; (b) along channel width direction; (c) along thickness direction from the bottom SiO_2 to device surface

In Fig. 6, temperature distributions for device on silicon wafers with different channel widths (W) but under the same electrical stress (the 5th row in Table 1) are compared. Although power densities are the same for devices with different W, it is found that W has significant influence on channel temperature rise. As W increases, although the channel temperature in the length direction follows almost the same distribution, the temperature rise gradually increases. In the width direction, not only the channel temperature rise increases with W, but its distribution becomes obviously flattened and its high temperature region is largely expanded. This indicates that if W increases, channel lateral heat dissipation becomes more difficult, leading to the higher temperature rise even if the stress power density is the same.

Shown in Fig. 7 is the channel peak temperature of TFT on silicon wafer with different W/L, dependent on stress power density obtained for 10 stress conditions listed in Table 1. The peak temperature increases with increasing SH stress power density, and similarly linear dependences are observed for all W/L devices. However, a data point obtained in saturation condition clearly deviates from the

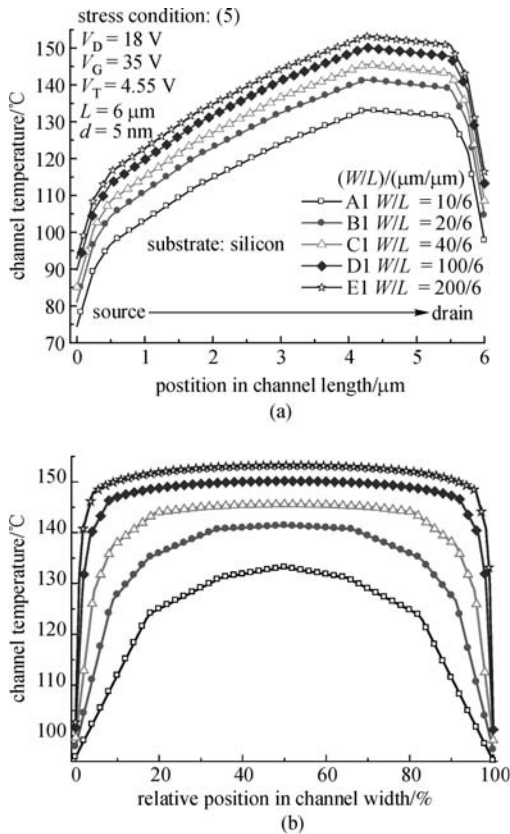

Fig. 6 Channel temperature distribution crossing peak temperature point simulated in TFT models on Si substrate with different W/L. (a) Along channel length direction; (b) along the relative position in channel width

linear dependence because of more concentrated power density distribution at the drain side as mentioned earlier. Furthermore, it is noted that the slope of the linear dependences gradually increases with increasing W/L, showing that the device with larger W/L has larger thermal resistance per unit area and its channel temperature rise is more sensitive to device power. It is in accordance with

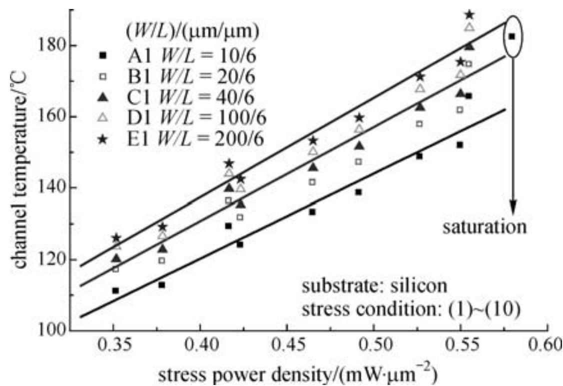

Fig. 7 Channel peak temperature dependent on stress power density simulated in TFT models on Si substrate with different W/L

previous observation from Fig. 6(b) that a wider device poses more difficulty for lateral heat dissipation.

5 Influence of substrate materials

In practical applications, TFT devices are often fabricated on the glass substrate. Here, the channel temperature distribution of a device on glass substrate (W/L = 10 μm/ 6 μm) under a typical SH condition (the 12th row in Table 1, stress power = 4.1 mW) is simulated to observe the influence of different substrate materials. Figures 8(a) to 8(c) show the temperature distributions crossing the peak temperature point in the inversion channel along the length, width and thickness directions respectively. Apparently, for TFT on glass substrate, a far smaller stress power density (~1/7 of that for the device on silicon wafer) can result in an equivalent channel temperature rise. Clearly, because of its low thermal conductivity, the bottom glass substrate effectively prevents Joule heating from dissipating through, resulting in the observed high channel temperature rise. Similarly, along the channel length direction, the high temperature region is still near the drain side, while along the width direction the distribution is also symmetrical. By comparing the temperature gradient in width and length directions, it is found that lateral heat dissipation in the channel length direction is still dominant, similar to that in the device on silicon wafer. The difference in substrate materials has minimal influence on lateral heat dissipation. From Fig. 8(c), along the thickness direction, the temperature gradient in the bottom oxide is estimated as 19 K/μm. Compared to that of the device on silicon wafer in Fig. 5(c), the heat dissipation through the bottom glass substrate is only ~1/17. In contrast, the temperature gradient in the gate oxide is ~ 40 K/μm (Fig. 8(c)). The heat dissipation through the channel top surface becomes more important for the TFT on glass substrate because of the low thermal conductivity of glass, i.e., the bottom substrate material change directly causes the change in the dominant device heat dissipation path in the vertical direction.

6 Transient temperature simulation

Rising/falling time dependent channel temperature can be studied by using transient simulation. It can be performed by ANSYS using a time integration option, after applying/ removing a stress power on/from the device FEA model at $t = 0$. Transient thermal simulation is performed for a device on silicon or glass substrate under typical SH stress, as shown in Table 1. Figure 9 shows the transient temperature curve of the steady-state peak temperature point upon applying/removing the SH stress on/from a device on silicon wafer (W/L = 200 μm/6 μm). It is shown that the temperature variation is very fast before the

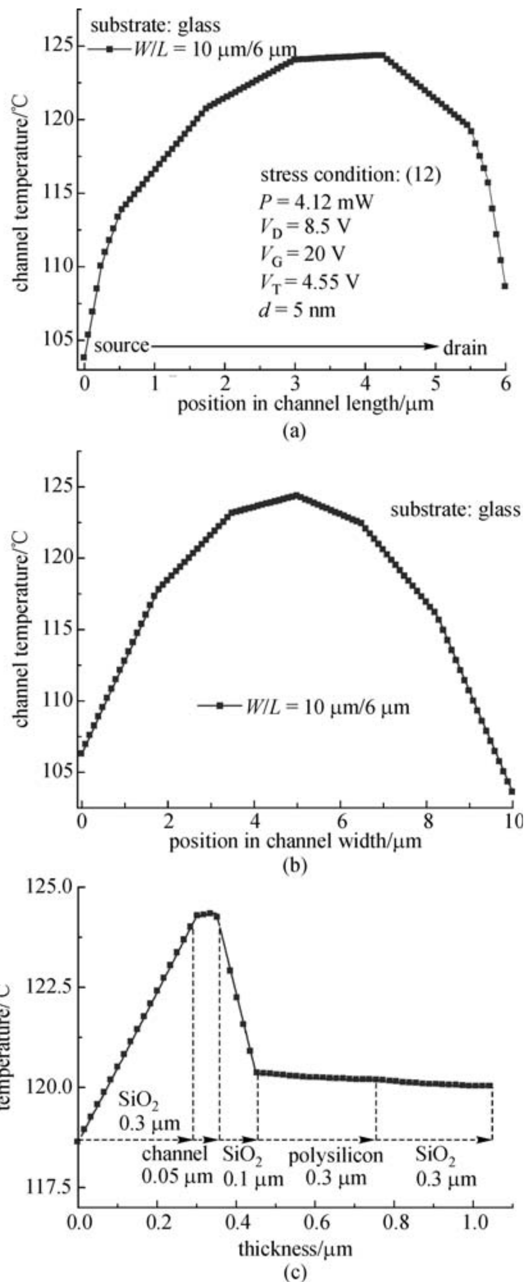

Fig. 8 Channel temperature distribution crossing peak temperature point simulated in $W/L = 10\ \mu m/6\ \mu m$ TFT model on glass substrate. (a) Along channel length direction; (b) along channel width direction; (c) along thickness direction from the bottom SiO_2 to device surface

channel temperature reaches a steady-state value for both rising and falling temperature. The time constant τ can be introduced to describe the transient temperature curve:

$$T(t) = T_\infty - (T_\infty - T_0)e^{-t/\tau}, \quad (2)$$

where T_0 is initial temperature, i.e., room temperature for heating and high temperature for cooling process; and T_∞ is steady-state temperature, i.e., high temperature for

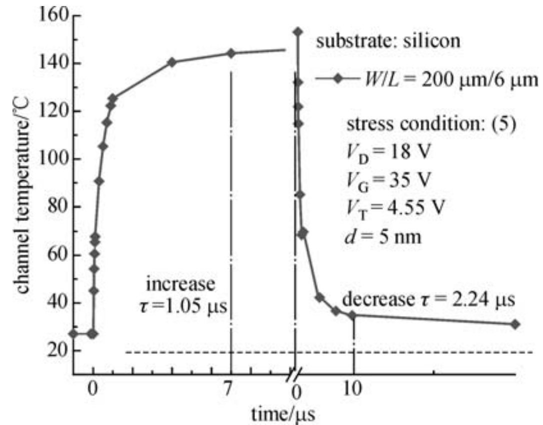

Fig. 9 Transient rising and falling temperature curves simulated in TFT model with $W/L = 200\ \mu m/6\ \mu m$ on Si substrate

heating and room temperature for cooling process. τ is determined by material thermal properties and device geometry. By curve fitting, τ for temperature rising/falling is estimated at 1.05 μs/2.24 μs. The discrepancy between the two values may relate to the difference in material thermal conductivity at room and high temperature.

Figure 10 shows the falling time constant τ depending on W for the device on silicon and glass substrate. Apparently, τ increases with increasing W following a linear trend in both cases. This is attributed to the larger thermal capacity for a larger v/L device. It is noteworthy that τ for device on glass is far larger than that for device on silicon wafer (~ 60 times). Again, the result indicates that the low thermal conductivity of glass substrate effectively blocks heat dissipation under SH.

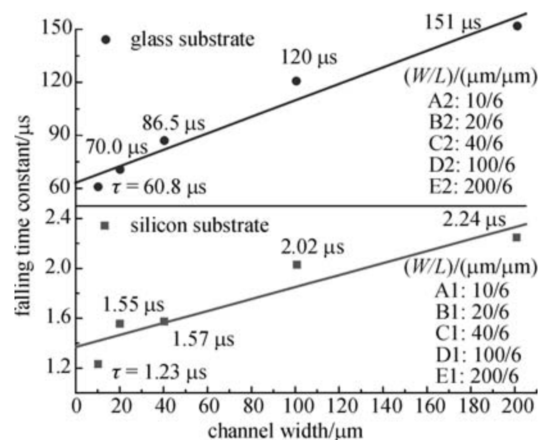

Fig. 10 Falling time constant τ dependent on W from TFT models with different W/L on Si or glass substrate

Finally, simulation error is discussed. By comparing the results from different computations, random error of numerical computation in convergence introduces channel temperature error < 0.2°C and can be neglected. A possible

error should be related to the accuracy of material thermal parameters used in the simulation. Presently, temperature dependent thermal parameters of Si, SiO_2 and Corning glass are well documented in references. However, thermal conductivity of poly-Si thin film is still a research topic, and it can depend on some specific thin film parameters such as grain size, shape and doping concentration [7,8]. For MILC poly-Si, no such data have yet been reported. By comparing the simulation results using different thermal conductivity data for heavily doped poly-Si [7,8], it is found that variation in the channel temperature is limited to $< 2°C$. For most applications of poly-Si TFTs, the single device simulation model used in this study is suitable. However, it should be emphasized that the single device model would underestimate the actual channel temperature when TFTs simultaneously operated under SH conditions are closely neighbored.

7 Conclusions

Channel temperature distribution of poly-Si TFTs under SH stress has the following features:

1) The high temperature region is offset to the drain side along the channel length direction while located in mid-channel width.

2) The high temperature region is more expanded in the device with larger W when stress power density is the same, and thus the channel temperature rise is lower when the device W/L is smaller.

3) Under SH, most heat dissipates through the bottom substrate for device on silicon wafer and through the channel upper surface for device on glass. Highly thermal conductive substrate can dramatically reduce the channel temperature rise.

4) Rising/falling device temperature is a transient process, with its time constant linearly increasing with the device width.

To reduce the SH effect, possible measures include: decreasing device power density under operation, using a high thermal conductivity substrate material, and using a small W/L device. For device on glass substrate, improving upper surface heat dissipation is very important. Steady and transient state simulation of channel temperature distribution also helps in investigating the mechanism of SH degradation.

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