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RESEARCH ARTICLE

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Two-dimensional subthreshold current model for dual-material gate SOI nMOSFETs with single halo

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Abstract A two-dimensional (2D) model for the subthreshold current in the dual-material gate (DMG) silicon-on-insulator (SOI) MOSFET with a single halo is presented. The model considers single halo doping in the channel near the source and a dual-material gate to derive the channel potential using the explicit solution of the 2D Poisson's equation. Together with the conventional drift-diffusion theory, this results in the development of a subthreshold current model for the novel structure. Model verification is carried out using the 2D device simulator ISE. Excellent agreement is obtained between the calculations and the simulated results of the model.

Keywords dual-material gate (DMG), silicon-on-insulator (SOI), electron mobility

1 Introduction

To keep pace with progress in process technology, CMOS devices have been scaled down, continuously pushing the MOS technology into the nanometer era. However, with the reduction of channel length, some effects such as short-channel effects (SCEs), drain-induced barrier lowering (DIBL) and hot carrier effect (HCE) are becoming increasingly important, since they degrade controllability of the gate voltage over a drain current because of increased charge-sharing from the drain/source regions. Dual-material gate (DMG) silicon-on-insulator (SOI) MOSFETs in Refs. [1–4] seem to be a very promising option for ultimate scaling of CMOS technology because of their excellent SCE suppression and high carrier transport efficiency. However, DMG SOI MOSFETs show considerable DIBL in the sub-100 nm regime. Boron pocket implantation has been reported to effectively improve MOSFET performance in Refs. [5–7]. In the past years, the reverse SCEs (RSCEs) of boron pocket-implanted MOSFETs have been extensively studied from an experimental or analytical approach. Single-halo MOSFET structures have been introduced for bulk substrates in Ref. [8] as well as SOI MOSFETs in Ref. [9] to adjust threshold voltage. Most of them focus on the threshold voltage behavior and driving capability in Ref. [10–12]. With the device scaling down and the integration increasing, power consumption seems to be the challenge of very-large-scale integration (VLSI) devices. Therefore, the characteristics in the subthreshold region limit the development of devices.

In this article, the structure of a DMG SOI MOSFET with a single halo (DMGH) is investigated and a subthreshold potential for the novel device is developed. Based on an explicit solution to the channel potential, the subthreshold current can be modeled using the drift-diffusion equation. The model development of subthreshold current is described in detail. Model verification is carried out and presented using the results from 2D device simulator ISE.

2 Modeling description

2.1 2D surface potential

A cross-sectional view of a fully depleted DMG SOI MOSFET with a single halo (DMGH) is shown in Fig. 1(a). For comparison, the conventional DMG SOI MOSFET is shown in Fig. 1(b). The doping concentration N_A near the source region is higher than N_B elsewhere in the channel. Neglecting the influence of fixed oxide charges on the electrostatics of the channel, the potential distribution in the silicon film before the onset of strong inversion can be written as

$$\frac{\partial^2 \phi_i(x, y)}{\partial x^2} + \frac{\partial^2 \phi_i(x, y)}{\partial y^2} = \frac{qN_i}{\varepsilon_{Si}},$$

$$L_{i-1} \leqslant x \leqslant L_i,\ 0 \leqslant y \leqslant t_{Si},\ i = 1, 2, 3, \tag{1}$$

where ε_{Si} is the dielectric constant of silicon film, t_{Si} is the

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film thickness, L is the device channel length, and N_i is the channel doping concentration, $N_1 = N_A$, $N_2 = N_3 = N_B$.

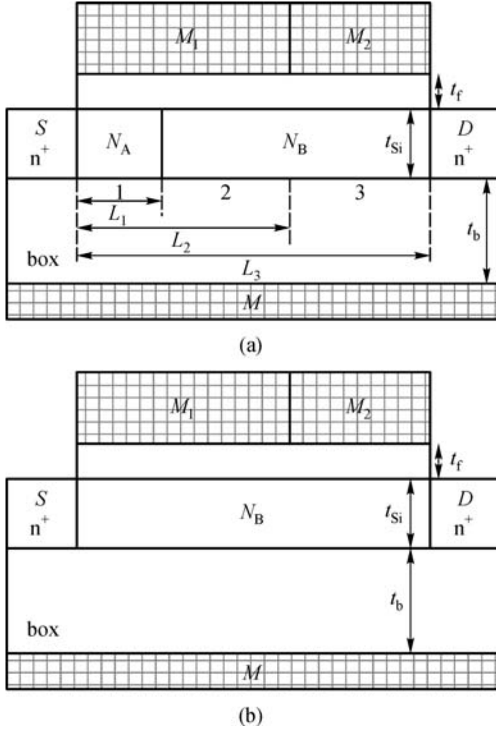

Fig. 1 Schematic structure of (a) DMG SOI MOSFET with single halo (DMGH) and (b) conventional DMG SOI MOSFET

The potential profile in the vertical direction, i.e., the y-dependence of $\phi_i(x, y)$, can be approximated by a simple parabolic function as proposed by Young in Ref. [3] for fully depleted SOI MOSFETs:

$$\phi_i(x, y) = \phi_{Si}(x) + c_{i1}(x)y + c_{i2}(x)y^2,$$

$$L_{i-1} \leqslant x \leqslant L_i,\ 0 \leqslant y \leqslant t_{Si},\ i = 1, 2, 3, \quad (2)$$

where $\phi_{Si}(x)$ is the surface potential and the arbitrary coefficients $c_{i1}(x)$ and $c_{i2}(x)$ are just functions of x.

Considering the gate and doping profile, the channel can be divided into three zones. Therefore, the flat band voltage for the three zones would be different, which are given as

$$V_{FBi} = \phi_{MSi} = \phi_{Mi} - \phi_{Sii},$$

$$L_{i-1} \leqslant x \leqslant L_i,\ 0 \leqslant y \leqslant t_{Si},\ i = 1, 2, 3, \quad (3)$$

where ϕ_{Mi}, ϕ_{Sii} are the metal work functions and the silicon work functions, respectively.

The semiconductor work function can be written as

$$\phi_{Sii} = \chi_{Si} + \frac{E_g}{2q} + \phi_{Fi}, \quad (4)$$

where $\phi_{Fi} = V_t \ln(N_i/n_i)$ is the Fermi potential, E_g is the silicon bandgap, χ_{Si} is the electron affinity, V_t is the thermal voltage, and n_i is the intrinsic carrier concentration.

The Poisson's equation is solved separately using the following boundary conditions:

1) Electric flux at the gate/front-oxide interface and the buried oxide/back channel interface is continuous for the three zones:

$$\left.\frac{d\phi_i(x, y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\phi_{Si}(x) - V'_{gsi}}{t_f},$$

$$\left.\frac{d\phi_i(x, y)}{dy}\right|_{y=t_{Si}} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{V'_{bsi} - \phi_{Bi}(x)}{t_b},$$

$$L_{i-1} \leqslant x \leqslant L_i,\ i = 1, 2, 3,\ 0 \leqslant y \leqslant t_{Si}, \quad (5)$$

where ε_{ox} is the dielectric constant of the oxide; t_f, t_b are the gate oxide and buried oxide thickness respectively; $V'_{gsi} = V_{gs} - V_{FB,fi}$, $i = 1, 2, 3$, where V_{gs} is the gate-to-source voltage; $\phi_{Bi}(x)$, $i = 1, 2, 3$ is the potential function along the back oxide-silicon interface; $V'_{bsi} = V_{bs} - V_{FB,bi}$, $i = 1, 2, 3$, where V_{bs} is the substrate bias; $V_{FB,fi}$, $V_{FB,bi}$, $i =$ 1,2,3 are the front- and back-channel flat band voltages, respectively.

2) The surface potential and electric flux at the interface of the three zones are continuous and shown as follows:

$$\phi_1(L_1, 0) = \phi_2(L_1, 0),\ \phi_2(L_2, 0) = \phi_3(L_2, 0),$$

$$\left.\frac{d\phi_1(x, y)}{dx}\right|_{x=L_1} = \left.\frac{d\phi_2(x, y)}{dx}\right|_{x=L_1},$$

$$\left.\frac{d\phi_2(x, y)}{dx}\right|_{x=L_2} = \left.\frac{d\phi_3(x, y)}{dx}\right|_{x=L_2}. \quad (6)$$

3) The potentials at the source and drain end are as follows:

$$\phi_1(0, 0) = \phi_{S1}(0) = V_{bi},$$

$$\phi_3(L, 0) = \phi_{S3}(L) = V_{bi} + V_{ds}, \quad (7)$$

where $V_{bi} = (E_g/2) + V_t \ln(N_A/n_i)$ is the built-in potential across the body-source junction.

The constants in Eq. (2) can be derived from the above boundary conditions. Substituting Eq. (2) into Eq. (1), we can obtain

$$\frac{d^2\phi_{Si}(x)}{dx^2} - \alpha^2 \phi_{Si}(x) = \beta_i,\ L_{i-1} \leqslant x \leqslant L_i,\ i = 1, 2, 3. \quad (8)$$

Here,

$$\alpha^2 = \frac{2(C_b C_{Si} + C_f C_{Si} + C_b C_f)}{t_{Si}^2 C_{Si}(2C_{Si} + C_b)},$$

$$\beta_i = \frac{qN_i}{\varepsilon_{\text{Si}}} - 2V'_{\text{gs}i}\frac{C_{\text{f}}(C_{\text{Si}} + C_{\text{b}})}{t_{\text{Si}}^2 C_{\text{Si}}(2C_{\text{Si}} + C_{\text{b}})} - 2V'_{\text{bs}i}\frac{C_{\text{b}}}{t_{\text{Si}}^2(2C_{\text{Si}} + C_{\text{b}})}, \ i = 1,2,3,$$

where $C_{\text{Si}} = \varepsilon_{\text{Si}}/t_{\text{Si}}$, $C_{\text{f}} = \varepsilon_{\text{ox}}/t_{\text{f}}$, $C_{\text{b}} = \varepsilon_{\text{ox}}/t_{\text{b}}$.

The above equations are simple second-order differential equations with constant coefficients, and thus the expression for the surface potential is of the form:

$$\phi_{\text{S}i}(x) = A_i\exp(\alpha x) + B_i\exp(-\alpha x) - \sigma_i, \quad i = 1,2,3, \tag{9}$$

where $\sigma_j = \beta_j/\alpha^2$, $j = 1,2,3$.

By using boundary conditions (5)–(7) to solve the constants in Eq. (8), the constants are

$$A_1 = \frac{(V_{\text{b}i} + V_{\text{ds}} + \sigma_3) - (V_{\text{b}i} + \sigma_1)\exp(-\alpha L) + V_{\text{SL}}}{2\sinh(\alpha L)},$$

$$B_1 = \frac{(V_{\text{b}i} + \sigma_1)\exp(\alpha L) - (V_{\text{b}i} + V_{\text{ds}} + \sigma_3) - V_{\text{SL}}}{2\sinh(\alpha L)},$$

$$A_i = A_{i-1} - \exp(-\alpha L_{i-1})(\sigma_{i-1} - \sigma_i)/2, \quad i = 2,3,$$

$$B_i = B_{i-1} - \exp(\alpha L_{i-1})(\sigma_{i-1} - \sigma_i)/2, \quad i = 2,3,$$

where

$$V_{\text{SL}} = (\sigma_1 - \sigma_2)\cosh(\alpha(L - L_1)) + (\sigma_2 - \sigma_3)\cosh(\alpha(L - L_2)).$$

2.2 2D subthreshold current model

Based on the drift-diffusion equation, the electron current density J_n in an nMOSFET can be written as

$$J_n = q\left(-n(x)\mu_n\frac{\text{d}\phi_{\text{S}}(x)}{\text{d}x} + D_n\frac{\text{d}n(x)}{\text{d}x}\right) = qD_n\left(-\frac{n(x)}{V_{\text{t}}}\frac{\text{d}\phi_{\text{S}}(x)}{\text{d}x} + \frac{\text{d}n(x)}{\text{d}x}\right), \tag{10}$$

where $n(x)$ is the electron density along the channel, and D_n is the electron diffusion coefficient, which can be related to the thermal voltage V_{t} and electron mobility μ_n through the Einstein relation as $D_n = V_{\text{t}}\mu_n$.

By multiplying Eq. (10) by an integrating factor of $\exp(-\phi_{\text{S}i}(x)/V_{\text{t}})$, the right side of the equation can be transformed into an exact derivative. Considering the boundary condition (7) and different doping concentrations in the channel, the current density can be expressed as

$$J_n = qD_n\exp\left(-\frac{V_{\text{b}i}}{V_{\text{t}}}\right)\frac{N_{\text{A}} - N_{\text{B}}\exp\left(-\frac{V_{\text{ds}}}{V_{\text{t}}}\right)}{\int_0^L\exp\left(-\frac{\phi_{\text{S}i}(x)}{V_{\text{t}}}\right)\text{d}x}. \tag{11}$$

The drain current I_{ds} in the channel is obtained by integrating the current density over the cross section of the conducting channel, which yields

$$I_{\text{sub}} = J_n W S_{\text{eff}}, \tag{12}$$

where W is the device channel width and S_{eff} is the effective channel thickness, which can be estimated as the distance from the surface to the position when the electrostatic potential has changed by V_{t}. According to the Gauss' law, the vertical component of the electric field at the surface $V_{\text{t}}/S_{\text{eff}}$, is equal to $Q_{\text{dep}}/\varepsilon_{\text{Si}}$ (Q_{dep} is the depletion charge) in the subthreshold region. Thus,

$$S_{\text{eff}} = V_{\text{t}}\sqrt{\frac{\varepsilon_{\text{Si}}}{2qN_{\text{CH}}\phi'_{\text{S}i}}}, \tag{13}$$

where $\phi'_{\text{S}i} = 2\phi_{\text{F}i}$ is the surface potential at the onset of strong inversion.

In the structure of a DMGH SOI MOSFET, since the channel is divided into three parts, the subthreshold current in the channel can be solved iteratively. According to Eq. (9), a complicated process is needed to calculate the denominator in Eq. (11). To come up with an analytical solution for Eq. (11), we propose to approximate $\phi_{\text{S}i}(x)$ as a piecewise linear function in the channel. From this, $\phi_{\text{S}i}(x)$ in Eq. (9) can be unified and rewritten as

$$\phi_{\text{S}i}(x) = \frac{\phi_{\text{S},m} - \phi_{\text{S},m-1}}{x_m - x_{m-1}}x + \frac{\phi_{\text{S},m-1}x_m - \phi_{\text{S},m}x_{m-1}}{x_m - x_{m-1}}. \tag{14}$$

Thus, the denominator in Eq. (11) is reduced to

$$\int_0^L\exp\left(-\frac{\phi_{\text{S}i}(x)}{V_{\text{t}}}\right)\text{d}x = \sum_{m=1}^{N}\frac{V_{\text{t}}\Delta x}{\phi_{\text{S},m} - \phi_{\text{S},m-1}}\exp\left(-\frac{\phi_{\text{S},m-1}}{V_{\text{t}}}\right) \times \left[1 - \exp\left(-\frac{\phi_{\text{S},m} - \phi_{\text{S},m-1}}{V_{\text{t}}}\right)\right], \tag{15}$$

where $\phi_{\text{S},m}$ is $\phi_{\text{S}}(x)$ at $x = m\Delta x$, $\Delta x = x_m - x_{m-1} = L/N$.

Applying this analytical method to Eq. (12), the subthreshold current density can be calculated.

3 Results and discussion

To verify the proposed analytical model, the 2D device simulator ISE was used to evaluate the results from the present model. For DMGH, typical values of the work function for gate metals M_1 and M_2 are chosen as 4.77 and 4.10 eV, respectively. The doping concentration close to the source is $N_{\text{A}} = 4\times10^{17}\ \text{cm}^{-3}$, the rest in the channel is $N_{\text{B}} = 1\times10^{17}\ \text{cm}^{-3}$, and the drain and source doping concentration is $N_{\text{D}} = 1\times10^{20}\ \text{cm}^{-3}$. The thicknesses of the front oxide, silicon film and buried oxide are 2, 12 and 200 nm respectively. The work function of the buried gate

is equal to that of M_1. The electron mobility in the channel μ_n is assumed as $500\ \mathrm{cm^2/(V \cdot s)}$.

The position-dependent potentials in the channel calculated from the present model are illustrated in Fig. 2 for DMGH SOI with two different channel lengths ($L = 50$ and 100 nm) and various drain biases. It is seen from Fig. 2 that a potential step profile exists near the interface of different gates. Because of step potential, when beyond 0.1 V drain bias, the additional drain voltage increase is not absorbed under the M_1 but under the M_2. In other words, the M_1 region is screened from the drain potential variations. Consequently, V_{ds} has a very small influence on M_1, even for the 50 nm channel length. The novel structure can suppress the SCEs as a result of the screening effect. Moreover, an extra potential step exists near the halo boundary besides the one near the interface between the two gates, which further suppresses the DIBL.

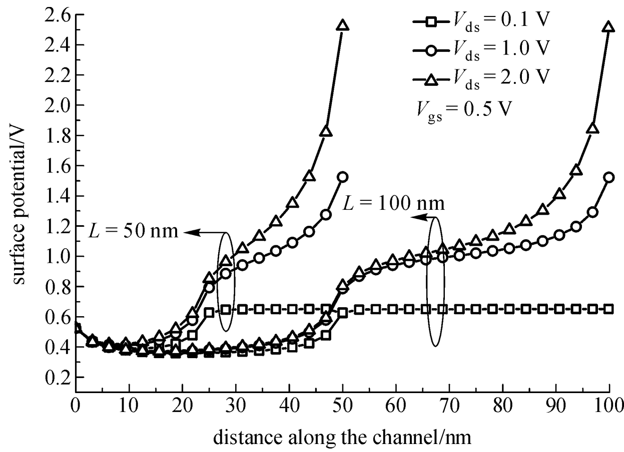

Fig. 2 Calculated channel potential for DMGH with two different channel lengths and various drain voltages

Figure 3 shows the subthreshold current characteristics of DMGH SOI NMOSFETs for different channel lengths and various drain voltages respectively. The symbols represent the calculation results using the exact channel potential; the dotted lines denote the calculated results using the piecewise-approximated channel potential. It is found that the analytical and exact results agree very well with each other, thus validating the analytical approach. Note that the subthreshold current increases with the reduced channel length, i.e., the shorter the channel length, the larger the subthreshold current at a given gate voltage will be. For a given gate bias, the subthreshold current differences with various drain biases increase with decreasing channel length because of a more significant DIBL effect in a shorter channel MOS device. For comparison, the subthreshold current for the conventional DMG SOI MOSFET is also given. It is found that the introduction of a single halo can significantly degrade the off-state current. Since the analytical approach with Eq. (15) is valid, it is used in the following discussions.

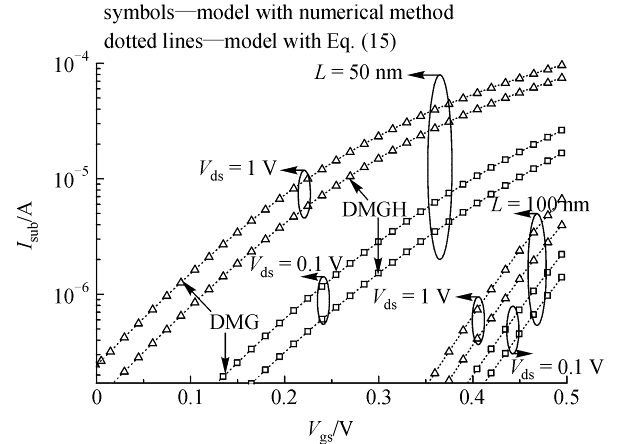

Fig. 3 Calculated I_{sub}-V_{gs} characteristics using exact and analytical approaches for two different channel lengths and various drain voltages

It is shown in Fig. 4 that subthreshold current-voltage characteristics with various work function differences between two gate materials. In Fig. 4, the symbols and solid lines represent the model calculations using the piecewise-approximated channel potentials and simulated results from 2D device simulator ISE. A very good agreement is found between the model predictions and simulated results. With the work function difference increasing, the subthreshold current decreases rapidly.

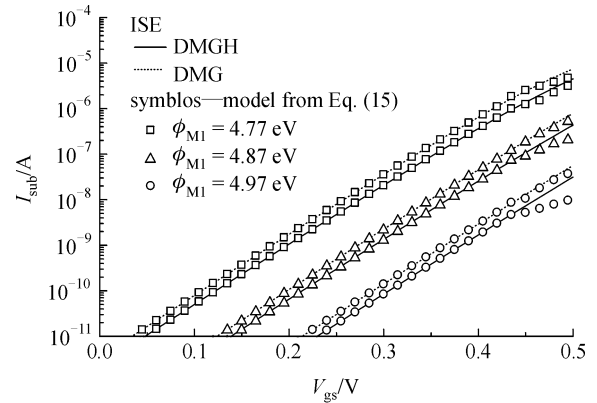

Fig. 4 Variation of I_{sub} characteristics with work function difference at $V_{ds} = 1$ V

The subthreshold current-voltage curves for three different halo dopings are illustrated in Fig. 5. It can be seen that the subthreshold current is reduced with increasing halo implant doping. A very good agreement is found between the model prediction using the piecewise-approximated channel potentials and simulated results from ISE for the sub-threshold region; beyond this region, however, the model is not valid and a large discrepancy between the model and simulations is observed.

Figure 6 shows the variation of subthreshold character-

istics with the effective halo lateral length L_1 as shown in Fig. 1, with the lengths L_2 and L_3, kept constant. It can be seen from the figure that the subthreshold currents change monotonically with halo lengths, and that the longer the halo length is, the smaller the current at a given gate voltage will be. It can be seen from Fig. 7 that with the length of M_1 ('control gate') increasing, at the fixed channel length L_3, the threshold currents decrease. This happens because the threshold voltage is enhanced with the L_2 increase.

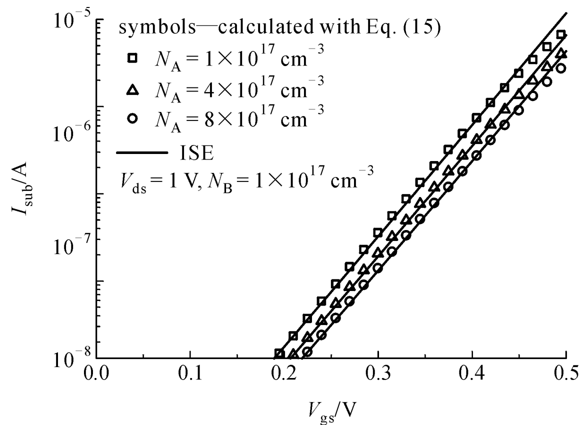

Fig. 5 Variation of I_{sub} characteristics with halo doping concentration at $V_{ds} = 1$ V

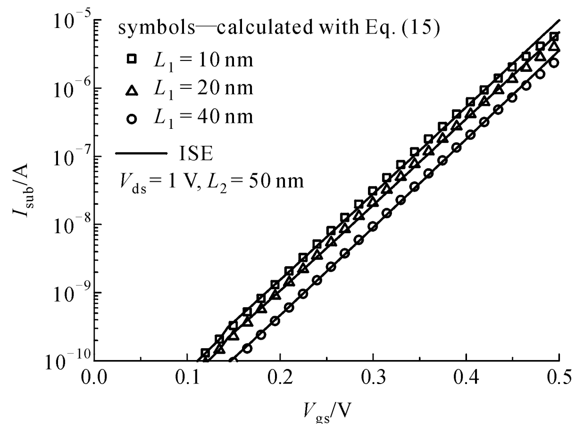

Fig. 6 I_{sub}-V_{gs} characteristics for different halo lengths with channel length fixed at $V_{ds} = 1$ V

4 Conclusions

An analytical subthreshold potential model for DMG SOI MOSFETs with a single halo is developed. Based on the potential profile, the subthreshold current model is derived with the conventional drift-diffusion theory. To simplify the calculation process for subthreshold current, an analytical method with piecewise-approximated channel potentials is proposed. An excellent agreement is found between the model predictions using both exact and piecewise-approximated channel potentials. The present model is useful for evaluating the subthreshold current for a novel MOS technology. Again, a good agreement is obtained between the model prediction results and simulated results from 2-dimensional device simulator ISE.

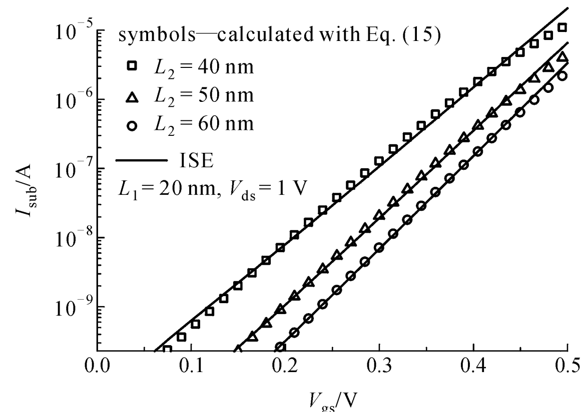

Fig. 7 I_{sub}-V_{gs} characteristics with various lengths of M_1 for channel length fixed at $V_{ds} = 1$ V

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