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RESEARCH ARTICLE

Weilian GUO, Huilai LIANG, Ruiliang SONG, Shilin ZHANG, Luhong MAO, Liuchang HU, Jianheng LI, Haitao QI, Zhen FENG, Guoping TIAN, Yuehui SHANG, Yongqiang LIU, Yali LI, Mingwen YUAN, Xiaobai LI

The design and fabrication on gate type resonant tunneling transistor

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Abstract In light of fabricating resonant tunneling diode (RTD), in this paper a GaAs-based resonant tunneling transistor with gate structure (GRTT) has been designed and fabricated successfully. A systematic depiction centers on the designs of material structure, device structure, photolithography mask, fabrication of device and the measurement and analysis of parameters. The fabricated GRTT has a maximum PVCR of 46 and a maximum transconductance of 8 mS. The work lays the foundation for further improvement on the performance and parameters of RTT.

Keywords resonant tunneling transistor (RTT), gate controlled device, GaAs based quantum device

1 Introduction

Resonant tunneling diode (RTD), despite being of high working frequency, high speed, bistable and self-latching [1], brings inconvenience to circuit design since there is no gain, low fanout or current drive capacity, uncontrollability on *I–V* characteristics, nor isolation between input and output circuit. While resonant tunneling transistor (RTT) with three terminals can overcome the weakness above. Although the frequency of RTT is not as high as that of RTD, it can reach more than ten GHz, which can be applied in the microwave circuit and high speed digital IC.

RTT can be defined as a resonant tunnel device with double barrier structure (DBS) and three terminals. It falls into two kinds: one is gate RTT, whose *I–V* characteristics can be controlled by the third terminal – gate terminal based on the RTD structure [2,3] and the other is compound RTT, whose DBS structure is combined with another high frequency three terminals device, such as HEMT [4], MESFET [5], HBT [6].

The gate RTT can be divided into Schottky gate structure and p-n junction gate structure. This paper focuses primarily on the Schottky gate RTT, and the design of the material, the structure and the layout. GaAs RTT devices are fabricated through two batches of fabrication with the gate-controlling capacity on the resonant current. As measured, the transconductance reaches 1.3–8 mS. Although this parameter is not high enough, it will be improved in the future research.

2 Material structure design

The material parameter of RTT is shown in Table 1. The material of RTT is similar to that of RTD since the gate structure of gate RTT is mainly realized by the device

Table 1 Material structure of Schottky gate RTT

thickness/nm	material	doping/cm^{-3}	layer
500	n^+-GaAs	2×10^{19}	top contact
50	n^--GaAs	2×10^{17}	emitter
100	n^--GaAs	5×10^{16}	
5	i-GaAs	undoped	spacer
5	i-$In_{0.17}Ga_{0.83}As$	undoped	sub-well
0.5	i-GaAs	undoped	spacer
1.7	i-AlAs	undoped	barrier
5	i-$In_{0.17}Ga_{0.83}As$	undoped	well
1.7	i-AlAs	undoped	barrier
0.5	i-GaAs	undoped	spacer
5	i-$In_{0.17}Ga_{0.83}As$	undoped	sub-well
5	i-GaAs	undoped	spacer
100	n^--GaAs	5×10^{16}	collector
50	n^--GaAs	2×10^{17}	
500	n^+-GaAs	2×10^{19}	bottom contact
SI GaAs–substrate (100)			

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Weilian GUO (✉), Huilai LIANG, Ruiliang SONG, Shilin ZHANG, Luhong MAO, Liuchang HU, Jianheng LI, Haitao QI
School of Electronic Information Engineering, Tianjin University, Tianjin 300072, China
E-mail: w.l.guo@eyou.com

Weilian GUO, Zhen FENG, Guoping TIAN, Yuehui SHANG, Yongqiang LIU, Yali LI, Mingwen YUAN, Xiaobai LI
13th Institute of CETC, Shijiazhuang 050051, China

structure and technology. The top and bottom layers with a heavy doping of Si are designed for achieving low resistance and conducting non-alloying technology. For the purpose of improving the I–V characteristic, $In_{0.17}Ga_{0.83}As$ sub-well is added to realize 2D-2D resonant tunneling. $In_{0.17}Ga_{0.83}As$ is chosen in place of GaAs as the material of main well in that its ground energy level is lower than the latter, which is conducive to reducing V_T and V_P. Other material layers are similar to the conventional RTD and it will not be explained here in detail.

3 Device structure design

3.1 Device structure and working theory

In order to enhance the Schottky gate controlling capacity on resonant current, two structures are chosen as described in Figs. 1(a) and 1(b): the groove gate structure and the self-aligned gate structure. In Fig. 1(a), the groove gate device structure is based on the technology that a groove is etched from the gate mesa to the DBS region, and then Schottky gate metal is deposited on the groove, making the depletion region expand over the DBS region. The lateral expansion of the depletion layer controls the current as a result of reducing the cross section area of vertical current channel when applying reverse voltage on the gate. In Fig. 1(b), the self-aligned gate structure is based on the technology that gate metal is deposited on the gate mesa near the DBS region under the shelter of emitter metal (AuGeNi) edge by self-aligned electron beam evaporation technology. In order to control the resonant current effectively, the self-aligned gate metal is made near the vertical side of emitter mesa to narrow the current channel cross section area, which is left by depletion region produced by the reverse gate voltage. The function of the two gate structures can be described as follows [3]:

$$d=\sqrt{\frac{2\varepsilon\varepsilon_0(V_D-V_G)}{qN_d}}, \tag{1}$$

$$S=w\left(L_{gg}-2d\right). \tag{2}$$

In Eqs. (1) and (2), V_G is gate voltage, d is the horizontal width of depletion region, V_D is the voltage of Schottky barrier, ε_0 is the permittivity of vacuum, ε is the permittivity of GaAs, q is the electronic charge, N_d is n^- doping concentration, L_{gg} is the distance between two gates. w is the thickness of the source terminal on the oriental perpendicular to the paper of the device, S is the cross section area of vertical current channel.

3.2 Device structure design

Based on the gate RTT structures above, two structures are devised: the groove gate structure and the self-aligned gate structure.

1) Groove gate structure: the metal of emitter and gate is designed in finger-like shape to enhance the gate controlling capacity effectively on the resonant current and increase the coupling degree between DBS region and gate.

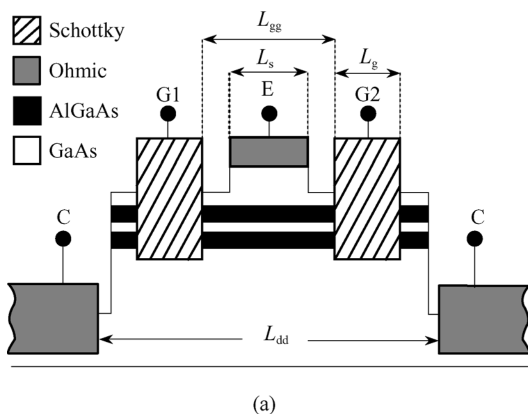
2) Self-aligned gate structure: gate metal is designed around the emitter mesa that is located near the DBS gate mesa.

3) Collector metal is designed as a closed rectangular frame around the whole device for both of above two structures to enhance the collecting effect of resonant current.

4 Layout design

4.1 Groove gate RTT layout

Figure 2 displays the layout of the groove gate RTT, where in Fig. 2(a) shows the whole RTT, Fig. 2(b) demonstrates part of the device. The emitter width is 3 μm and the gate width is 2 μm, between which the distance is 2 μm. The whole area of the emitter is 288.5 μm^2.



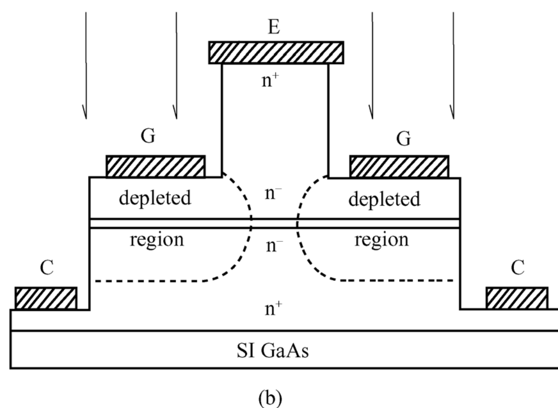


Fig. 1 Two different gate structures of RTT. (a) Groove gate RTT; (b) self-aligned gate RTT

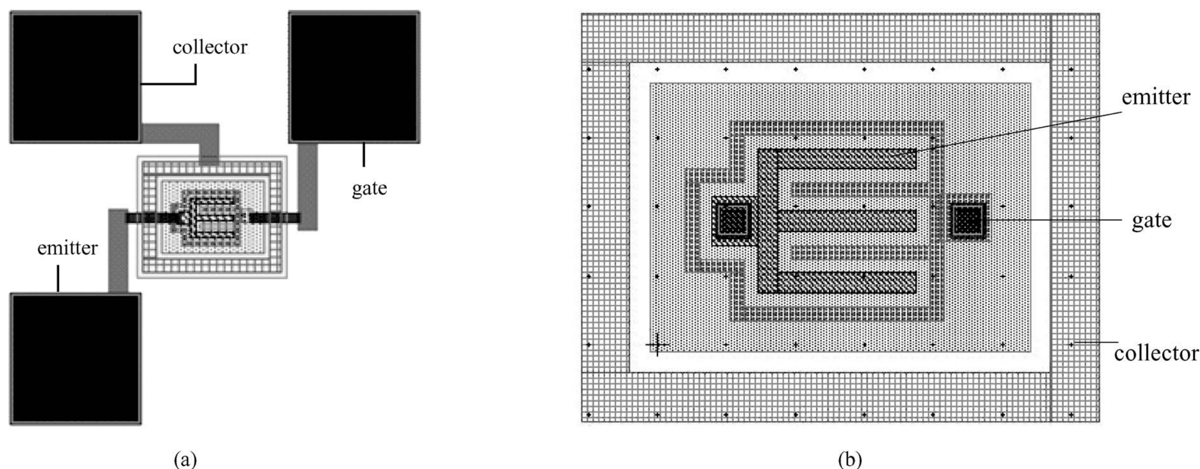


Fig. 2 Mask of groove gate RTT. (a) Mask shape of whole RTT; (b) mask shape of part of the device

4.2 Layout of self-aligned gate RTT

In Fig. 3, the emitter is designed in two different areas: 8 μm × 8 μm (upper emitter), 5 μm × 5 μm (lower emitter), the area of the gate is 570 μm^2.

5 Fabrication of device

The specific fabrication process consists of the following steps: cleaning → emitter photolithograph → sputtering emitter metal → lift-off emitter metal → gate mesa etching → etching groove → evaporating gate Schottky barrier metal → lift-off gate metal → collector photolithograph → sputtering collector metal → lift-off collector metal → big mesa photolithograph provided by photoresist → big mesa etching → Si_3N_4 grown by PECVD → pad photolithograph → pad etching → sputter interconnection metal → lift-off metal → rapid thermal annealing → bonding and packaging.

6 Parameter measurement and analysis

6.1 Groove gate RTT

6.1.1 *I–V* Characteristics of device

Groove gate RTT has been measured by XJ4810 type curve tracer. The *I–V* characteristics on different gate voltages are shown in Fig. 4.

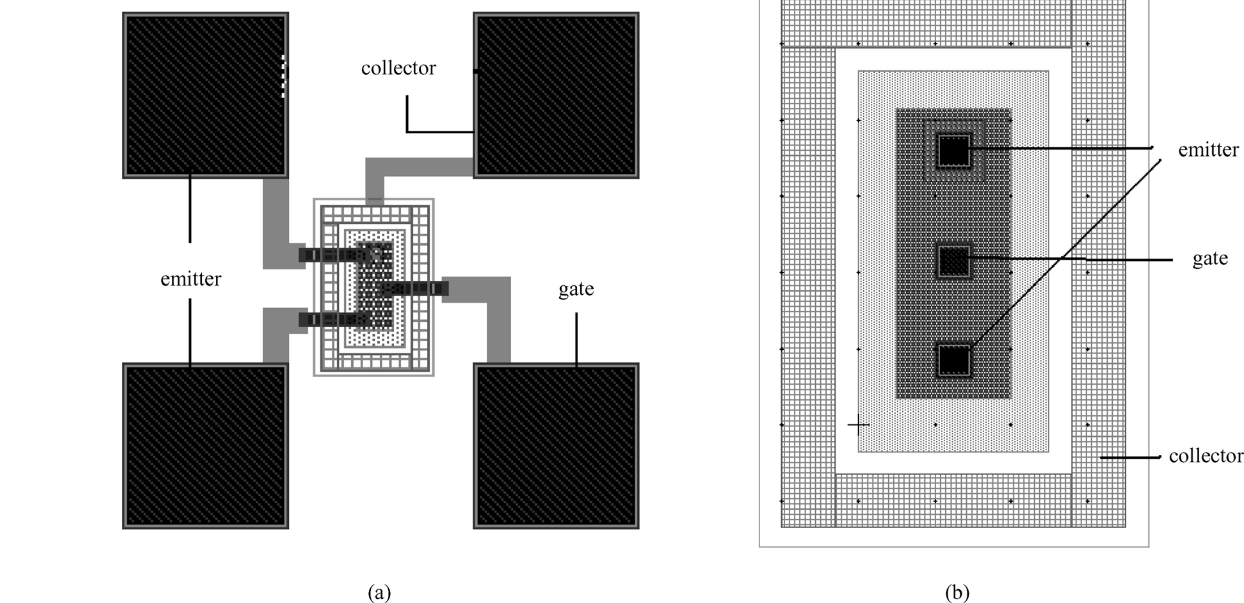
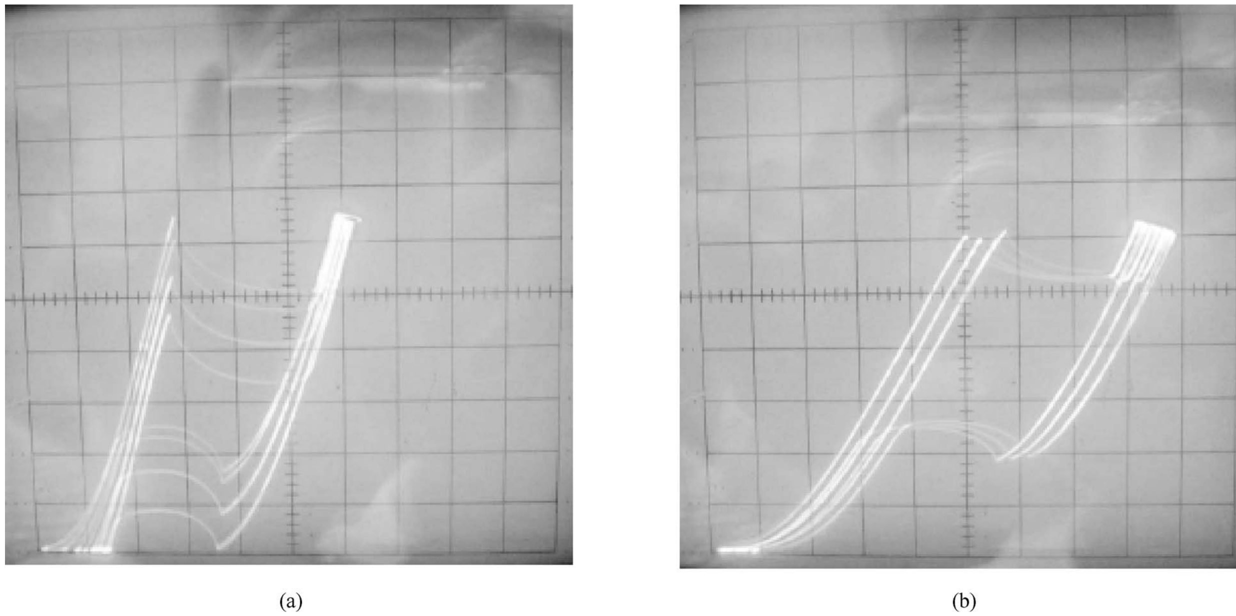


Fig. 3 Mask of the self-aligned gate RTT. (a) Mask shape of the whole RTT; (b) mask shape of part of the device



(a) (b)

Fig. 4 *I–V* characteristics of the groove gate RTT (taking gate voltage as a parameter). (a) Top terminal grounding (*x*: 0.2 V/div, *y*: 5 mA/div, step: 0.5 V); (b) bottom terminal grounding (*x*: 0.2 V/div, *y*: 10 mA/div, step: 1 V)

6.1.2 DC parameter of device

From the *I–V* characteristics above, DC parameters versus gate voltage V_G is depicted in Table 2 (top terminal is grounded) and Table 3 (bottom terminal is grounded). From Table 2, the average transconductance $\Delta I_P/\Delta V_G$ is estimated as 5–8 mS when the top terminal is grounded.

Table 2 DC parameters of groove gate RTT when the top terminal is grounded as gate voltage

V_G/V	I_P/mA	I_V/mA	V_P/V	V_V/V	V_T/V	R_N/Ω	PVCR	PVVR	J_P/ kA·cm^{-2}
0	32.5	8.5	0.58	0.74	0.065	−6.66	3.82	0.78	11.26
−0.5	30.5	7.5	0.58	0.74	0.16	−6.95	4.07	0.78	10.57
−1.0	27.0	4.0	0.57	0.72	0.24	−6.52	6.75	0.79	9.36
−1.5	23.0	0.5	0.56	0.71	0.28	−6.66	46.0	0.79	7.97

Table 3 DC parameters of groove gate RTT when the bottom terminal is grounded as gate voltage

V_G/V	I_P/mA	I_V/mA	V_P/V	V_V/V	V_T/V	R_N/Ω	PVCR	PVVR	J_P/ kA·cm^{-2}
0	60	19	1.0	1.11	0.04	−2.68	3.16	0.90	20.79
−1	60	19	1.06	1.15	0.10	−2.19	3.16	0.92	20.79
−2	61	20	1.16	1.23	0.16	−1.70	3.05	0.94	21.14

6.1.3 The characteristics of RTT device parameters for different gate voltages

The relation of the DC parameter of the groove RTT is shown in the data of the tables above, while gate voltage is indicated in Fig. 5 when the top terminal is grounded, and Fig. 6 displays the relation when the bottom terminal is grounded.

6.1.4 *I–V* characteristics of groove gate RTT and DC parameters varying with V_G voltages

1) When the top terminal is grounded.

a) I_P and I_V vary obviously with V_G. The quantity of $\Delta I_P/\Delta V_G$ and $\Delta I_V/\Delta V_G$ are large, I_P and I_V become smaller with lower V_G (negative value).

b) V_P and V_V change weakly with V_G. With higher V_G, V_P moves towards right slightly. V_V seems to be constant.

c) With bigger absolute value of V_G and smaller value of I_V, PVCR becomes higher obviously; as $V_G = 1.5$ V, PVCR = 46, V_G and PVCR go beyond that of RTD.

d) With higher V_G, V_T turns smaller. R_N and PVVR are invariable.

2) When the bottom terminal is grounded.

a) I_P and I_V change slightly with V_G. The absolute value of I_P is higher than that when the top terminal is grounded.

b) Though the amplitude of V_P and V_V do not change greatly with V_G, while it is apparent. When the absolute value of V_G grows bigger, V_P and V_V turn bigger simultaneously (it moves towards right on the voltage axis).

c) The R_N, PVCR and PVVR change slightly with V_G. The change of V_T is less obvious when the top terminal is grounded, while both in a similar tendency.

6.2 Self-aligned gate RTT

6.2.1 *I–V* characteristics of device

I–V characteristics of device is shown in Fig. 7.

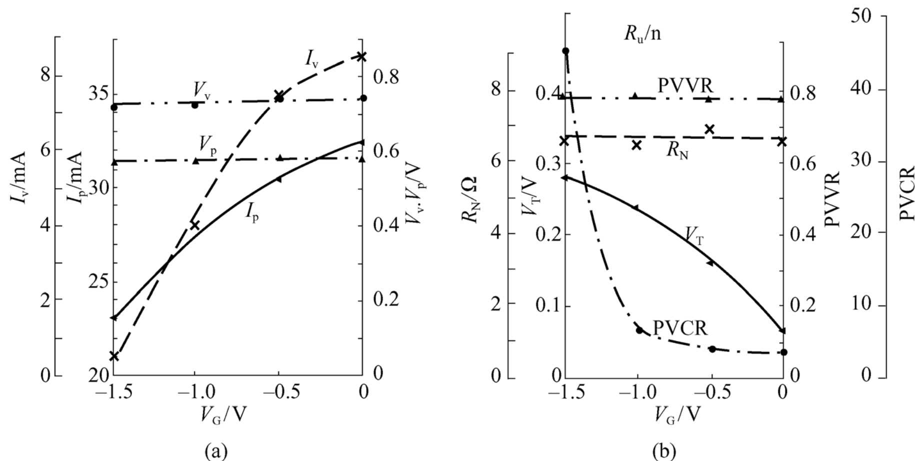


Fig. 5 I_P-, I_V-, V_P-, V_V-V_G characteristics and V_T-, R_N-, PVCR-, PVVR-V_G characteristics of groove gate RTT when the top terminal is grounded. (a) I_P-, I_V-, V_P-, V_V-V_G characteristics; (b) V_T-, R_N-, PVCR-, PVVR-V_G characteristics

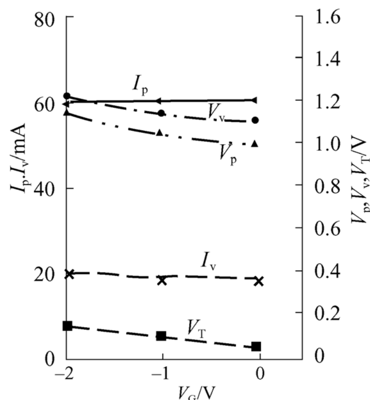


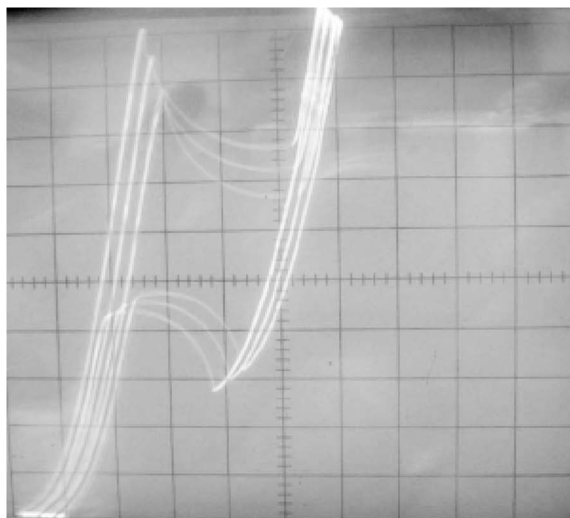
Fig. 6 I_P-, I_V-, V_P-, V_V-, V_T-V_G characteristics of groove gate RTT when the bottom terminal is grounded

6.2.2 DC parameters of device

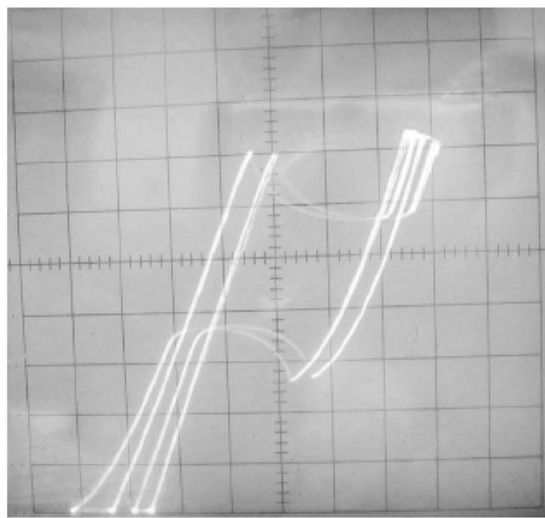
The DC parameters of the self-aligned gate RTT are demonstrated in Table 4 (top terminal is grounded) and Table 5 (bottom terminal is grounded).

6.2.3 The characteristics of RTT device parameters for different gate voltages

With reference to the data in Table 4, we can make out the trend of DC parameters of the self-aligned gate RTT with gate voltage when the top terminal is grounded, as shown in Fig. 8. The situation is similar between the groove gate RTT and the self-aligned gate RTT when the bottom terminal is grounded except that the V_T of the self-aligned gate RTT is larger, thus the characteristics is neglected in Fig. 8.



(a)



(b)

Fig. 7 I–V characteristics of the self-aligned gate RTT. (a) When the top terminal is grounded (x: 0.2 V/div, y: 2 mA/div, step: 1 V); (b) when the bottom terminal is grounded (x: 0.2 V/div y: 5 mA/div, step: 1 V)

Table 4 DC parameters of the self-aligned gate RTT when the top terminal is grounded serving as gate voltage

V_G/V	I_P/mA	I_V/mA	V_P/V	V_V/V	V_T/V	PVCR	PVVR	R_N/Ω	J_P/ kA·cm^{-2}
0	20.2	5.6	0.54	0.76	0.22	3.6	0.71	15	80.8
−0.5	19.0	6.0	0.56	0.82	0.28	3.16	0.683	20	76.0
−1.0	17.6	6.4	0.60	0.86	0.32	2.75	0.697	23.2	70.4

Table 5 DC parameters of the self-aligned gate RTT when the bottom terminal is grounded serving as gate voltage

V_G/V	I_P/mA	I_V/mA	V_P/V	V_V/V	V_T/V	PVCR	PVVR	R_N/Ω	J_P/ kA·cm^{-2}
0	35	13	0.92	1.04	0.40	2.69	0.88	5.45	140
−1	35	13	1.0	1.14	0.48	2.69	0.877	6.36	140

6.2.4 *I*–*V* characteristics of the self-aligned gate RTT and DC parameters varying with V_G voltages

1) When the top terminal is grounded

Comparing Figs. 4(a) and 7(a), or Tables 2 and 4, we can find that the self-aligned RTT and the groove gate RTT share in common in that I_P and I_V change with V_G more obviously than when the bottom terminal is grounded, i.e., $\Delta I_P/\Delta V_G$ and $\Delta I_V/\Delta V_G$ are higher. While their difference consists in the following two aspects:

a) There are some changes in V_P and V_V with the gate voltage of the self-aligned gate RTT.

b) The tendency of I_V changing with V_G is opposite to that of the PVCR, which means that the absolute value of V_G grows bigger, while I_V becomes higher and the PVCR goes lower.

2) When the bottom terminal is grounded

Comparing Figs. 4(a) and 7 (a) or Tables 2 and 4, V_T of the self-aligned gate RTT is higher than that of the groove gate RTT, while the other situations are more or less similar.

6.3 Analysis of the experimental results

The experimental results are complex, with plenty of phenomena not being reported before. Thus for simplicity, a preliminary analysis is given in this paper.

For either the groove gate RTT or the self-aligned gate RTT, the big difference as regards when the top terminal or the bottom terminal is grounded lies in that in the former case $\Delta I_P/\Delta V_G$ and $\Delta I_V/\Delta V_G$ are big, $\Delta V_P/\Delta V_G$ and $\Delta V_V/\Delta V_G$ are small, while for the latter $\Delta V_P/\Delta V_G$ and $\Delta V_V/\Delta V_G$ are big, $\Delta I_P/\Delta V_G$ and $\Delta I_V/\Delta V_G$ are small. The essential reason is that there is asymmetry on the device structure. Explanations are given as follows:

1) The area of the top terminal (self-aligned gate RTT) is small and the shape is finger-like (groove gate RTT), but the bottom electrode is of rectangle shape.

2) The gate mesa is made by shallow etching in the fabrication, and the real location is between DBS and top electrode.

Besides, the simulation of the device shows that when the gate electrode reverse voltage is applied and the bottom terminal is grounded, the depletion region extent in vertical current channel is more sever than that when the top terminal is grounded. Thus there is a large value of resistance in series when the bottom terminal is grounded under the reverse gate voltage. V_P and V_V move along the axis of voltage when resonant tunneling current drifts across the resistance and drops, i.e., $\Delta V_P/\Delta V_G$ and $\Delta V_V/\Delta V_G$ are big. Conversely, when the top terminal is grounded, the channel region is depleted slightly and maintains the neutral charge channel; when the cross

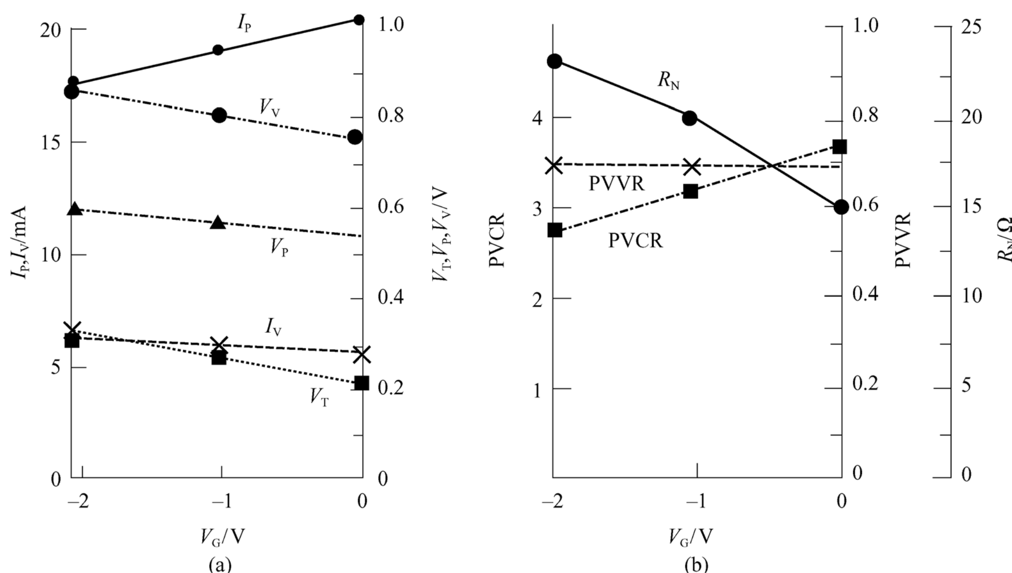


Fig. 8 I_P-, I_V-, V_P-, V_V-, V_T-V_G characteristics and R_N-, PVCR-, PVVR-V_G characteristics of self-aligned gate RTT when the top terminal is grounded. (a) I_P-, I_V-, V_P-, V_V-, V_T-V_G characteristics; (b) R_N-, PVCR-, PVVR-V_G characteristics

section area of neutral charge channel changes with gate voltage, I_P and I_V will change with it, i.e., $\Delta I_P/\Delta V_G$ and $\Delta I_V/\Delta V_G$ are big.

Furthermore, there still exist some problems with the high threshold voltage V_T in RTT with different gate styles, as shown on I–V characteristics. In particular, when with a high absolute value of V_G, V_T grows larger correspondingly, which jeopardizes the circuit design. This should be attributed to the existence of another current leaking channel between the emitter and the gate electrode. For instance, there is some metal left on the sidewall of the emitter mesa caused by lifting off the emitter metal non-thoroughly, which makes the current leaking channel between the emitter and gate come into being. These problems shall be studied and resolved in the further research.

7 Conclusions

This paper illustrates two structures of the RTT device (the groove gate structure and the self-aligned gate structure) generated by GaAs substrate. Material design, device structure design, layout design and fabrications are also explained. Based on the measurement, it is reported that the main DC parameters (I_P, V_P, PVCR) change with the gate voltage. The highest PVCR reaches 46. $\Delta I_P/\Delta V_G$ and $\Delta I_V/\Delta V_G$ are large when the top terminal is grounded, $\Delta V_P/\Delta V_G$ and $\Delta V_V/\Delta V_G$ are large when the bottom terminal is grounded. Based on experimental results, a preliminary explanation is given and the transconductance (G_m) of 1.3–1.8 mS is also estimated. There still exist some limitations in this research, for example, the threshold voltage is a little large and varies with V_G, shall be worked on in the further research.

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