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RESEARCH ARTICLE

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Effect of the silicon substrate structure on chip spiral inductor

Abstract In this paper, the effect of the substrate structure on the performance of the spiral inductor is investigated by the 3-D electromagnetic simulator, Ansoft high frequency structure simulator (HFSS). With variations in the substrate structure including substrate conductivity, permittivity and thickness of the dielectric layer, the performance of the inductors has been analyzed in detail. The simulation results and analyses indicate that the performance of the spiral inductor can be mostly improved by lowering the conductivity of the substrate, increasing the thickness of the dielectric layer and using the low K dielectric layer. In the mean time, some guidelines or ‘‘design rules’’ are summarized by the results of this study.

Keywords silicon, spiral inductor, quality factor, substrate structure

1 Introduction

Currently, planar spiral inductors have become essential elements of communication circuit blocks such as voltage controlled oscillators (VCOs), low-noise amplifiers (LNAs), mixers, and intermediate frequency filters (IFFs). To meet the need for greater portability, increased functionality, and lower costs of today's wireless communication systems, integrated planar spiral inductors with small form factors, high quality factor Q, and high self-resonant frequencies on silicon substrate are highly desired. At high frequency, substrate losses are an important limitation in achieving higher performance inductors on silicon. To improve inductor performance with bulk silicon, much reduced substrate losses have been demonstrated by using high-resistivity, silicon-on-insulator (SOI) [1,2], and micromachining techniques [3]. However, the optimization of the spiral is a never-ending job and there is still a great incentive to design and optimize spiral inductors fabricated on Si substrates.

In this paper, the spiral inductor is analyzed by using the 3-D simulator, Ansoft high frequency structure simulator (HFSS), to study the influence of the substrate structures on the inductors' performance in a multi-GHz frequency range. The spiral inductors with different substrate structures have been simulated and analyzed. Some guidelines or ‘‘design rules’’ are summarized by the results of this study.

2 Modeling of spiral inductors

The structure and physics model of spiral inductors are shown in Figs. 1 and 2. Figure 1 (a) is a simplified cross-sectional view of the spiral inductor. A top metal layer (M1) and interconnection metal layer (M2), separated by an insulator layer, form the feed line and spirals of the inductor. The simplified top view of the spiral inductor is shown in Fig.1 (b), where D is the outer diameter, ID is the inner diameter, S and W are spacing between traces and width of the metal trace, respectively.

The lumped physical model of a spiral inductor on silicon and the main parameters are illustrated in Fig. 2. Since an inductor is intended for storing magnetic energy only, the inevitable resistance and capacitance in a real inductor are counter-productive and thus are considered as parasitics. The inductance and resistance of the spiral and underpass are represented by the series inductance, L_s, and the series resistance, R_s, respectively. The overlap between the spiral and the underpass allows direct capacitive coupling between the two terminals of the inductor. This feed-through path is modeled by the series capacitance, C_s. The oxide capacitance between the spiral and the silicon substrate is modeled by C_{ox}. The capacitance and resistance of the silicon substrate are modeled by C_{Si} and R_{Si}.

The main parameters of the lumped physical model can be calculated by the following equations:

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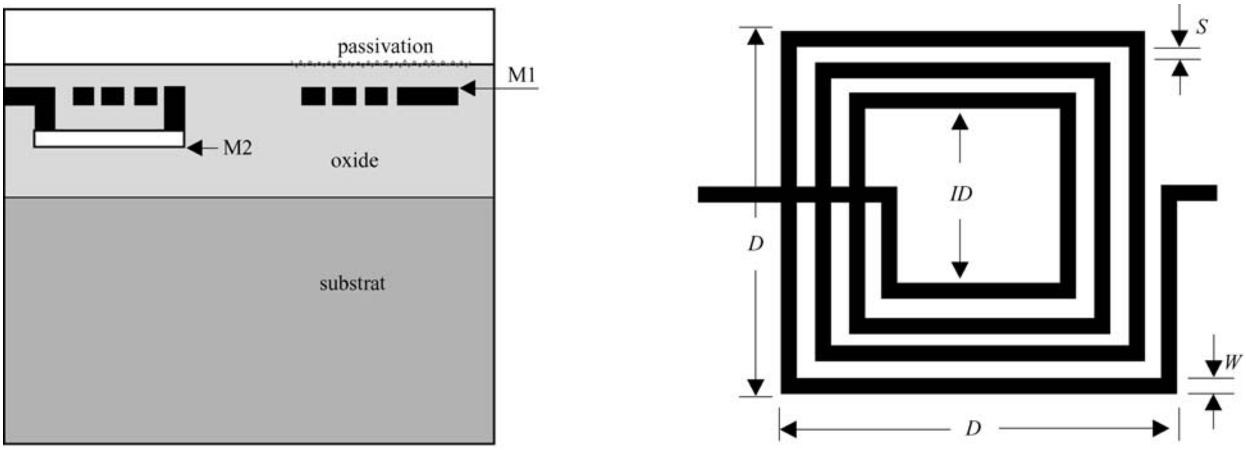


(a) (b)

Fig. 1 (a) Simplified cross-sectional view of the spiral inductor; (b) simplified top view of the spiral inductor

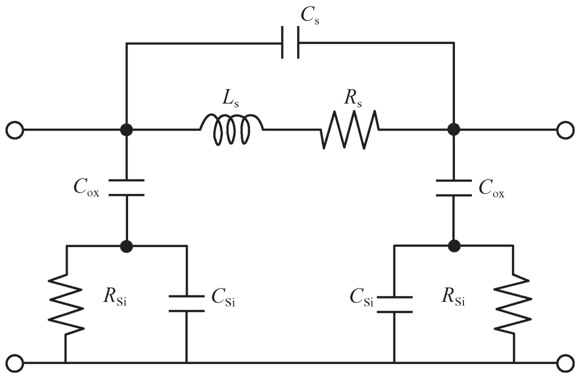


Fig. 2 Lumped physical model of a spiral inductor on silicon

$$R_s = \frac{\rho l}{w\delta(1 - \mathrm{e}^{-t/\delta})}, \tag{1}$$

$$C_s = nw^2 \frac{\varepsilon_{ox}}{t_{ox_{metal}}}, \tag{2}$$

$$C_{ox} = \frac{1}{2} lw \frac{\varepsilon_{ox}}{t_{ox}}, \tag{3}$$

$$C_{Si} = \frac{1}{2} lwC_{sub}, \tag{4}$$

$$R_{Si} = \frac{2}{lwG_{sub}}, \tag{5}$$

where l is the total length of the metal, t is the thickness of the metal, C_{sub} and G_{sub} are capacitance and conductance per unit area, respectivelty, ε_{ox} and t_{ox} denote the dielectric constant and thickness of the oxide layer between the inductor and the substrate. Other parameters are metal resistivity ρ, width w and metal skin depth δ.

The HFSS system generates full electromagnetic (EM) field solutions and associated port characteristics and *S*-parameters. *Y* parameters can be deduced from the *S*-parameters at a defined range of frequencies for individual inductors. The effective inductance *L* and the quality factor *Q* of the inductors are calculated from the *S*-parameters and *Y* parameters. From the *Q*-*f* curve, the maximum *Q* (Q_{max}) and self resonance frequency (SRF) are easily derived.

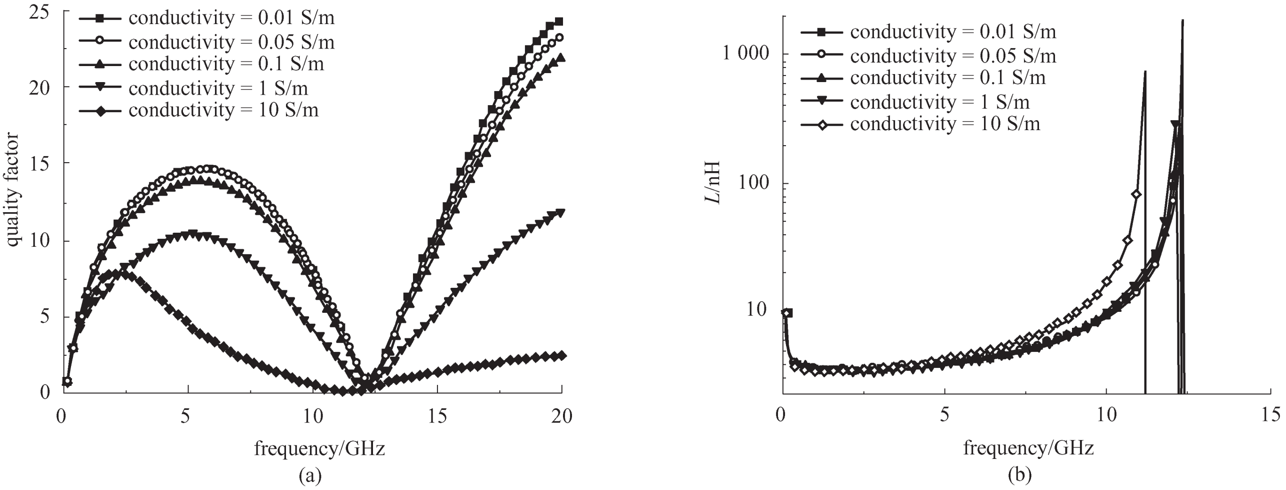
3 Results and discussion

3.1 The effect of the substrate conductivity on the performance of the inductor

Five types of inductors are chosen for the simulation with the variation of the conductivity. All types of inductors have the same layout parameters except the conductivity of the substrate. Table 1 and Fig. 3 illustrate the comparison of the *Q* factors as well as inductances *L*, $f_{Q_{max}}$ and SRF with regard to the variation of the conductivity of the substrate.

Table 1 The performance of the inductors with regard to the variation of conductivity

conductivity / $\mathrm{S{\cdot}m^{-1}}$	Q_{max}	$f_{Q_{max}}$ / GHz	inductance / nH	SRF / GHz
10	7.89	2.2	3.50	11.1
1	10.4	5.3	4.06	12.2
0.1	13.85	5.5	4.14	12.3
0.05	14.53	5.6	4.22	12.4
0.01	14.55	5.7	4.24	12.3



(a)
(b)

Fig. 3 (a) Simulation result of the spiral inductor Q factor with regard to the variation of conductivity; (b) simulation result of the spiral inductor inductance with regard to the variation of conductivity

In the case of varying the conductivity, it can be noted that the inductances which are in the same frequency and Q factor have no obvious variation as the conductivity of the substrate increases in low frequency range. In the high frequency ranges, Q factors have obvious variation as the conductivity of the substrate increases. However, the performance of the inductors will have no obvious variation when the conductivity of the substrate is lower than 0.1 S/m. When the conductivity of the substrate decreases from 10 S/m to 1 S/m, the maximum Q factor ($Q_{\max}$) is increased by 31.8%. When the conductivity of the substrate decreases from 1 S/m to 0.1 S/m, the maximum Q factor ($Q_{\max}$) is increased by 33.2%. When the conductivity of the substrate decreases from 0.1 S/m to 0.05 S/m and 0.01 S/m, the maximum Q factor ($Q_{\max}$) is only increased by 4.9% and 5.1%. When the conductivity of the substrate is lower than 0.1 S/m, the effect of the substrate on inductors is not obvious.

In low frequency ranges, the loss of the metal line is the main reason for restricting the performance of the inductors. In high frequency ranges, the loss of the substrate, such as capacitance and conductance of the substrate, is the main reason. C_{sub} and G_{sub} mainly depend on the conductivity of the substrate. As the conductivity of the substrate increases, the skin depth of the substrate also increases at the same frequency. The eddy currents in the substrate cause a significant lowering of the total inductance and increase in loss. It is the main reason for the lower Q in the high frequency range.

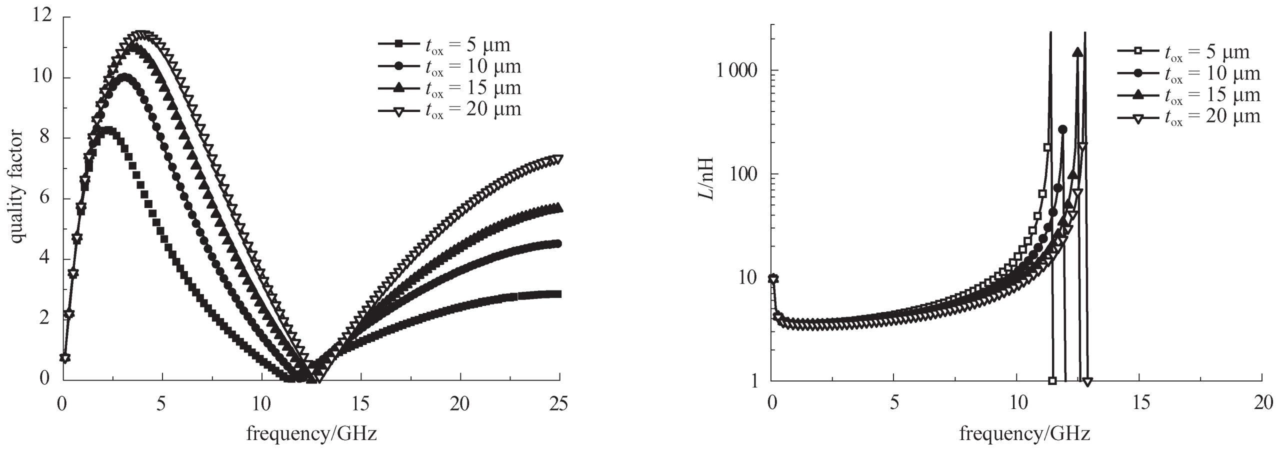
In the sub-micro silicon process, the heavily doped substrates are usually used, and the resistivity is usually from 10 Ω·cm to 30 Ω·cm. For inductors on the heavily doped silicon substrates, the magnetic coupling between the spiral and the substrate can potentially induce eddy currents in the heavily doped silicon. The extra energy loss can decrease the inductances. In the traditional metal oxide semiconductor (MOS) process, the performances of spiral inductors are limited by substrates. To achieve high performance inductors, lower resistivity is the main solution. In Ref. [4], a microwave monolithic integrated circuit power amplifier was fabricated on a P type silicon with a conductivity of 0.01 S/m. The performance of the inductor on the silicon can be improved when the conductivity is lower than 0.1 S/m.

3.2 The effect of the isolator layer thickness on the performance of the inductor

Four types of inductors are chosen for the simulation with various thicknesses of the isolator layer between the substrate and the metal. All of the inductors have the same parameters except the thickness of the isolator layer. Figure 4 and Table 2 illustrate the comparison of the Q factors as well as inductances $L, f_{Q_{max}}$ and SRF with regard to the variation of the thickness of the isolator layer

Figure 4 and Table 2 illustrate an obvious improvement of the Q factor with the increase of the oxide layer thickness. When the thickness is varied from 5 μm to 10 μm, 15 μm and 20 μm, the $Q_{\max}$ can be improved by 21.2%,32.8% and 38.5%. With the increase of the frequency, the improvement of the Q factor will be decreased. There is no obvious variation on inductances L, $f_{Q_{max}}$ and SRF with regard to the variation of the thickness of the isolation layer.

The isolator oxide layer can isolate the metal and substrate and decrease the interaction between them. A thick isolator layer can decrease parasitic capacitance, which explains the improvement of the Q factor in the low frequency. With the increase of the frequency, the parasitic capacitance C_{ox} between the metal and substrate is effectively short circuited and the substrate effect becomes the main factor affecting the performance of the inductor. Therefore, the Q factor has no obvious change



(a) (b)

Fig. 4 (a) Simulation result of the spiral inductor Q factor with regard to the variation of the oxide thickness; (b) simulation result of the inductor inductance with regard to the variation of the oxide thickness

Table 2 Performances of the inductors with regard to the variation of the silicon dioxide thickness

thickness / μm	$Q_{\max}$	$f_{Q_{max}}$ / GHz	inductance / nH	SRF / GHz
5	8.27	2.3	3.60	11.4
10	10.02	3.1	3.62	12.0
15	10.98	3.5	3.68	12.5
20	11.45	3.9	3.68	12.8

for the different isolation layers in the high frequency range.

The *Q* factor can be improved by a thicker isolation layer. Furthermore, the thickest possible oxide should be realized under the device to minimize the substrate capacitance. This not only minimizes the losses, but also maximizes the self-resonant frequency of the device. At a minimum, self-resonance will occur due to interwinding capacitance as opposed to substrate capacitance. However, a thicker isolator layer will bring difficulties to the semiconductor process. It is difficult to acquire the high quality thick oxide layer.

3.3 The effect of isolator layer material on the performance of the inductor

According to the equivalent electric model of the spiral inductor, there are two different parasitic capacitors, C_s and C_{ox}, affecting the high frequency performance of the spiral inductor. C_s is between the two conductors while C_{ox} is between the inductor and the silicon substrate. The capacitor between metals and the parasitic capacitor between the metal line and the substrate are all proportional to the permittivity ε and reciprocal to the thickness of the dielectric layer. However, the thick dielectric layer is terrible for device fabrication. Some materials with low *K* have been made. Therefore, the optimization of the material property of the dielectric layer is of great importance for improving the inductor performance.

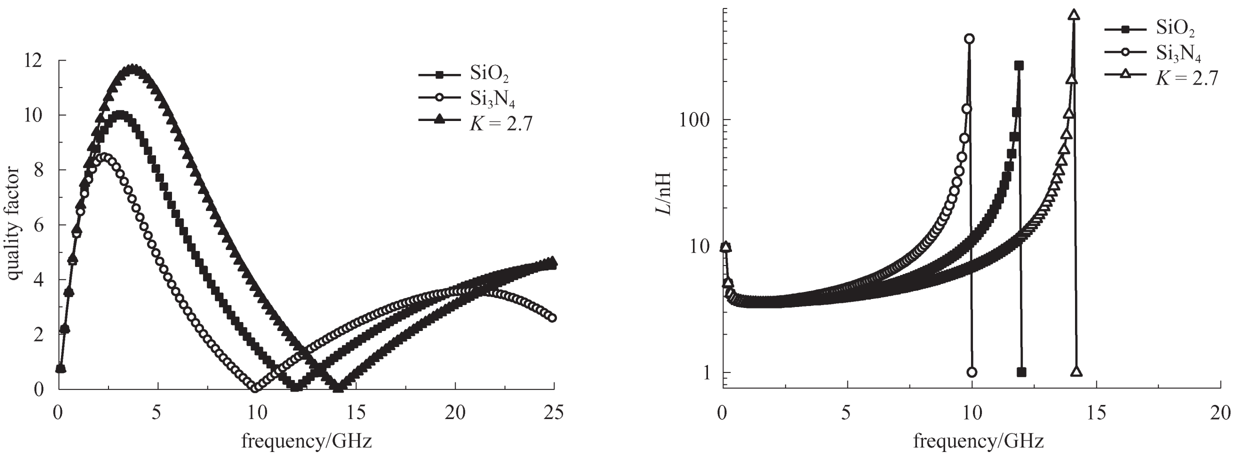
To study the impact of the materials of the substrate isolator layer on the inductor performance, three inductors with different isolator layer materials are simulated. The parameters in the three inductors excluding the *K* values of the different substrate isolator layer materials are all assumed to be the same. The simulation results are shown in Table 3 and Fig. 5.

Table 3 Performances of the inductors with regard to the variation of the dielectric layer

permittivity	Q_{max}	$f_{Q_{max}}$ / GHz	inductance / nH	SRF / GHz
7(Si_3N_4)	8.37	2.3	3.67	9.9
4(SiO_2)	10.02	3.1	3.62	12.0
2.7	11.65	3.7	3.67	14.1

In Table 3 and Fig. 5, it is obvious that the *Q* factor of the inductor increases largely with the decrease of the permittivity of the substrate isolator layer. When the relative permittivity changes from 7 to 4 and 2.7, $Q_{\max}$ increases by about 19.7% and 9.2% with about 34.8% and 60.9% increments for the frequency corresponding to $Q_{\max}$, as well as 21.2% and 42.4% increments for the SRF. Therefore, the dielectric material with low *K* value can effectively increase the *Q* factor and the SRF of the inductor.

The parasitic capacitors C_s and C_{ox} can be effectively reduced by using a material with low *K*, and the characteristic of the inductor can be improved simultaneously. Compared with other methods, by designing the structure of the substrate, adopting a dielectric material with low *K* value is not only effective in reducing the impact of the loss of the substrate, but also essential for the semiconductor interconnection. In reality, the metal line can be treated as an inductor, and the parasitic capacitor



(a) (b)

Fig. 5 (a) Simulation result of the spiral inductor Q factor with regard to the variation of the dielectric layer; (b) simulation result of the inductor inductance with regard to the variation of the dielectric layer

can be made of the metal lines in the interlink layer and the dielectric layer. Therefore, the LC vibration could be triggered by the inductor and the capacitor. Thereafter, the operating frequency goes down. It is not easy to reduce the inductor of the metal line, but effective to reduce the capacitor attributed to the coupling effect of metal lines by using a material with low K and low permittivity.

The dielectric material with low K value has attracted a lot of scientists and engineers in micro-electronics techniques. As far as we are concerned, the K value could be 2.5. A porous membrane, named methylsilsesquioxane (MSQ) adopted by International Sematech (ISMT), is composed of silica and hydrocarbon, and its dielectric constant is about 2.5.

3.4 The effect of SiGe alloy in the substrate on the performance of the inductor

Silicon germanium heterostructure bipolar transistor (HBT) and strained CMOS device are the focus of silicon-based micro-electronics research at present. The nonselective epitaxial growth is the main method of material fabrication for the production of SiGe HBT and the strained silicon material. Compared with the conventional silicon technologies, one more layer with SiGe alloy is needed in the substrate material of the passive device. However, the effect of SiGe alloy on the substrate for a passive device has not been reported yet. More accurate expression of the device's characteristic is necessary for the design of the radiofrequency chip. Therefore, we analyze the impacts of the SiGe alloy layer on the characteristic of the inductor in two different substrate structures, which are exemplified as follows:

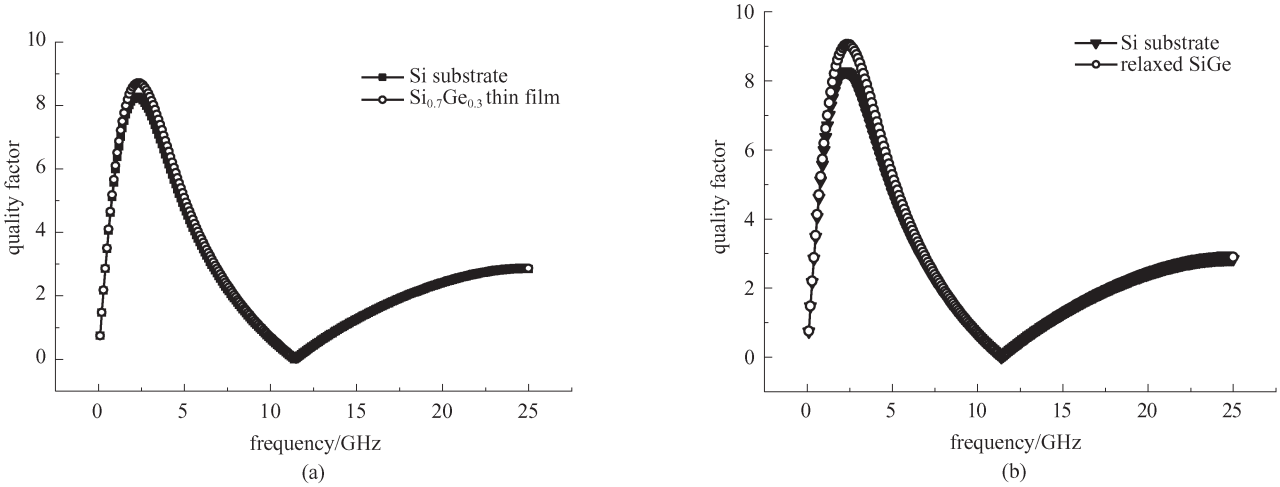
1) The substrate structure that can be integrated with SiGe HBT, whose primary feature is that a 70-nm $Si_{0.7}Ge_{0.3}$ alloy layer is inserted between the inductor and the substrate.

2) The substrate structure that is integrated with strained silicon CMOS chip, with a 3-μm SiGe alloy layer, of which the composition of Ge degrades from 0.3 to 0, is inserted between the inductor and the substrate. The simulation results are shown in Fig. 6.

In Fig. 6, it can be seen that the SiGe alloy layer has no effect on the inductance. The Q factor of the inductor has no obvious change. However, compared with the inductor on a pure silicon substrate, the maximum of the Q factor on the substrate structure with SiGe alloy layer will increase a little, by about 5.32% increment for a structure with 70 nm $Si_{0.7}Ge_{0.3}$ alloy layer. The thicker the SiGe alloy layer is, the larger the increment of the maximum of Q factor will be, with about 11.4% increment for a structure having 3 μm gradual degrading SiGe alloy layer. When the SiGe alloy layer is inserted, the high frequency coupling efficiency of the inductor and the substrate will decrease, so the effect of the substrate on the performance of the inductor will decrease, and the Q factor of the inductor will increase simultaneously. Therefore, the SiGe alloy layer is not only effective for increasing the performance of the active device, but also appropriate for improving the characteristic of the passive device.

4 Conclusions

The effect of the loss of the substrate on the inductor decreases with the reduction of the conductivity of the substrate. The inductor on the substrate with lower conductivity will have higher Q factor. For the silicon substrate, when the conductivity falls down from 10 S/m to 0.1 S/m, the Q factor of the inductor increases obviously. However, when the conductivity is decreased to a much lower value, the enhancement tendency of the Q factor will slow down. Along with the increase of the



(a)

(b)

Fig. 6 (a) Simulation result of the spiral inductor Q factor with a thin film of SiGe on the substrate; (b) simulation result of the spiral inductor Q factor with a thick film of relaxed SiGe on the substrate

thickness of the oxide layer between the metal and the substrate, the coupling efficiency between the inductor and the substrate decreases, and the capacitor caused by the oxide layer also decreases, and consequently the effect of the substrate on the performance of the inductor decreases simultaneously, while the Q factor of the inductor increases. However, it is difficult to generate a thick oxide layer. The isolator layer with low K dielectric not only effectively improves the Q factor of the inductor, but also effectively increases the self-resonant frequency. Thus, it is an ideal way to improve the performance of the silicon-based spiral inductor by using low K dielectric. Also, the low K dielectric will be very useful in the future of micro-electronics technologies. The SiGe alloy layer can improve the performance of the inductor in some way in SiGe BiCOMS, but the effect is not obvious because the thickness of the SiGe alloy layer is generally small.

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