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RESEARCH ARTICLE

Yan HE, Jianyun HU, Hao MIN

An ultra low-voltage, low-power baseband-processor for UHF RFID tag

Abstract A novel ultra low-voltage, low-power baseband-processor for UHF radio frequency identification (RFID) tag is presented here. The baseband-processor is compatible with the EPC™ class-1 generation-2 (C1G2) UHF RFID protocol, and fits the requirements of ultra low-power of passive tags. Based on the analysis of the special power consumption of the tag, a new architecture is proposed. A novel scheme for generating pseudo-random numbers as well as a new method of partial-decoding is developed. Besides, other low-power techniques are also adopted for the special baseband-processor which implements complex functions, such as encoding/coding, anti-collision and authorization scheme, and reading/writing operation to EEPROM. The chip was fabricated in 0.35 μm 1P3M standard CMOS process. Experimental results show that it achieves low power operation of 3.15 μW @ 1.5 V with the core area of 1.1 mm × 0.8 mm.

Keywords radio frequency identification (RFID), tag, low-power, baseband-processor, instantaneous power

1 Introduction

Nowadays, the application of radio frequency identification (RFID) system is increasing rapidly, including supply chain management, access control, public transportation, open-air events, airport baggage, and so on. To meet the market requirements, the preferred RFID system must exhibit features like low cost and low-power, especially for tags in great demand [1].

The RFID system is a wireless communication system in which the radio frequency (RF) signals realize contactless communication with the coupling of electro-magnet to achieve multi-objectives identification. In terms of hardware, it consists of a reader and a tag. According to the latest specification of the RFID air interface-EPC™ C1G2 UHF RFID protocol [2], the communication between the reader and tag is described as follows. First, a reader transmits data to a tag by modulating an RF signal in the frequency range of 860–960 MHz; and then the passive tag recovers both the data and operation power from the RF signals. After signal processing, the tag backscatters the reply data to the reader in the way of modulating the reflection coefficient of the antenna while the reader is transmitting a continuous wave (CW) RF signals to the tag.

Research results show that the energy received by the tags is inversely proportional to the square of operation distance. Longer operation distance requires smaller power dissipation [3–6]. Therefore, power consumption is a key factor for the performance of the tag. Usually, the chip of the tag is comprised of RF front-end, baseband-processor and EEPROM. Researchers have done many efforts in reducing the power of RF front-end and EEPROM [5,7], but the results show that it is too difficult to greatly reduce power. The baseband-processor, as the main block to process protocol, occupies about 40% power consumption of the whole tag. Therefore, a low-power, low-voltage baseband-processor can achieve maximum operation range.

Recently, most baseband-processors choose the CPU architecture [8–11], and almost do not analyze the characteristics of protocol processing or develop special circuits [12]. However, based on the characteristic of protocol processing and special low-power demands, this paper proposes a new architecture with power management scheme, and also presents a novel method of partial-decoding and a new scheme of generating 16-bits pseudo-random numbers. Moreover, other low-power techniques are introduced for the low-power design.

2 Power analysis and architecture

2.1 Power analysis

Usually, as to the electronic portable products powered by a battery, the total energy is finite, whereas, large

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Yan HE (✉), Jianyun HU, Hao MIN
Mirco-electronics Department, Fudan University, Shanghai 201203, China
E-mail: yanhe@fudan.edu.cn

instantaneous power can be provided. Therefore, the low-power design for these products is low energy design in essence. However, for the passive tag whose energy is recovered from electro-magnetic carriers, the total energy is infinite as long as the tag stays in a continuous electro-magnetic field permanently, while its instantaneous power is finite, depending on the energy transmitted by the electro-magnetic carrier instantaneously. Thus, the low-power design for the tag is low instantaneous power design, especially the maximum of instantaneous power. Therefore, the idea of making the power consumption more evenly distributed over the whole operation period can eliminate the peak power, and achieve longer operation distance and higher performance [5].

2.2 Architecture

According to the protocol, the tag features are as follows: 1) The tag is passive, so the low-power design for the tag should be more focused on decreasing the maximum instantaneous power; 2) Since communication between the tag and the reader adopts half-duplex mode, the tag only executes one command at one time and will not respond to any other command until it finishes; 3) The "slotted aloha" anti-collision algorithm which the tag adopts doesn't need a quick response (the response time is about 187.5–750 μs). Therefore, protocol execution doesn't require high speed; 4) The tag executes commands in an order of receiving and decoding signals → CRC checking → command analyzing → executing command (implementing anti-collision algorithm and authentication scheme, reading/writing EEPROM) → CRC generating → encoding and transmitting signals.

Nowadays, CPU architecture as the most conventional one is based on CISC command-set [8–11], such as Neumann architecture or Harvard architecture. The architecture is mainly designed for the processors with volumes of computation, high speed and parallel execution for multi-commands. It requires all the modules to work together. Therefore, this kind of architecture consumes large instantaneous power, and the power consumption of some modules, such as the ROM, is difficult to reduce. Considering the characteristics of protocol processing and the special low-power requirement of the tag, a novel architecture is presented, as shown Fig. 1, where the dash-line represents clock signal. Power management module (PWM) transmits clock and enable signals to other modules to control their operation states; CU delivers control signal to direct other modules so that they can implement anti-collision algorithm and authentication scheme; OCU assists CU to control the data-flow of encoding and CRC generating; besides, RD is the command signal transmitted by the reader and MOD is the reply signal from the tag.

The merits of the proposed architecture are as follows: 1) It is eases modification or improvement on each module, since the modules are divided by function and independent of each other; 2) The architecture gives flexibility in logic control, is good for implementing the power management scheme and pipeline operation; 3) The scheme of multi-modules division allows the power to spread evenly over the whole chip and the maximum size of one module is no more than 35% of the baseband-processor (see Fig. 2), so that the power will not dissipate mainly on one module and cause larger instantaneous power consumption when it works. Finally, the proposed architecture also provides a new idea on how to design a low-power baseband-processor for other half-duplex communication systems.

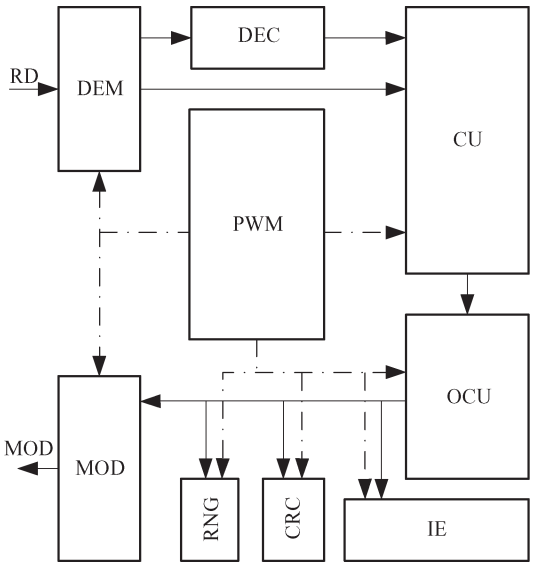

Fig. 1 Baseband-processor architecture diagram
DEM: Data decode module; DEC: Command decoder module; CU: Control Unite module; OCU: Output control unite module; IE: Interface to EEPROM module; MOD: Data encode module; PWM: Power management module; RND: Random generator module; CRC: Cyclic redundancy checks module;

With the simulation results and the circuit scale of each module which is compiled by a design compiler, Fig. 2(a) illustrates the percentage of power consumption for each module, where the largest one is CU, amounting to about 34%. Figure 2(b) shows each module's active period when the tag processes the protocol (where the dash-line denotes the optional operation).

3 Design of low-power baseband-processor

Usually, in digital circuits, power consumption consists of both static power and dynamic power. The dynamic power consumption is the dominant one, occupying about 90% of total power consumption. It can be calculated as:

$$P = 0.5\alpha C_{\mathrm{L}} V_{\mathrm{DD}}^2 f, \tag{1}$$

where α represents the switching activities, f represents the frequency of circuit operation, C_{L} represents the total load

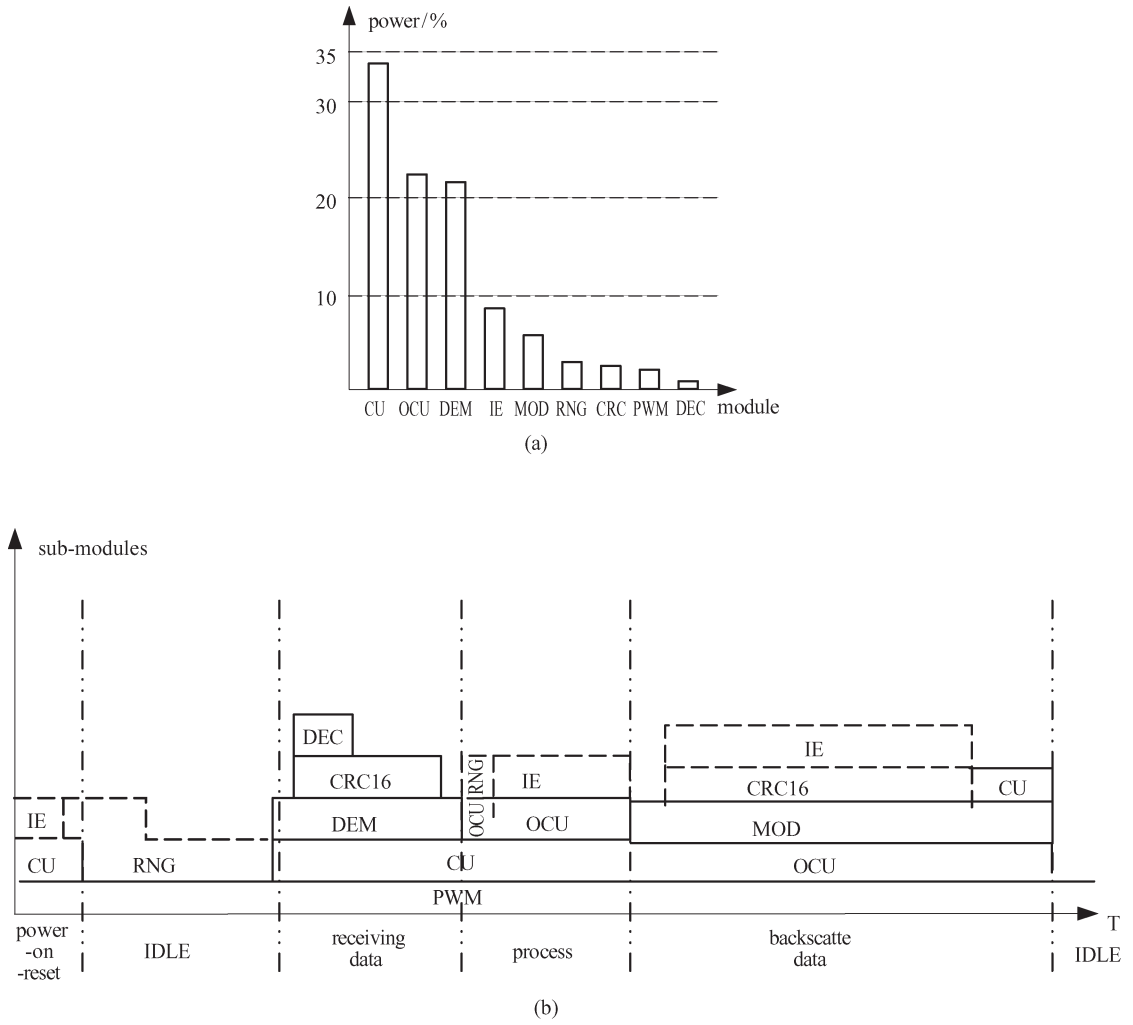

Fig. 2 (a) Power consumption of each module; (b) working period of each module

capacitance of circuit and V_{DD} represents power supply voltage. Therefore, low-power design can be achieved by reducing the V_{DD}, C_L, f and α. The low-power techniques adopted in our design are presented in the following.

3.1 Power management scheme with gated-clock

As Fig. 2 (b) shows, there is no need for each module to work at all times. So, redundant power consumption can be avoided if the modules are stopped when they are idle. However, the normal enable signal can't cut off the clock of the modules which dissipates about 1/3 power consumption of the design. In order to eliminate the redundant power consumption, a gate-clock technique is employed, which can cut off the clock of the modules that do not work at that time [13,14]. By controlling the clock on/off for modules, the instantaneous load capacitance of clock tree is reduced. Thus, the maximum instantaneous power is lowered significantly.

On the other hand, in order to ensure operation performance, the asynchronous handshake scheme [10,13,15] is introduced between the PWM and the other modules, as shown in Fig. 3. For example, when one module is required to run, the PWM sends a request signal REQ first and the module replies with an ACK signal. When both REQ and ACK are valid, i.e., the first handshake finishes, PWM allocates the clock to the module and it starts to work. After the module fulfills its task, ACK turns invalid and the clock is cut off. Consequently, the module stops running and REQ turns invalid. Then the second handshake finishes. Assume that the maximum of instantaneous power consumption of the conventional baseband-processor is 100%. The instantaneous power dissipation of the baseband-processor with power management scheme is described in Fig. 4, where the maximum of instantaneous power consumption is reduced by about 30%.

3.2 A new method of generating 16-bits pseudo-random numbers

According to the protocol, the anti-collision scheme requires each tag to generate unique 16-bits pseudo-random

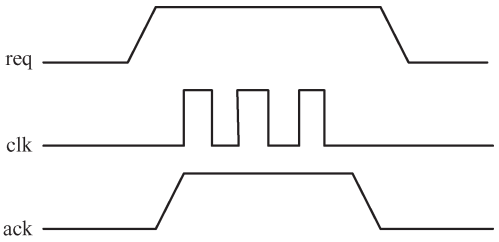

Fig. 3 Timing of handshake protocol

number (RN16). So how to obtain different RN16 based on the uniform random number generator (RNG) is the key problem for anti-collision scheme implementation. A simple but effective method is proposed, using the diversities on the seeds and the operation periods of the RNGs: when a tag falls into the reader's field, it first turns into power-on-reset state. At the moment, it fetches the data CRC-16 of EPC stored in EEPROM (which is defined by the manufacturers) and puts into the RNG as a seed. Then RNG works until the tag detects a low level signal, which means that the reader starts to transmit a command to the tag. Therefore, to the greatest extent, the dissimilarity among tags is achieved due to the dual-randomicity of the seeds and the operation periods. Besides, since RNG works at power-on-reset period and command detecting period when most sub-modules do not work, the peak of instantaneous power consumption is lowered.

3.3 A partial-decoding method for variable-length commands

A partial-decoding method is proposed. In the protocol, the commands are of variable-length, from 2 to 8 bits. In conventional 8–64 decoder, the operation of decoding the command of less than 8 bits would cause redundant switches, which increases instantaneous power consumption, and dissipates hardware resource. To overcome these drawbacks, a partial-decoding method is developed, as shown in Fig. 5, where the circle denotes finishing decoding a command, rectangle denotes multiplexer with 2-inputs. It decodes the first 2 bits of the command first. If the command is just the 2-bits, the decoding is finished; otherwise, the second 2 bits (3rd bit and 4th bit) or the third 2 bits (5th bit and 6th bit) should be chosen to decode according to the first 2 bits; and the rest could be deduced by analogy. Therefore, this method not only improves the speed of decoding, but also reduces the area (i.e. number of gates) and eliminates redundant power consumption.

3.4 A pipe-line structure for receiving/transmitting signals

The idea of pipe-line is flexibly used for processing the instruction and backscattering the reply data to the reader. Take coding for transmitting signals for example,

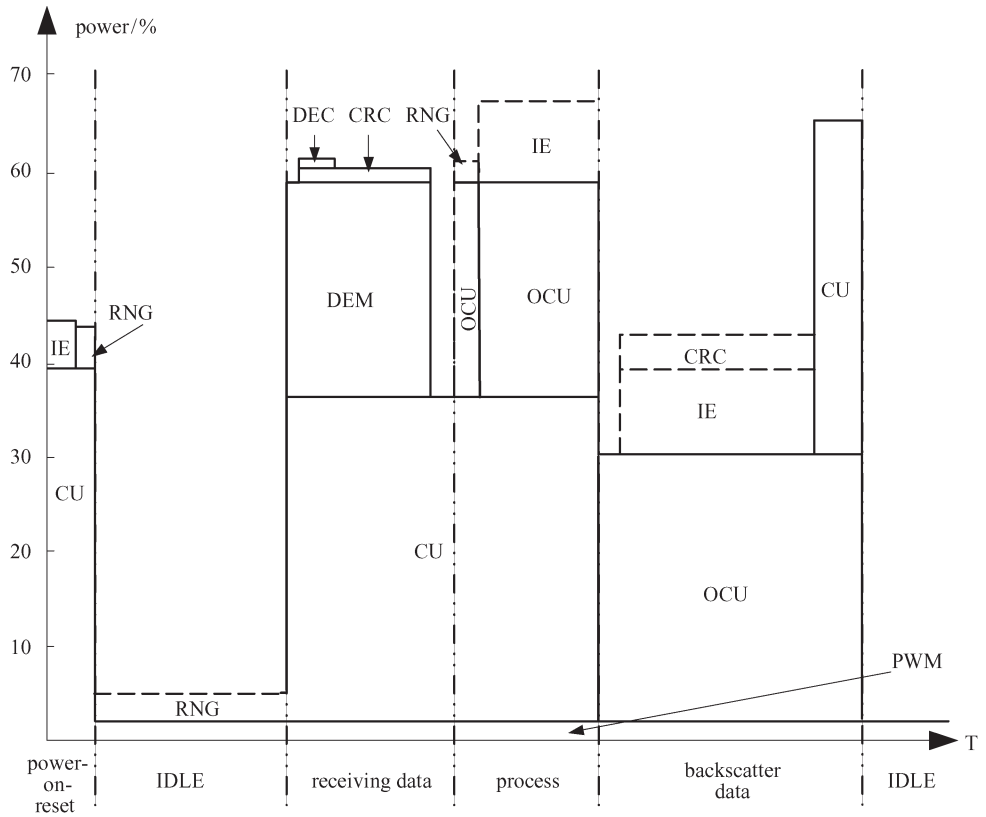

Fig. 4 Power consumption of each period with power management scheme

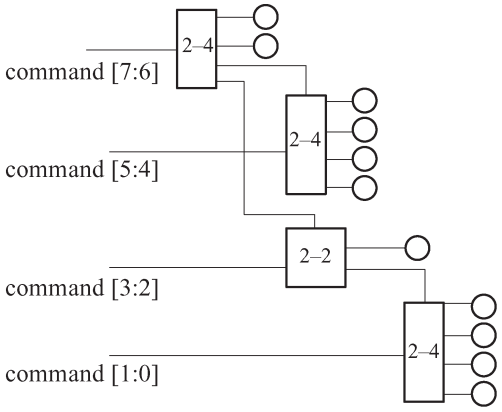

Fig. 5 Partially command decoder

the traditional method is: fetching all the data which should be transmitted from EEPROM first and putting them into a group of registers, then sending to CRC module to generate CRC codes bit by bit, finally coding and backscattering them (both the data and CRC codes) in serial mode. As a result, it would cost a number of register resource and take long operation time. To solve this problem, 3-stage pipe-line structure operation is developed (see Fig. 6): fetching data, generating CRC code and coding data. All the transmitting data are operated bit by bit. The comparison result shows that the pipe-line structure not only decreases the response time but also improves the operation efficiency. Besides, since only one register is required, both the area and the power consumption are saved.

3.5 Reducing logic depth technology

A low-power technique, called reducing logic depth, is adopted in our design. This technique reduces redundant power consumption by balancing the delay of each data path and minimizing extra transitions. Take the adder for example (see Fig. 7), in the adder with chain implementation, the logic length is deep and the delay of each data path is imbalanced. Therefore, it will cause extra switches and

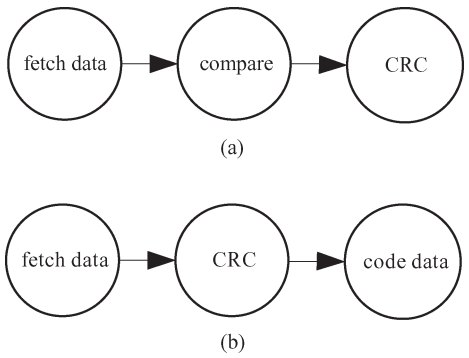

Fig. 6 Pipe-line operation. (a) Pipe-line for receiving; (b) pipe-line for transmitting

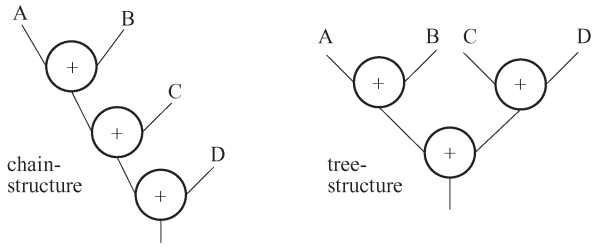

Fig. 7 Adder with chain-structure and tree-structure

dissipate more power, compared with the one with tree implementation.

Furthermore, other low-power techniques are adopted in the design as well, such as using (n-1) AND gates to implement an n-bit comparator, employing Gray-code state-machines, and so on. They work together to reduce power efficiently.

3.6 Design implementation and verification

The design-flow of implementation and verification for the chip of baseband-processor is: RTL-level circuit design (verilog HDL) → function verification (using Modelsim and Altera FPGA platform) → compiling design (using design compiler of Synopsys) → place and route (using silicon ensemble of Cadence) → design rule check (DRC) and layout vs schematic (LVS) (using calibre of Mentor) → tapping out (Chartered 0.35 μm 1P3M process). Figure 8 (a) is the verification platform based on FPGA and Fig. 8(b) is the photograph of the chip. The design is about 7 000 gates with the area of 1.1 mm × 0.8 mm. The power is 3.15 μW with the average current of 2.1 μA @1.5 V. Compared with that in Refs. [8,10–12], our design can implement complex function with lower power dissipation, as shown in Table 1, achieving our expected object.

4 Conclusions

In this paper, a novel ultra low-power low-voltage baseband-processor is presented. Based on the characteristic of protocol processing and special low-power demand, a new architecture with the scheme of power management is proposed. For circuit design, a partial-decoding method and a RN16 generating scheme is developed. Besides, other low-power techniques, such as pipe-line structure, reduce of logic depth, are adopted to reduce power. The chip is fabricated in Chartered 0.35 μm CMOS process. Experimental results show that it achieves high performance with lower power consumption.

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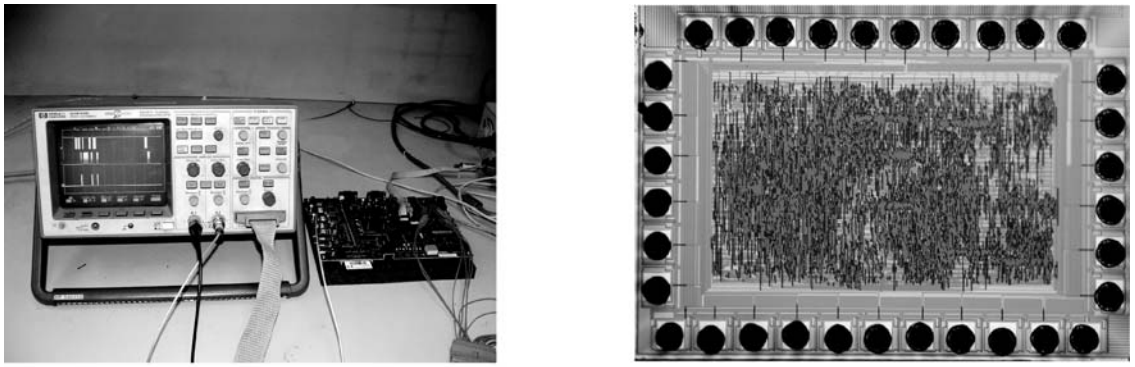

(a) (b)

Fig. 8 (a) The platform for FPGA verification; (b) microphotograph of chip

Table 1 Summary of performance and comparison to others' work

	authors	S. Masui [8]	A. Abrial [10]	M. Usami [11]	Y. Fukumizu [12]	this work
	publish time	1999	2001	2004	2004	
	process	0.8 μm	0.25 μm	0.18 μm	0.18 μm	0.35 μm
function	coding/decoding, command decoder	Yes	Yes	Yes	Yes	Yes
	read/write EEPROM	Yes	Yes	No	Yes	Yes
	anti-collision scheme	Yes	Yes	No	Yes	Yes
	CRC	No	No	No	Yes	Yes
	others	No	BIST	No	Time hopping DS-CDMA	No
	power	<2 mW*	0.8 mW	1.5 μW*	23.4 μW*	3.15 μW

Note: $*$ means the power consumption of whole tag

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