Front. Electr. Electron. Eng. China (2006) 4: 385–389
DOI 10.1007/s11460-006-0074-4

RESEARCH ARTICLE

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A zero-voltage zero-current soft switching DC/DC converter

Abstract A novel three-level zero-voltage zero-current switching (ZVZCS) DC/DC converter is proposed in this paper. A tapped-inductor is used to replace the normal output filter inductor, so that the circulating current in the zero-state can be reset to zero. The reset voltage and the reset time can be set conveniently just by simply changing the winding ratio of the tapped inductor. The converter achieves a zero-current tuning off for inner switching, and a zero-voltage tuning on for outer switching. No circulating current exists in the zero state, so that the loss in the on-state is reduced, and the efficiency can be improved. The experimental results verify that the ZVZCS has low voltage stress, zero-voltage and zero-current switching.

Keywords three-level DC/DC converter, tapped inductor, soft-switching

1 Introduction

In order to meet the standards corresponding to the input current quality, such as the IEC61000-3-2, the power factor correction (PFC) technique has been commonly used in many power supplies. It is a well known fact that the three-phase single-switch boost rectifier is a quite competitive option for this PFC stage, since it easily complies with the aforementioned standard that is also simple, efficient, reliable and comes at a low cost. However, in order to reduce the harmonic distortion in the three-phase boost rectifier, the output voltage must be increased with respect to the input voltage. In fact, its output voltage may be even higher more than 800 V. This high output voltage will automatically increase the voltage stress for the second-stage DC/DC converter, and will reduce the efficiency of the converter. The three-level technique proposed can solve this high voltage stress problem. In fact, only half the level of the DC link voltage will be applied to the switch in this converter. Therefore, this new topology is widely used in high-voltage high-power application cases [1–3].

Another great feature of this converter is that the soft-switching technique can reset the primary current during the freewheeling stage, and achieve a zero-current switching (ZCS) for the inner switches**,** so that the efficiency of the converter can be greatly improved. Canales et al. [4] proposed a modified converter with an active switch and a clamped capacitor in the secondary side. In their study, when the auxiliary active switching device was turned on, the voltage of the clamped capacitor reflects to the primary side of the transformer and applies to the leakage inductor L_r. Thus, the circulating current is being reduced until it reaches zero, and the inner switches realize the zero current switching (ZCS). This topology has to increase the auxiliary active switching device and should design its corresponding logic control circuits. Reference [5] adopted an auxiliary recoverable snubber capacitor to deliver and store energy. The lossless snubber capacitor cannot only reset the primary current, but also absorb the high frequency ringing voltage due to the reverse recovery of the secondary rectifier diodes. The main disadvantage is that there still is a high voltage stress on the rectifier diodes. A zero current switching converter with the help of a tapped inductor and a snubber capacitor was presented in Ref. [6]. By setting an appropriate turn ratios of the tapped inductor, the ZVZCS condition can be extended to a very wide range of load. However, this circuit has some disadvantage such as the presence of high voltage spikes on the secondary side of the transformer because of the resonance of the inductor in primary and the capacitor in secondary.

This paper proposes a novel three-level ZVZCS DC/DC converter by introducing a tapped inductor. The zero-current switching mechanism of the proposed converter is quite different from that in the traditional ZVZCS DC/DC converters. Because no recoverable snubber capacitor is used, the voltage spike in the secondary side of the transformer

Translated from *Journal of Zhejiang University* (*Engineering Science*), 2006, 40(2): 334–338 (in Chinese)

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can be avoided. The voltage and the time to reset the circuit current can be regulated easily just by setting the turn ratios of the tapped inductor. No auxiliary active switch is needed. The principle of this converter is analyzed, and experimental results in a 400 W setup are given to verify the validity of the proposed converter.

2 The proposed converter principal

The proposed ZVZCS phase-shifted DC/DC converter is shown in Fig. 1. In this circuit, a tapped inductor L_d is used to replace the normal output filter inductor. This tapped inductor functions both as a filter and a transformer (to deliver the reset energy). A capacitor C_r is used to store the reset energy. A small value inductor L_r is used to restrict the current delivered from the tapped inductor to the capacitor C_r. During the freewheeling stage, when the diode D_{S_1} is turned on, the voltage across the capacitor C_r can be reflected to the primary through the main transformer T_r, and applies to the leakage inductor L_k, which forces the freewheeling circulating current to be reset to zero.

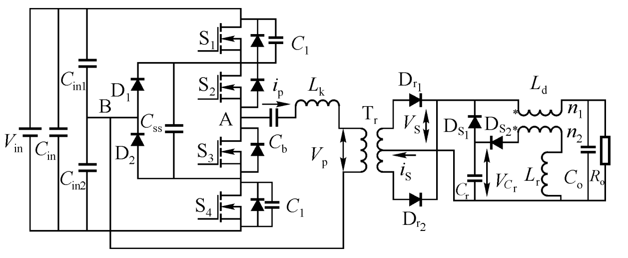

Fig. 1 ZVZCS three-level DC/DC converter

In order to simplify the analysis of the converter, it is assumed that it is in steady state operation. The inductance of the tapped inductor L_d is large enough, so that its primary current can be treated as a constant level during commutation interval. The flying capacitor C_{ss} is so large that its voltage is constant. The transformer magnetizing current is neglected. Figure 2 shows the operation waveforms. The proposed converter has eight modes in each half of the operation period as shown in Fig. 3. These modes are described as follows:

Mode 0 (t_0-t_1): the outer switch S_1 has been conducted before t_0. The outer switch S_2 turns on at t_0, and the primary current flows from $V_{in}/2$ and C_{in}, via S_1, S_2 and L_k to the primary-side of the transformer. In this stage, the rectifier diodes D_{r_1}, D_{r_2} are conducting simultaneously, both the primary and the secondary side voltage of the transformer is zero, and the input voltage ($V_{in}/2$) is totally applied to the inductor L_k. The primary current i_p increases linearly from zero to $n_s i_{L_d}/n_p$, where n_p, n_s are the turns of the primary and secondary-side of the transformer, respectively, and i_{L_d} is the current of the tapped inductor current.

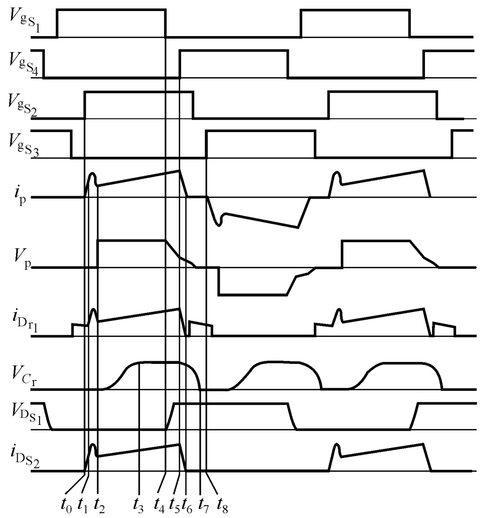

Fig. 2 Principal waveforms of the proposed converter

$$i_p=\frac{1}{L_k}\frac{V_{in}}{2}(t_1-t_0) \tag{1}$$

Mode 1 (t_1-t_2): the reversed recovery stage of the rectifier diode (D_{r_2}). In this mode, the input voltage $V_{in}/2$ is applied to the transformer, and the rectifier diode D_{r_2} is reverse biased. Because of the diode reverse recovery effect, an oscillation appears between the parasitical capacitor of D_{r_2} and the leakage inductor L_k This oscillation is governed by following equations:

$$\begin{cases} L_k'\dfrac{di_p'}{dt}+V_{C_{D_{r2}}}=V_{in}' \\ i_p'=I_0+C_{D_{r2}}\dfrac{dV_{C_{D_{r2}}}}{dt} \end{cases} \tag{2}$$

where $i_p(t_1)=n_s i_0/n_p$, and when $t=t_2$, $i_0=i_{DC_{r_1}}$ $u_{L_K}=0$(i_p', L_K', V_{in}' is a separate value which converts into secondly of i_p, L_K, V_{in}). The rectifier diode D_{r_2} is reverse biased.

Mode 2 (t_2-t_3): this is the energy delivering stage. Half of the DC link voltage ($V_{in}/2$) applies to the transformer, and power is delivered to a load through the transformer and inductor. At the same time, the secondary side of the inductor charges the capacitor C_r via the current limiting purposed inductor L_r. The charging current is described as

$$\begin{cases} L_r\dfrac{di_{L_r}}{dt}+V_{C_r}=\dfrac{n_2}{n_1}(V_s-V_0) \\ C_r\dfrac{dV_{C_r}}{dt}=i_{L_r} \\ V_s=\left(\dfrac{n_s}{n_p}\right)\dfrac{V_{in}}{2} \end{cases} \tag{3}$$

The initial and end states conditions are:

$V_{C_r}(t_2)=0$, $i_{L_r}(t_2)=0$, and $i_{L_r}(t_3)=0$,

$$V_{C_r}(t_3)=2\left[\frac{n_2}{n_1}(V_s-V_0)\right]$$

where n_1, n_2 are the turns of primary and secondary windings of the inductor L_d.

Mode 3 ($t_3 - t_4$): when the charging current i_{L_r} regresses to zero, the diode D_{S_2} is switched off, and ends the charging mode. The clamping capacitor voltage V_{C_r} is kept constant. During this stage, the secondary side of the tapped inductor is an open circuit (the voltage V_{C_r} is much smaller than V_s), and the tapped inductor functions as a common one.

Mode 4 (t_4 – t_5): at t_4, the switch S_1 is turned off, i_p charges the capacitors C_1, and discharges the capacitors C_4 via fly capacitor C_{ss}. After the voltage across the S_4 reduces to zero, its reversed-parallel diode will be turned on, and the outer switch S_4 can be turned on in zero-voltage state.

Mode 5 (t_5 – t_6): the diode D_{S_1} automatically conducts when the secondary voltage V_s is reduced to V_{C_r}, the secondary side voltage of the transformer V_s is clamped to V_{C_r}. At the same time, the voltage V_s is reflected to the primary side by the transformer. The primary voltage V_p is clamped

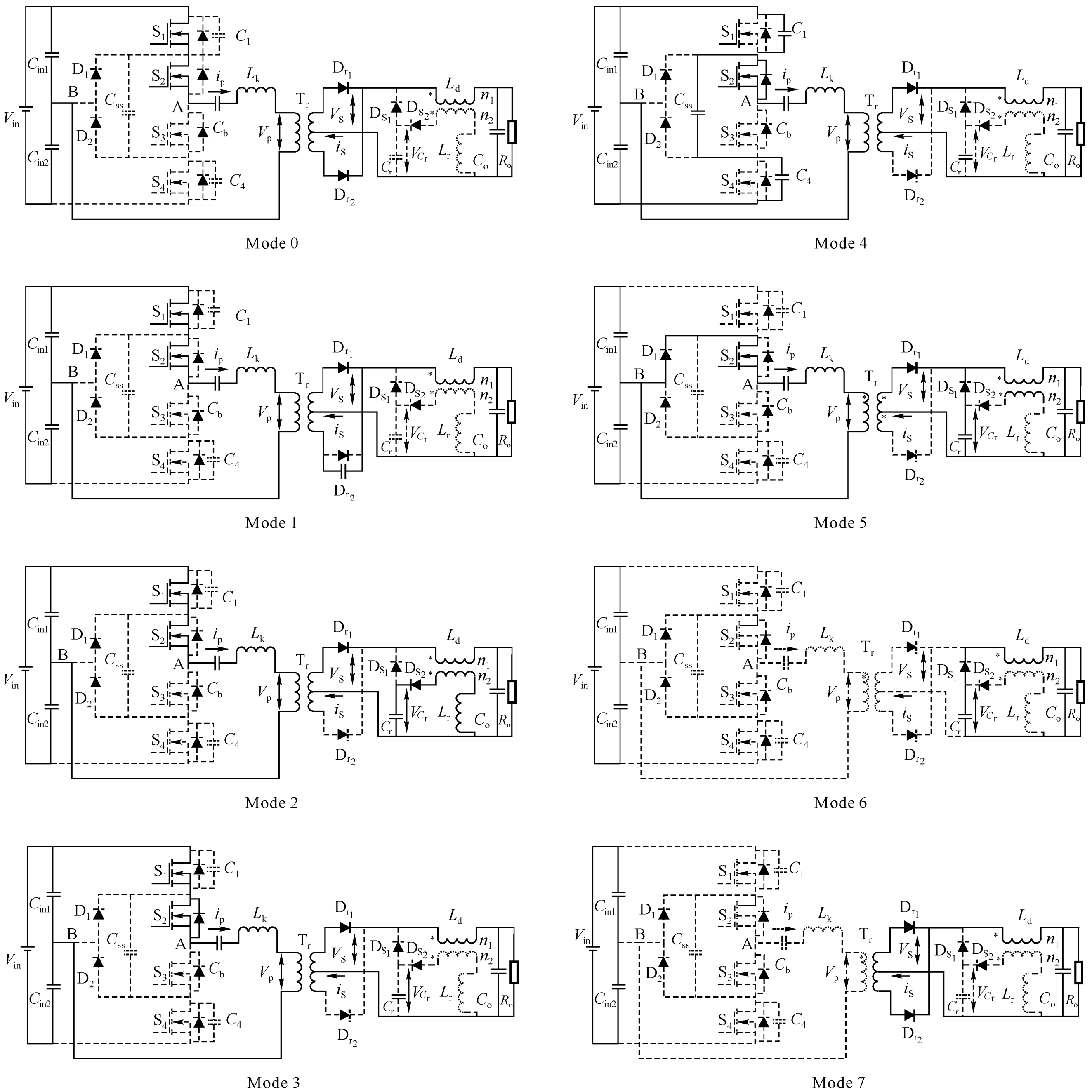

Fig. 3 Circuit configuration for operation mode in ZVZCS DC/DC converter

to the level of $n_p V_{C_r} / n_s$. A resonance happens between the leakage L_k and the capacitor C_r. The primary current i_p quickly decreases to zero. The secondary current i_s will decrease to zero simultaneously, and the rectifier diode D_{r_1} is turned off automatically.

$$\begin{cases} C_r \dfrac{dV_{C_r}}{dt} = i_p'(t - t_5) + i_{L_d} \\ i_p' = \dfrac{n_p}{n_s} i_p \end{cases} \tag{4}$$

Mode 6 ($t_6 - t_7$): there is a bit of positive voltage across the capacitor C_r, the rectifier diode D_{r_1} is blocked by V_{C_r}, and the capacitor C_r discharges to the load through the diode D_{S_1} until V_{C_r} decreases to zero at time t_7.

Mode 7 ($t_7 - t_8$): this is a freewheeling stage. After V_{C_r} is reduced to zero, the storage energy in the tapped inductor flows through the diodes D_{r_1}、D_{r_2}. The voltage across the transformer is zero. This stage does not transfer power. At t_8, the switch V_{S_3} is turned on by a logic control. The current i_p flows to the transformer in the reverse direction, and starts a new half cycle.

3 Experiments

An experimental prototype was developed to verify the validity of the proposed ZVZCS three-level DC/DC converter. Table 1 shows the specifications and the parameters.

Table 1 Experiment parameters of prototype converter

Parameters	Values
V_{in}/V	530 DC
V_{out}/V	40 DC
I_{out}/A	10
f/Hz	100 K
S_1–S_4	IRF840
D_{r_1}–D_{r_2}(diode)	MUR3060PT
D_1, D_2	U860
D_{S_1}, D_{S_2}	IRO36X
C_{in1}, C_{in2}/μF	0.22 (450 V)
C_{ss} /μF	0.33(250 V)
n_p/n_s	18/5
L_k/μH	11
C_r/μF	0.1
L_r/μH	6
L_d(primary/secondary)/ μH	464/156

Experimental waveforms of the proposed converter are shown in Fig. 4. Figure 4(a) is the primary voltage V_{AB} and current i_p. Obviously, i_p decreases to zero swiftly when V_{AB} is zero. Figure 4(b) shows the voltage V_s and current i_s in the secondary side of the transformer. It can be seen that there is a voltage trail during the voltage fall stages. It is this trail voltage that reflects to the primary side of the transformer and resets the circulating current. Figure 4(c) shows

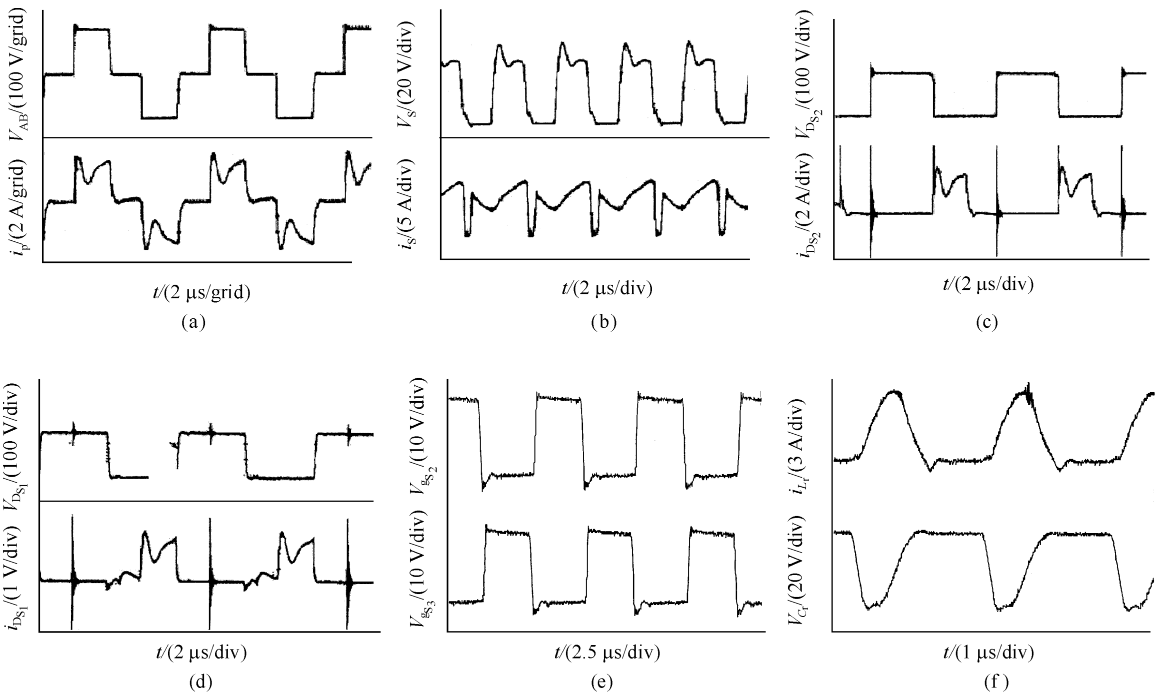

Fig. 4 Experimental waveforms. (a) V_{AB}, i_p; (b) V_s, i_s; (c) $V_{D_{S_2}}, i_{D_{S_2}}$; (d) $V_{D_{S_1}}, i_{D_{S_1}}$; (e) $V_{g_{S_2}}, V_{g_{S_3}}$; (f) V_{C_r}, i_{L_r}

the voltage V_{DS_2} and current i_{DS_2} of the inner switch S_2. Obviously, the current i_{DS_2} falls to zero prior to the voltage rising. Therefore, a true ZCS action is achieved. Figure 4(d) shows the voltage V_{DS_1} and current i_{DS_1} of outer switch S_1, evidently a true ZVS action is realized. Figure 4(e) shows the gate waveforms of the inner switches S_2, S_3. These two logic gates are out of the phase. Figure 4(f) shows the current wave form of L_d and voltage waveform of storage capacitor C_r.

Figure 5(a) shows the converter efficiency when it loads 10 A of current. The efficiency will be higher when the input voltage becomes higher. Figure 5(b) shows the efficiency in case of a different output current. When the input voltage is 440 V, it can be seen that if the converter is in full load (10 A), the efficiency can be increased by about 92.6%.

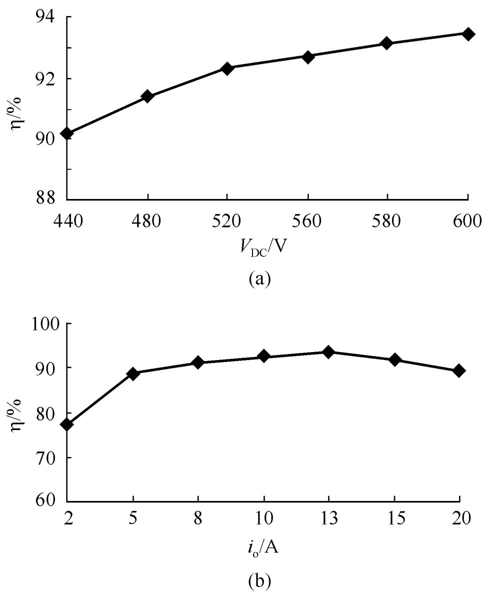

Fig. 5 Efficiency of converter

4 Conclusions

This paper proposes a novel three-level DC/DC converter. In this converter, a tapped inductor is used to achieve zero-voltage and zero-current switching (ZVZCS), It can reduce the voltage stress at the primary side switches, and eliminate the voltage spikes at the secondary side rectify diodes. By regulating the turn ratio of the tapped inductor, the voltage, which is used to reset the primary current, can be easily adjusted. No auxiliary active switch and the corresponding control circuit is needed. The power stage and its control are simple and easy to realize. The theoretical analysis and experimental results are given to confirm the performance of the proposed converter.

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