Compressed Page Walk Cache

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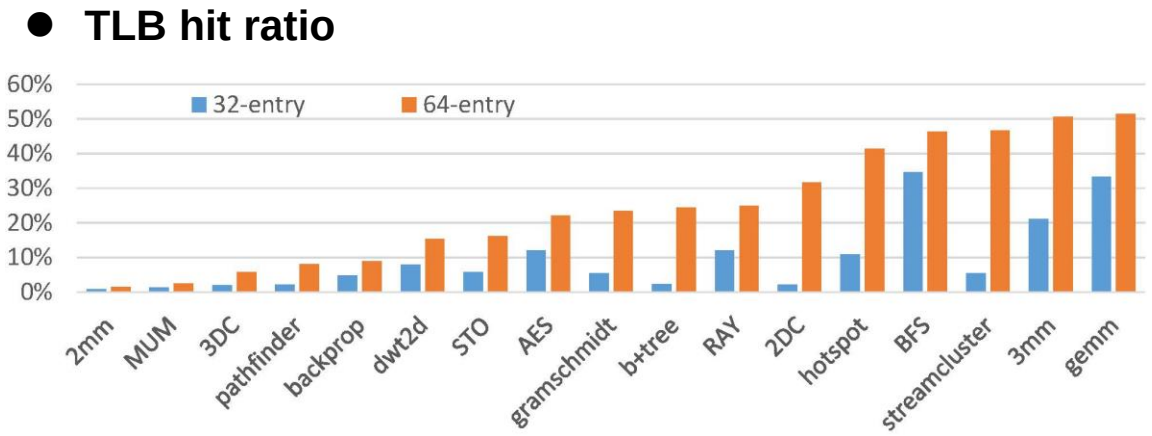
Problems & Ideas

- Problems of excessive address translation overhead
  - High miss ratio of TLB
  - Excessive page table accesses



- Ideas: Compressed Page Walk Cache (Redesgin the structure of page walk cache to hold more high level page table entry)
  - Reduce the overhead of TLB miss
  - Improve the hit ratio of PWC

Main Contributions

Contribution 1. We conduct a comprehensive investigation of all level page table entries accessed by typical benchmarks. We observe that the L4 and L3 indices exhibit good locality, causing the redundancy in TPC, while the low perfor mance of TPC is mainly caused by the poor locality of L2 indices.

Contribution 2. We propose the CPWC which can eliminate all redundancies in traditional PWC without increasing the lookup latency. Our CPWC can cache more page table entries, and effectively reduces the number of page table accesses during page walks. Additionally, CPWC implements parallel lookup by subtly providing the association information among three-level indices, avoiding the serial lookup.