

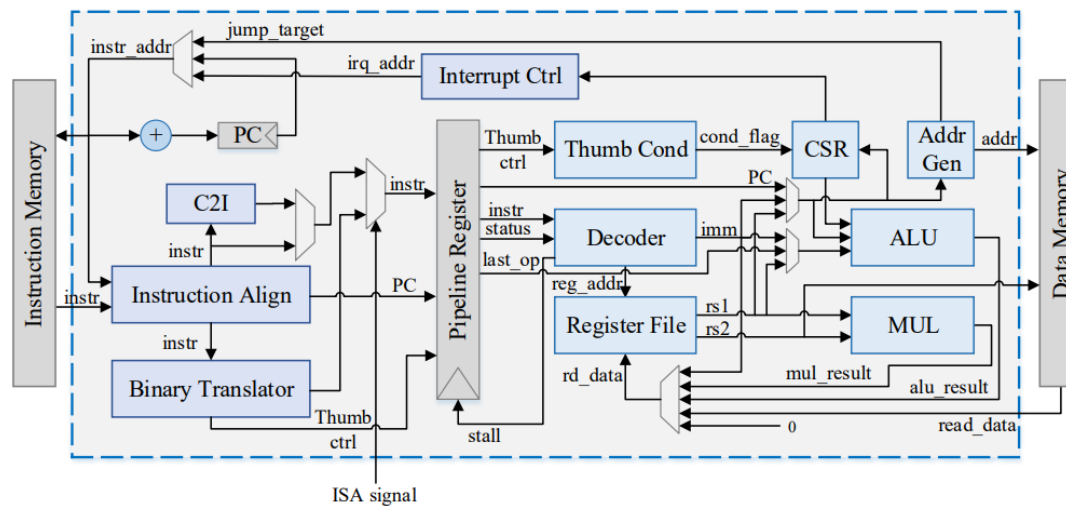
# RVAM16: A Low-Cost Multiple-ISA Processor Based on RISC-V and ARM Thumb

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# Problems & Ideas

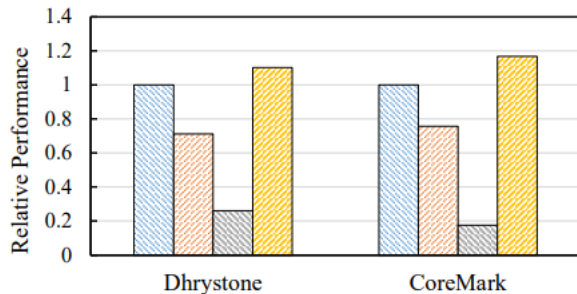
- The problem of software compatibility in the embedded field
  - numerous impressive ISAs have emerged
  - additional software cost and software ecosystem challenge
  - environment, performance, and cost limitations
- Ideas: Taking a low-cost multiple-ISA processor based on binary translation to solve software compatibility.



The microarchitecture of RVAM16 multiple-ISA processor core. The module of Binary Translator completes the translation of ARM Thumb instruction to RISC-V. RVAM16 improves the performance of running ARM Thumb programs by hardware supporting ARM Thumb condition flags, branch instructions, and condition execution.

# Main Contributions

- Contributions:
  - A low-cost Multiple-ISA processor microarchitecture based on hardware binary translation.
  - Hardware optimization methods to reduce the translation ratio of non-native and native ISAs and hardware overhead.
  - An implementation of the multiple-ISA processor prototype that supports both RV32IMC and ARMv6-M, as well as evaluating its performance, power and area.



- RVAM16 runs native RISC-V codes
- RVAM16 runs non-native ARM Thumb codes
- Only HBT runs non-native ARM Thumb codes
- Cortex-M0 runs ARM Thumb codes

Core	Area ( $\mu\text{m}^2$ )	Benchmark (Target ISA)	Power (mW)			Relative Energy
			Static	Dynamic	Total	
RVAM16	24269.28	Dhrystone (RISC-V)	1.69	1.51	3.20	0.84
		CoreMark (RISC-V)	1.69	1.59	3.28	0.90
		Dhrystone (ARM Thumb)	1.71	1.70	3.41	1.25
		CoreMark (ARM Thumb)	1.70	1.78	3.48	1.26
RISC-V + HBT	26658.41	Dhrystone (RISC-V)	1.86	1.48	3.34	0.87
		CoreMark (RISC-V)	1.86	1.55	3.41	0.94
		Dhrystone (ARM Thumb)	1.87	1.77	3.64	3.65
		CoreMark (ARM Thumb)	1.87	1.71	3.58	5.59
Base RISC-V Core	20757.91	Dhrystone (RISC-V)	1.37	1.42	2.79	0.73
		CoreMark (RISC-V)	1.36	1.53	2.89	0.79
Ibex	32802.67	Dhrystone (RISC-V)	2.29	2.70	4.99	0.93
		CoreMark (RISC-V)	2.29	3.26	5.55	1.04
Cortex-M0	26264.45	Dhrystone (ARM Thumb)	2.41	1.80	4.21	1.00
		CoreMark (ARM Thumb)	2.41	1.85	4.26	1.00

The evaluation results of the RVAM16 processor prototype. Left: relative performance of running Dhrystone and CoreMark. Right: the area, power and energy cost of different core at the same process technology and frequency.