

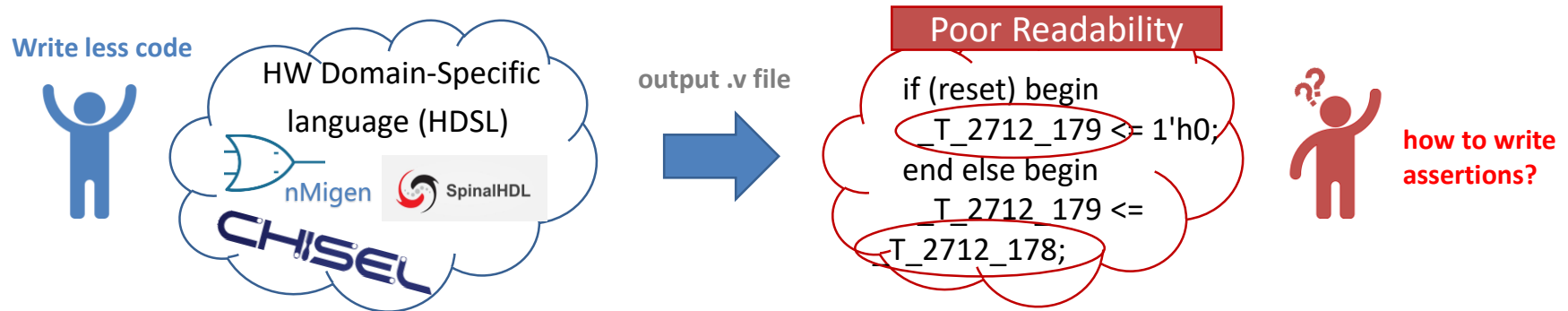
PyABV: A Framework for Enhancing PyRTL with Assertion-Based Verification

Yue CHENG, Tun LI, Hongji ZOU, Wanxia QU

Frontiers of Computer Science, DOI: [10.1007/s11704-024-40127-0](https://doi.org/10.1007/s11704-024-40127-0)

Problems & Ideas

- Problems: The Lack of ABV in HADM:
 - Which forces designers have to write assertions based on the Verilog code automatically generated from HDSLs descriptions.
 - The poor readability and complexity of auto-generated Verilog is hard for designers to write assertions on the generated code, which makes productivity gains from HADM are lost in verification.



- Ideas: We proposed PyABV, a framework to model assertions, generate and synthesis monitors from assertions for simulation and for on-line monitoring.

Main Contributions

- Contributions:
 - Integrate ABV in HADM and model SVA in Python;
 - Support the simulation semantics of SVA and explore various optimization techniques, such as multi-threading and coroutines, to enhance dynamic verification;
 - Adopt a feature-oriented programming approach to support synthesized assertion integration, which makes assertion hardware checkers be composed to designs under verification easily and flexibly.

