FPGA Sharing in the Cloud: A Comprehensive Analysis

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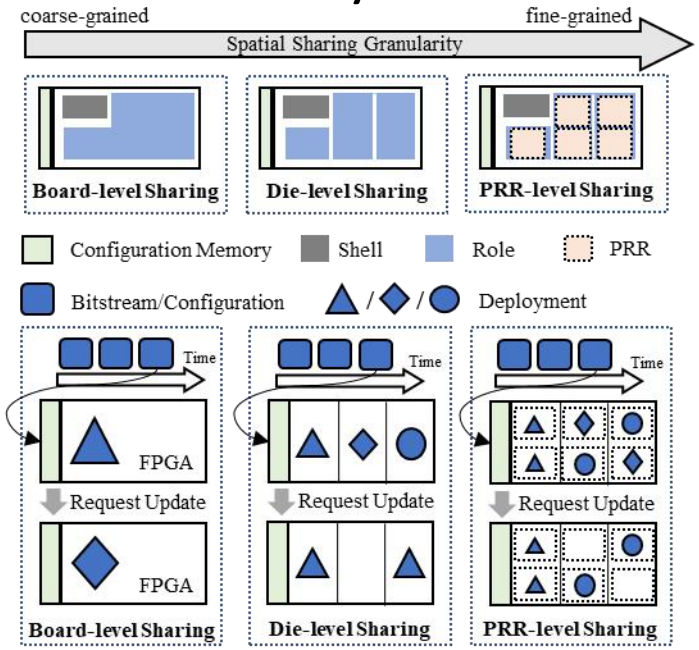
Problems & Ideas

- Problems of FPGA sharing in cloud
  - There is very limited works discuss on the topic of FPGA resource sharing and specific sharing formats
  - Existing work lacks discussions on cloud FPGA sharing support and cost issues.
- Ideas: We examine related works of cloud FPGA sharing and provide a comprehensive analysis.



FPGA sharing granularity. Mainly contains three granularity, Board-level, Die-level and PRR-level

Main Contributions

- Contributions:
  - We examine the related works of resource-oriented FPGA sharing. We discuss corresponding concepts of shared resources and provide a classification based on the hierarchical organization;
  - We classify research works according to FPGA sharing supports including hardware support, software support, and security guarantee. We describe major system optimization solutions;
  - We present a preliminary cost study of sharing-based FPGA systems. Focusing on the attribution and processing stages, we classify these connected expenses.

Table 3 Supports for FPGA sharing

Category	Support	Related work
Hardware	Reconfiguration	[15,21,32,33,63]
	Connectivity	[30,46]
	Partition	[1,21,55]
Software	Isolation	[64]
	Migration	[65,66]
	Abstraction	[64,67]
	Virtualization	[18,68,69]
	Management	[15,46,60]
	Scheduling	[21,44,47,56,69]
	Development	[18,31,47]
Security	Data Confidentiality	[70–72]
	Bitstream Protection	[60,73–75]
	Power Control	[76–78]
	Workload Isolation	[3,30,45,79]
	Configuration Refresh	[63,80]

Table 4 Software support of FPGA sharing, categorized by target partition of device.

Work	SW Support	Organization	Contorl Unit	Sharing Manner	Year	Key Technique
RC3E [56]	RV, RM, TS	PRR	I/O	S&T	2016	hypervisor
VFR [54]	RV, RM, TS	PRR	I/O	S&T	2016	PRR manager
RRaaS [45]	RV, RM, TS, DT	PRR	API	S&T	2016	NoC, hypervisor
hCODE [47]	RV, RM, TS, DT	PRR	I/O & logic	S&T	2018	PRR manager
FPGApooling [21]	RV, RM, TS	PRR	I/O& logic	S&T	2021	Pooling scheduler
Feniks [64]	RV,RM,SA,PI	DPRR	I/O & logic	S&T	2017	Region isolation, I/O abstraction
RACOS [46]	RV, RM	DPRR	Accelertor API	S&T	2017	PCIe controller
LiveMig [66]	RV,TM,TS	DPRR	I/O& logic	S&T	2018	Live task migration
AmorphOS [30]	RV, RM	DPRR	I/O	S&T	2018	PCIe controller, Zone manager
ViTAL [18]	RV, RM, DT	DPRR	I/O & logic	S&T	2020	Compiler, Hypervisor
Coyote [67]	RV, RM, SA, TS	DPRR	I/O & logic	S&T	2020	OS abstraction
Hetero-ViTAL [31]	RV, RM, TS, DT	DPRR	I/O & logic	S&T	2021	Hypervisor, LL Block
pvFPGA [44]	RM, TS	Board	Accelertor API	T	2013	Xen VMM
Catapult [15]	RM, TS	Board	I/O & Network	T	2014	Resource controller
VFACC [60]	RM, TS	Board	Accelertor API	T	2015	Hypervisor, PCIe controller
Blaze [57]	RM, TS, DT	Board	I/O	T	2016	Run-time manager
QMC [83]	RM, TS	Board	I/O & Network	T	2017	Avalone connector
Migration [65]	RM,TN,TS.	Board	API & Network	T	2017	vFPGA-based Migration
RTDNN [69]	RM, TS	Board	Accelertor API	T	2018	Hypervisor
FPGAvirt [49]	RM, TS	Board	Network	T	2018	NoC, Sevice manager

* **PI** means performance isolation, **TM** means task migration, **SA** means software abstraction, **RV** means resource virtualization. **RM** means resource management, **TS** means task scheduling, **DT** means development tools.

The comprehension analysis of the FPGA sharing works, we deeply explored the FPGA sharing supports.