PhyLS: An AI-driven Physically Aware Synthesis Platform

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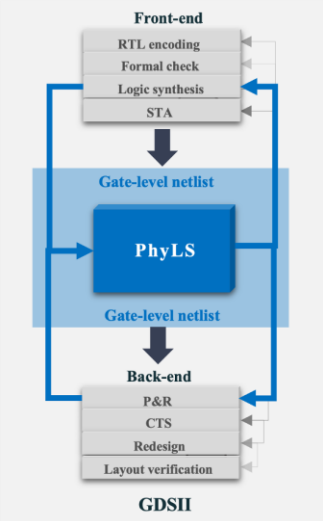
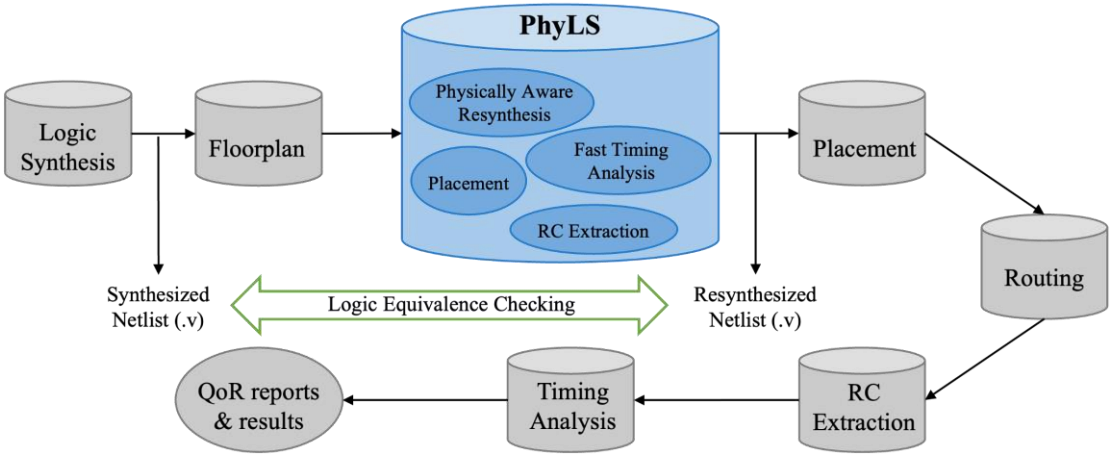
Problems & Ideas

- A critical bottleneck in modern digital IC design is the gap between FE logic synthesis and BE physical design.
  - Traditional synthesis tools often lack physical awareness, generating sub-optimal netlists.
- Ideas: We propose PhyLS, an AI-native, physically aware synthesis platform designed to bridge the FE-BE gap.

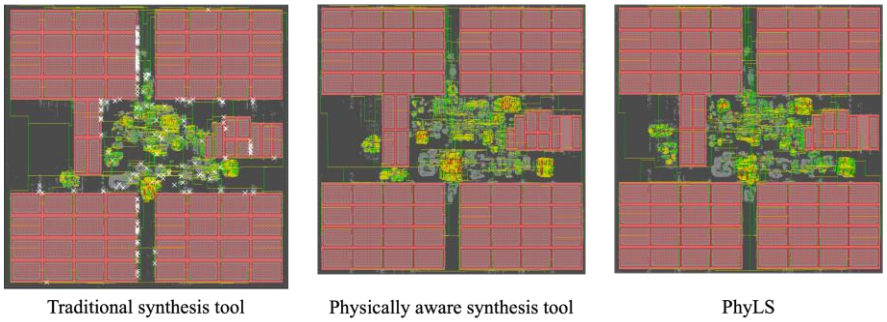


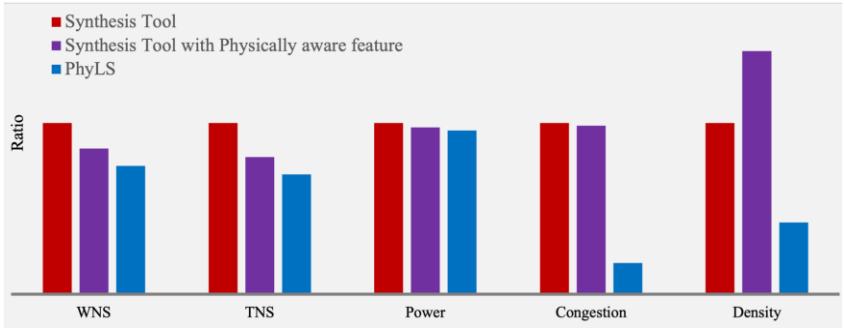


Left: PhyLS acts as a bridge between FE logic synthesis and BE physical implementation. Right: The PhyLS internal engine utilizes predictive modeling (GNN) and intelligent agents (RL) to perform physically aware resynthesis

Main Contributions

- Contributions:
  - The efficacy of PhyLS was validated using commercial TSMC 28nm process technology.
  - Achieved over 15% improvement in final layout Power, Performance, and Area (PPA).
  - Reduced Worst Negative Slack (WNS) by over 10% and Total Negative Slack (TNS) by over 15%.
  - Significantly reduced congestion and density, accelerating the design convergence cycle.





Left: Layout comparison showing PhyLS (rightmost) generates a cleaner layout with significantly less congestion compared to traditional methods. Right: Quantitative results showing PhyLS (blue bar) achieves superior WNS, TNS, Power, and Congestion metrics compared to existing industry tools