A New Design of Parity Preserving Reversible Multipliers Based on Multiple-Control Toffoli Synthesis Targeting Emerging Quantum Circuits

Mojtaba NOORALLAHZADEH, Mohammad MOSLEH, Kamalika DATTA

Frontiers of Computer Science, DOI: 10.1007/s11704-023-2492-3

Problems & Ideas

- Problems of conventional logic :
  - With the increase in fabrication density over the last few decades, semiconductor technology is being pushed to extreme limits and power dissipation has become a major issue.
  - The loss of information is associated with laws of physics requiring that one bit of information lost dissipates $k\,T \ln 2$ of energy, where k is Boltzmann's constant and T is the temperature of the system.
  - Ideas: The computing must be done using reversible logic technologies because the energy consumption of reversible technologies is theoretically zero.

Main Contributions

- Contributions:
  - Six new reversible functional blocks (called *Z*-block, *F*-block *A*-block, *T* -block, *S*-block, and L-block), along with their reversible and quantum gate realizations, have been proposed;
  - The layout of a parity-preserving reversible full-adder using reversible functional blocks has been presented;
  - The designs of two reversible parity-preserving multipliers have been shown, with partial product generation and multi-operand addition to generating the final product ;
  - The proposed designs have been evaluated against existing published works, with respect QC, GC, GO, and CI.

TABLE V
COMPARISON OF PARITY-PRESERVING REVERSIBLE UNSIGNED MULTIPLIER DESIGNS

Designs	QC	GO	GI	GC
[25]	244	64	64	48
[24]	205	49	49	52
[26] #1	184	56	56	36
[26] #2	177	49	49	28
[27]	184	44	44	33
[23]	169	45	45	26
[28]	300	44	45	124
Proposed	151	39	39	19
% improv. [25]	38.11	39.06	39.06	60.41
% improv. [24]	26.34	20.40	20.40	63.46
% improv. [26] #1	17.93	30.35	30.35	47.22
% improv. [26] #2	14.68	20.40	20.40	32.14
% improv. [27]	17.93	11.36	11.36	42.42
% improv. [23]	10.65	13.33	13.33	26.92
% improv. [28]	49.66	11.36	13.33	84.67
Average	25.04	20.89	21.17	51.03

TABLE VII
COMPARISON OF PARITY-PRESERVING REVERSIBLE SIGNED MULTIPLIER DESIGNS

Designs	QC	GO	GI	GC
[12]	401	90	90	57
[26]	297	86	86	46
[23]	289	82	82	44
Proposed	262	74	74	35
% improv. [12]	34.66	17.77	17.77	38.59
% improv. [26]	11.78	13.95	13.95	23.91
% improv. [23]	9.34	9.75	9.75	20.45
Average	18.59	13.82	13.82	27.65

The results of unsigned and signed multiplier circuit designs were obtained based on the proposed blocks. Left: unsigned multiplier. Right: signed multiplier