

TRAP : trace runtime analysis of properties

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Problems & Ideas

- Problems of sound use of Virtual Prototyping tools for codesign
 - How to express properties close to natural language requirements
 - How to explore and debug very large simulation traces
 - How to avoid recompilation of large simulation models during debug
- Ideas: Use Models to drive the debugging process
 - Use Behavioral Patterns to simplify the specification language
 - Use the Models to instrument the simulation code
 - Use dynamic binding at run-time to transform raw traces into sequences of property-relevant logical events

Main Contribution

- Our Virtual Prototyping Environment based on SimSoC

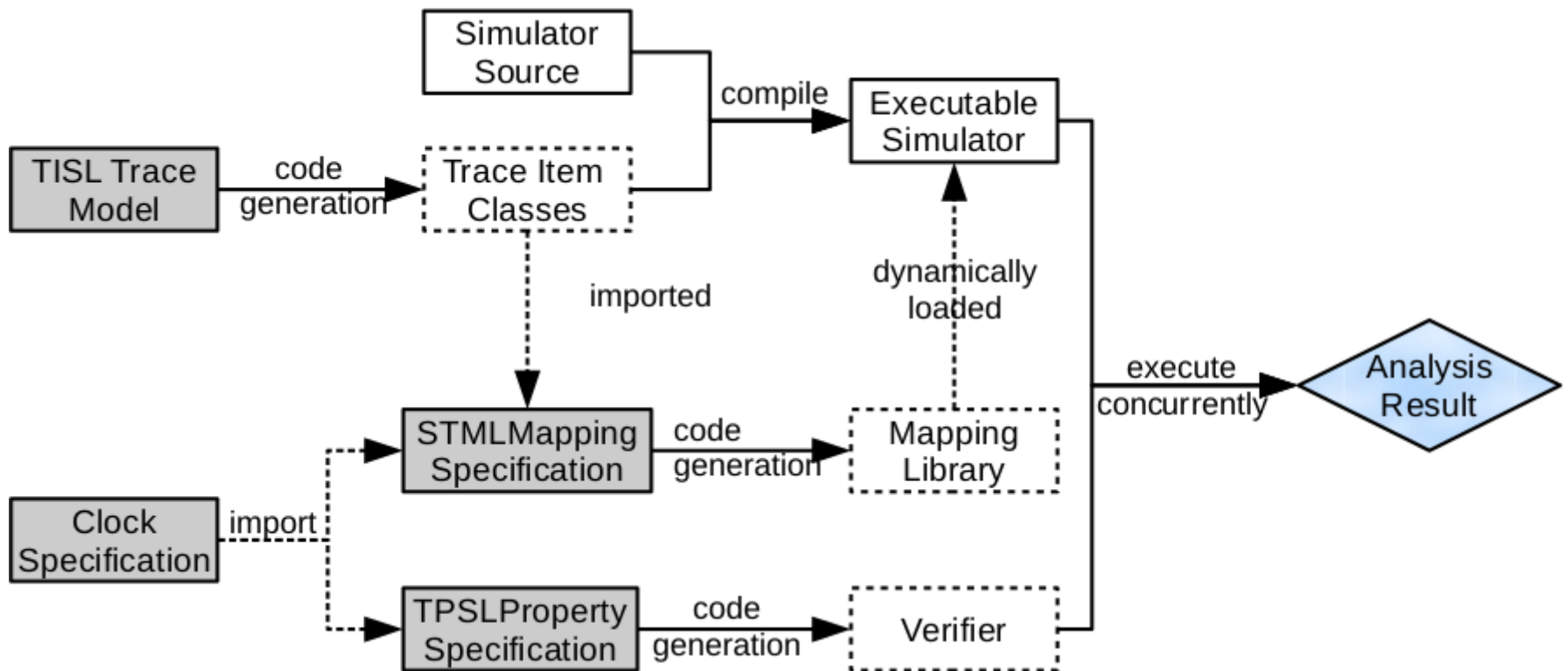


Fig. TRAP: 3 DSLs for Runtime Verification